CA-IS302x Low-Power Bidirectional I²C Isolators

1. Features

- **Bidirectional Data Transfer from DC to 2.0MHz**
- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: >40 years
  - Withstands up to 3.75kV$_{RMS}$ (narrow-body package) and 5kV$_{RMS}$ (wide-body packages) isolation rating for 60s (V_{ISO})
  - Narrow-body and wide-body Packages (4mm or 8mm Creepage and Clearance)
  - ±150 kV/μs typical CMTI
  - Schmitt trigger inputs for high noise immunity
  - High electromagnetic immunity and withstands ±10kV surge
  - ±8kV Human Body Model ESD Protection
- **3.0V to 5.5V Wide Supply Operation**
- **Wide Operating Temperature Range: -55°C to 125°C**
- **RoHS-Compliant Packages**
  - Narrow-body SOIC8-NB(S) package
  - Wide-body SOIC8-WB(G) package
  - Wide-body SOIC16-WB(W) package
- **Open-drain Outputs**
  - 3.5mA Side A sink current capability
  - 35mA Side B sink current capability

2. Applications

- I²C, SMBus, PMBus™ Interfaces
- Motor control systems
- Medical Equipment
- Battery Management
- Instrumentation

3. General Description

The CA-IS302x devices are complete dual-channel, galvanic digital isolators with up to 3.75kV$_{RMS}$ (narrow-body package)/5kV$_{RMS}$ (wide-body package) isolation rating and ±150kV/μs typical CMTI. All device versions have Schmitt trigger inputs for high noise immunity and each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier to provide high electromagnetic immunity and low EMI. These devices feature high-integration design and only require fewer external components, V_{DDA}, V_{DDB} bypass capacitors and pull-up resistors, to build an isolated I²C interface.

This family of devices operates from DC to 2.0MHz. The CA-IS3020 offers two bidirectional, open-drain channels for applications, such as multi-master I²C, that require data and clock to be transmitted in both directions on the same line. The CA-IS3021 provides an isolated I²C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). All devices feature independent 3.0V to 5.5V supplies on each side of the isolator and the logic levels are set independently on either side by V_{DDA} and V_{DDB}. A simplified block diagram for a single CA-IS302x channel is shown in the figure below.

The CA-IS302x family are specified over the -55°C to +125°C operating temperature range and are available in 8-pin SOIC narrow body package, 8-pin SOIC wide body package and 16-pin SOIC wide body package. The wide temperature range and high isolation voltage make the devices ideal for use in harsh industrial environments.

Device information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3020 CA-IS3021	SOIC8(S)	4.90mm ×3.90 mm
	SOIC8-WB(G)	5.85 mm ×7.50 mm
	SOIC16-WB(W)	10.30 mm × 7.50 mm

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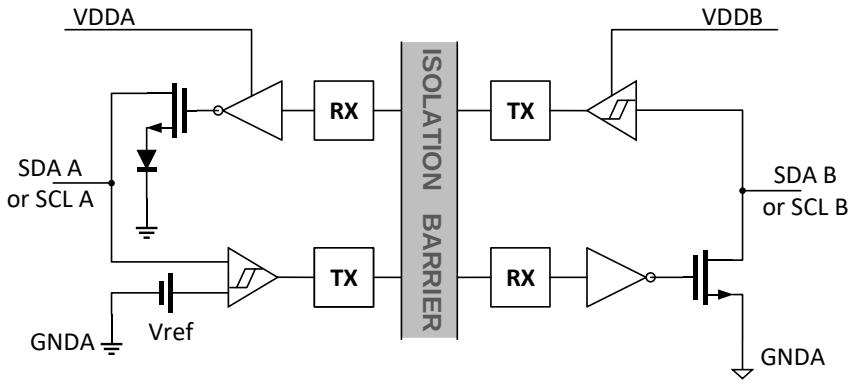
CA-IS302x functional block diagram



4. Ordering Information

Table. 4-1 Ordering Information

Part Number	# of Bidirectional Channels	# of Unidirectional Channels	Rated Voltage (kV)	Default Output	Package
CA-IS3020S	2	0	3.75	Open drain	SOIC8
CA-IS3021S	1	1	3.75	Open drain	SOIC8
CA-IS3020G	2	0	5.0	Open drain	SOIC8-WB
CA-IS3021G	1	1	5.0	Open drain	SOIC8-WB
CA-IS3020W	2	0	5.0	Open drain	SOIC16-WB
CA-IS3021W	1	1	5.0	Open drain	SOIC16-WB

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Contents

5. Revision History

Revision 0: Initial version.
Revision 0 to Revision A

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6. Pin Configuration and Description

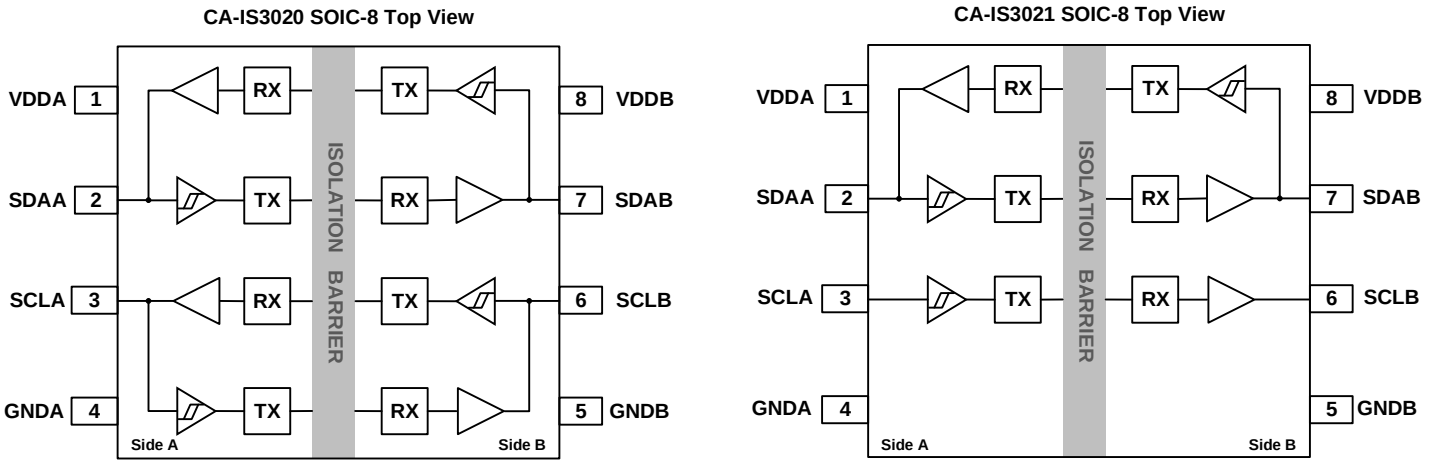

Figure. 6-1 CA-IS3020/21 SOIC-8 Top View

Table. 6-1 CA-IS3020 pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power	Power supply for side A.
SDAA	2	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	3	Digital I/O	Bidirectional clock input/output on side A. SCLA is translated to/from SCLB and is an open-drain output.
GNDA	4	Ground	Ground reference for side A.
GNDB	5	Ground	Ground reference for side B.
SCLB	6	Digital I/O	Bidirectional clock input/output on side B. SCLB is translated to/from SCLA and is an open-drain output.
SDAB	7	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	8	Power	Power supply for side B.

Table. 6-2 CA-IS3021 pin Description

Pin name	Pin number	Type	Description
VDDA	1	Power	Power supply for side A.
SDAA	2	Digital I/O	Bidirectional data input/output on side A. SDAA is translated to/from SDAB and is an open-drain output.
SCLA	3	Digital I/O	Clock input on side A. SCLA is translated to SCLB.
GNDA	4	Ground	Ground reference for side A.
GNDB	5	Ground	Ground reference for side B.
SCLB	6	Digital I/O	Clock output on side B. SCLB is translated from SCLA and is an open-drain output.
SDAB	7	Digital I/O	Bidirectional data input/output on side B. SDAB is translated to/from SDAA and is an open-drain output.
VDDB	8	Power	Power supply for side B.

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7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum Value	Maximum Value	Unit
V_{DDA}, V_{DDB}	Power supply voltage[2]	-0.5	6.0	V
SDAA, SCLA	Input/Output voltage	-0.5	V_{DDA}+0.5[3]	V
SDAB, SCLB	Input/Output voltage	-0.5	V_{DDB}+0.5[3]	V
I_{OA}	Output Current	-20	20	mA
I_{OB}	Output Current	-100	100	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. The maximum voltage must not be exceed 6 V.

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±8000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

Parameters		Minimum Value	Maximum Value	Unit
V_{DDA}, V_{DDB}	Power supply voltage	3.0	5.5	V
V_{SDDA}, V_{VSCLA}	A side input voltage	0	V_{DDA}	V
V_{SDDB}, V_{VSCLB}	B side input voltage	0	V_{DDB}	V
V_{ILA}	A side Input low voltage	0	0.5	V
V_{IHA}	A side Input high voltage	0.7xV_{DDA}	V_{DDA}	V
V_{ILB}	B side Input low voltage	0	0.3xV_{DDB}	V
V_{IHB}	B side Input high voltage	0.7xV_{DDB}	VDDB	V
I_{OLA}	A side Output current (low level)	0.5	3.5	mA
I_{OLB}	B side Output current (low level)	0.5	35	mA
C_A	Maximum load capacitance on A side		40	pF
C_B	Maximum load capacitance on B side		400	pF
f_{MAX}	Maximum Frequency		2	MHz
T_A	Environmental temperature	-40	125	°C
T_J	Junction temperature	-40	150	°C

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7.4. Thermal Information

Thermal Metric		CA-IS302x			Unit
		W(SOIC-16)	G(SOIC-8)	S(SOIC-8)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	92.3	109.0	°C/W

7.5. Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
P_D	Maximum power dissipation (both sides)	V_{DDA} = V_{DDB} = 5.5 V, T_J = 150 °C, C_A = 40 pF, C_B = 400 pF; Input a 1-MHz 50% duty cycle clock signal			86	mW
P_{DA}	Maximum power dissipation (side-A)				34	mW
P_{DB}	Maximum power dissipation (side-B)				52	mW

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7.6. Insulation Specifications

Parameters		Test conditions	Value			Unit
			W	G	S	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	8	4	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	19	14	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	>600	>600	V
	Material group	In accordance with IEC 60664-1	I	I	I	
IEC 60664-1 over-voltage category		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	I-III	n/a	
DIN V VDE V 0884-11:2017-01[1]						
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	849	565	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	600	400	V_{RMS}
		DC voltage	849	849	565	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	7070	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method in accordance with IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	6250	6250	5000	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety test of the sub-category 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	≤5	pC
		Method a, after environmental test of the sub-category 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	≤5	
		Method b1, routine test (100% production test) and preprocessing (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	~0.5	pF
R_{IO}	Isolation resistance[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	$>10^{9}$	
	Contaminant level		2	2	2	
UL 1577						
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	5000	3750	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

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7.7. Safety-Related Certifications

VDE (pending)	CSA (pending)	UL	CQC	TUV (pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to CSA/IEC 60950-1 and CSA/IEC 62368-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017
		SOP8-S: 3750 V_{RMS}; SOP8-G: 5000V_{RMS};	SOP8-S: Basic insulation, 400 V_{RMS} maximum working voltage. SOP8-G: Reinforced insulation, 600 V_{RMS} maximum working voltage. (Altitude ≤ 5000 m)	
		Certificate number: E511334	Certificate number: SOP8-S: CQC20001267428 SOP8-G: CQC20001267438	

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7.8. Electrical Characteristics

Over recommended operating conditions, unless otherwise specified

Parameters		Test conditions	Minimum Value	Typical Value	Maximum Value	Unit
Side A						
V_{ILTA}	Logic low input threshold (SDAA and SCLA)		470	500	520	mV
V_{IHTA}	Logic high input threshold (SDAA and SCLA)		500	560	620	mV
V_{HYSA}	Voltage input hysteresis	V_{IHTA} -V_{ILTA}	40	60	80	mV
V_{OLA}	Logic low output voltage (SDAA and SCLA) [1]	0.5mA ≤ (I_{SDAA} and I_{SCLA}) ≤ 3.5mA	630	700	760	mV
ΔV_{OITA}	Logic-low output voltage to logic-high input voltage threshold difference (SDAA and SCLA)[1,2]	0.5mA ≤ (I_{SDAA} and I_{SCLA}) ≤ 3.5mA	100			mV
Side B						
V_{ILTB}	Logic low input threshold (SDAB and SCLB)		1.13	1.33	1.53	mV
V_{IHTB}	Logic low output voltage (SDAB and SCLB)		1.55	1.75	1.97	mV
V_{HYSB}	Voltage input hysteresis	V_{IHTB} -V_{ILTB}	0.30	0.42	0.54	mV
V_{OLB}	Logic-low output voltage (SDAB and SCLB)	0.5mA ≤ (I_{SDAB} and I_{SCLB}) ≤ 3.5mA			0.4	mV
Both Sides						
$\|I_L\|$	Input leakage currents, SDAA, SCLA, SDAA, and SCLA	V_{SDAA} = V_{SCLA} = VDDA V_{SDAB} = V_{SCLB} = VDDB			1	mV
C_I	Input capacitance to local ground (SDA1, SCL1, SDA2,and SCL2)			3		pF
CMTI	Common mode transient immunity	see Figure 8-3	100	150		kV/μS
V_{DDUV}	VDD_ Undervoltage-lockout threshold[3]		1.95	2.24	2.53	pF

Notes:

1. This parameter apply to the CA-IS3020 (SDAA, SCLA) and CA-IS3021 SDAA bidirectional lines only.
2. ΔV_{OITA} = V_{OLA} – V_{IHTA}. This is the minimum difference between logic-low output voltage and a logic-high input voltage.
3. Any $V_{DD\_}$ voltage on both side, less than the minimum will ensure device lockout. VDD_ voltage on both side A and side B greater than the maximum will prevent device lockout.

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7.9. Supply Current Characteristics

Over recommended operating conditions, unless otherwise specified, see Figure 8-1 for more information.

Parameters	Test conditions		Minimum Value	Typical Value	Maximum Value	Unit
3 V ≤ V_{DDA}, V_{DDB} ≤ 3.6 V						
CA-IS3020	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		4.9	5.7	mA
		I_{DDB}		4.7	5.2	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.4	2.8	
		I_{DDB}		2.2	2.6	
CA-IS3021	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.9	4.4	
		I_{DDB}		2.4	3.7	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		1.7	2.6	
		I_{DDB}		1.8	2.8	
4.5 V ≤ V_{DDA}, V_{DDB} ≤ 5.5V						
CA-IS3020	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		5.0	5.7	mA
		I_{DDB}		4.7	5.2	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		2.4	2.8	
		I_{DDB}		2.2	2.6	
CA-IS3021	V_{SDAA} = V_{SCLA} = GNDA; V_{SDAB} = V_{SCLB} = GNDB; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		3.0	4.5	
		I_{DDB}		2.5	3.8	
	V_{SDAA} = V_{SCLA} = V_{DDA}; V_{SDAB} = V_{SCLB} = V_{DDB}; R1 = R2 = OPEN; C1 = C2 = OPEN	I_{DDA}		1.8	2.7	
		I_{DDB}		1.9	2.9	

7.10. Timing Requirements

		Minimum Value	Typical Value	Maximum Value	Unit
t_{SP}	Input noise filter	10	25		ns

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7.11. Switching Characteristics

over recommended operating conditions, unless otherwise specified

Parameters		Test conditions		Minimum Value	Typical Value	Maximum Value	Unit
3 V ≤ (V_{DDA}, V_{DDB}) ≤ 3.6 V							
t_{fA}	Fall Time(SDAA, SCLA)	See figure 8-1 R1 = 953Ω C1 = 40pF	A side input from 0.7xV_{DDA} to 0.3xV_{DDA}	18	23	28	ns
			A side input from 0.9xV_{DDA} to 900mV	32	40	48	
t_{fB}	Fall Time (SDAB, SCLB)	See figure 8-1 R2 = 95.3Ω C2 = 400pF	B side input from 0.7xV_{DDB} to 0.3xV_{DDB}	12	16	20	
			B side input from 0.9xV_{DDB} to 400mV		30	60	
t_{PLHA-B}	Propagation Delay, Side A to Side B	See figure 8-1 R1 = 953Ω R2 = 95.3Ω C1 = C2 = 10pF	A side input = 0.55V to B side output = 0.7xV_{DDB}		100	135	
t_{PHLAB}	Propagation Delay, Side A to Side B		A side input = 0.7V to B side output = 0.4V		100	130	
PWD_{AB}	Pulse Width Distortion		$\lvert t_{PHLAB} - t_{PLHAB} \rvert$		7	30	
t_{PLHBA}[1]	Propagation Delay, Side B to Side A		B side input = 0.4xV_{DDB} to A side output = 0.7xV_{DDA}		80	100	
t_{PHLBA}[1]	Propagation Delay, Side B to Side A		B side input = 0.4xV_{DDB} to A side output = 0.9V		90	120	
PWD_{BA}[1]	Pulse Width Distortion		$\lvert t_{PHLBA} - t_{PLHBA} \rvert$		5	20	
t_{LOOPA}[1]	Loop propagation delay on Side A	See figure 8-2 R1 = 953Ω C1 = 40pF R2 = 95.3Ω C2 = 400pF	A side input = 0.4V to A side output = 0.3xV_{DDA}		200	220	
4.5 V ≤ (V_{DDA}, V_{DDB}) ≤ 5.5 V							
t_{fA}	Fall Time(SDAA, SCLA)	See figure 8-1 R1 = 1430Ω C1 = 40pF	A side input from 0.7xV_{DDA} to 0.3xV_{DDA}	10	12	14	ns
			A side input from 0.9xV_{DDA} to 900mV	40	50	60	
t_{fB}	Fall Time (SDAB, SCLB)	See figure8-1 R2 = 143Ω C2 = 400pF	B side input from 0.7xV_{DDB} to 0.3xV_{DDB}	8	10	12	
			B side input from 0.9xV_{DDB} to 400mV	20	28	36	
t_{PLHAB}	Propagation Delay, Side A to Side B	See figure 8-1 R1 = 1430Ω R2 = 143Ω C1 = C2 = 10pF	A side input = 0.55V to B side output = 0.7xV_{DDB}		100	120	
t_{PHLAB}	Propagation Delay, Side A to Side B		A side input = 0.7V to B side output = 0.4V		70	90	
PWD_{AB}	Pulse Width Distortion		$\lvert t_{PHLAB} - t_{PLHAB} \rvert$		30	45	
t_{PLHBA}[1]	Propagation delay, side B to side A		B side input = 0.4xV_{DDB} to A side output = 0.7xV_{DDA}		110	130	
t_{PHLBA}[1]	Propagation delay, Side B to side A		B side input = 0.4xV_{DDB} to A side output = 0.9V		100	150	
PWD_{BA}[1]	Pulse Width Distortion		$\lvert t_{PHLBA} - t_{PLHBA} \rvert$		8	20	
t_{LOOPA}[1]	Loop propagation delay on side A	See figure 8-2 R1 = 1430Ω C1 = 40pF R2 = 143Ω C2 = 400pF	A side input = 0.4V to A side output = 0.3xV_{DDA}		210	230	

Note:

1. This parameter apply to the CA-IS3020 (SDAA, SCLA) and CA-IS3021(SDAA) bidirectional lines only.

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8. Parameter Measurement Information

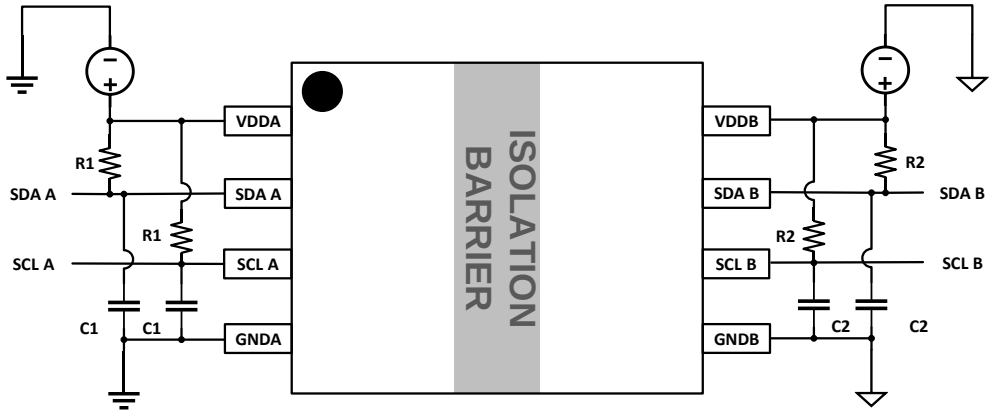

Figure. 8-1 Test Circuit

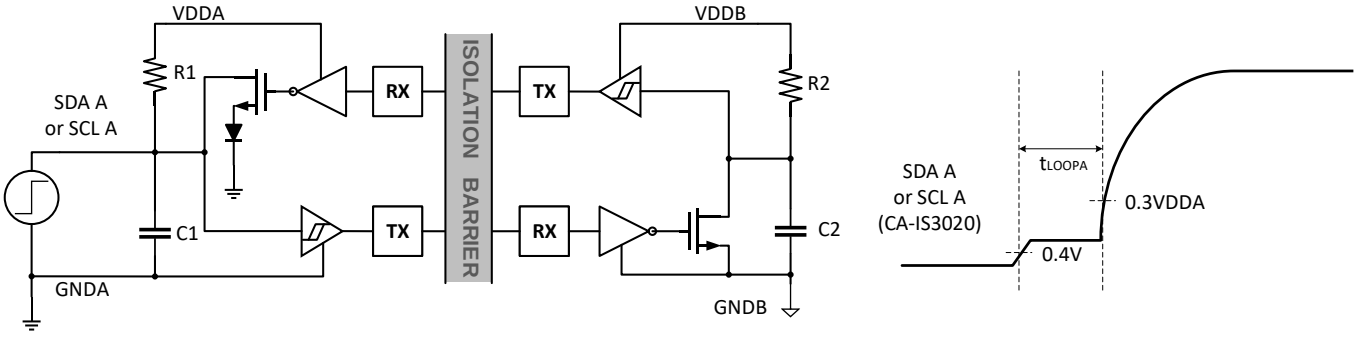

Figure. 8-2 t_{LOOPA} Test Circuit and Timing Diagram

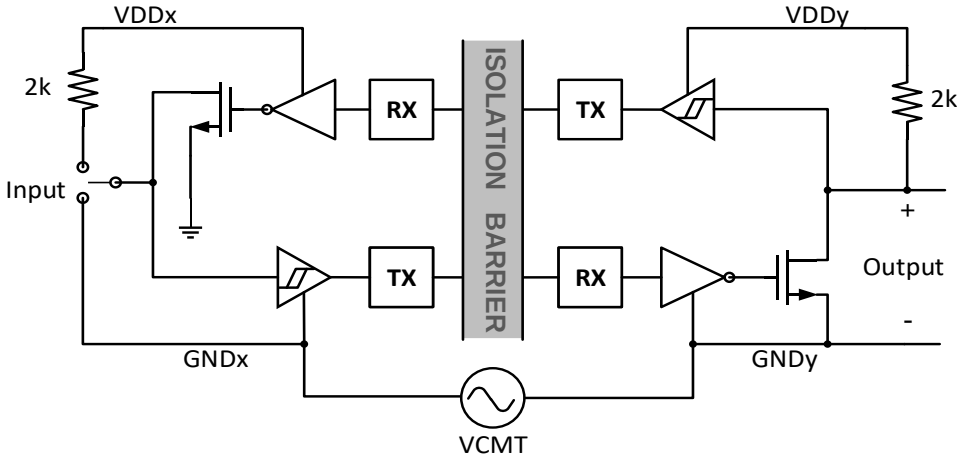

Figure. 8-3 Common-Mode Transient Immunity Test Circuit

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9. Detailed Description

9.1. Overview

The CA-IS302x family of devices is complete dual-channel, bidirectional galvanic digital isolators with up to 3.75kV$_{RMS}$ (narrow-body package) or 5kV$_{RMS}$ (wide-body package) isolation rating and ±150kV/µs typical CMTI. All devices have Schmitt trigger inputs for high noise immunity and each isolation channel has logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier. The CA-IS3020 offers two bidirectional, open-drain channels for applications, such as multi-master I^{2}C, that require data and clock to be transmitted in both directions on the same line. The CA-IS3021 provides an isolated I^{2}C compatible interface supporting master mode only, with a unidirectional clock (SCL), and bidirectional data (SDA). All devices can support up to 2.0MHz operating frequency and feature independent 3.0V to 5.5V supplies (V_{DDA} and V_{DDB}) on each side of the isolator to setup the logic levels independently on either side, see *Table 9-1* for the CA-IS302x key features.

The CA-IS302x family are specified over the -55°C to +125°C operating temperature range. The wide temperature range and high isolation voltage make the devices ideal for use in harsh industrial environments.

Table. 9-1 Key Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION[1]	MAXIMUM FREQUENCY
CA-IS3020	Bidirectional(SCL) Bidirectional(SDA)	Narrow-body package: 3750V$_{RMS}$, 5300 V$_{PK}$ Wide-body package: 5000V$_{RMS}$, 7071 V$_{PK}$	2.0MHz
CA-IS3021	Unidirectional(SCL) Bidirectional(SDA)		

Note:
1. For more details, please see the *Insulation Specifications* table.

9.2. Functional Block Diagrams

Compared with inductive isolation, the CA-IS302x devices based on capacitive isolation can get low power at high frequency operation, reduces propagation delay and jitter, and provide good immunity to magnetic fields. See *Figure 9-1* and *Figure 9-2* the CA-IS302x function block diagram for more details. To build the bidirectional signal path, the CA-IS302x integrated two unidirectional isolated signal lines for each bidirectional line. All of output channels provide open-drain output to comply with the standard I^{2}C interface. Side A is designed to connect to the low capacitance I^{2}C node with up to 40pF of load capacitance, while side B is designed for connecting to a fully loaded I^{2}C bus with up to 400 pF of load capacitance.

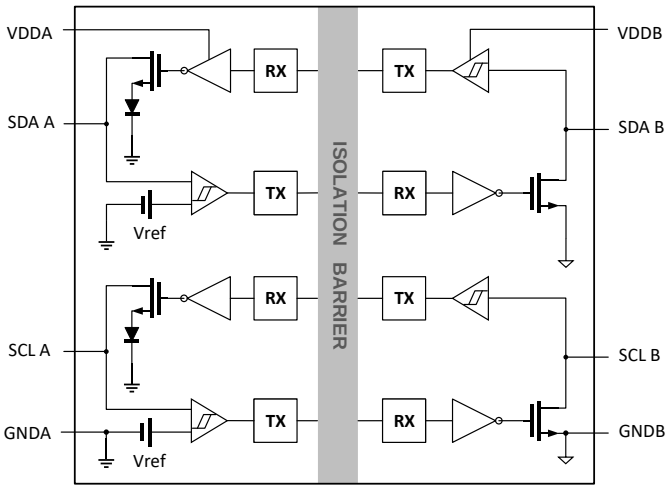

Figure. 9-1 The CA-IS3020 Block Diagram

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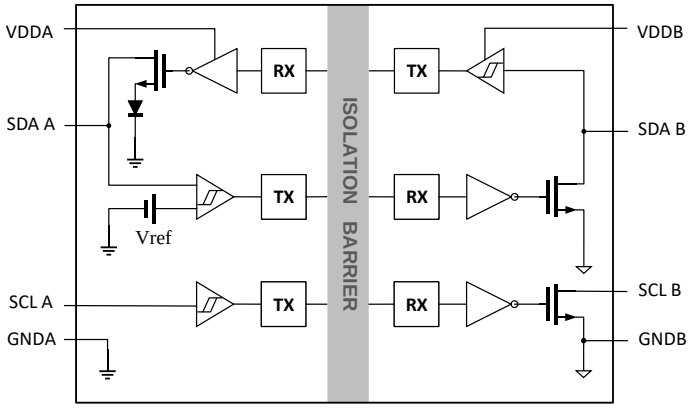

Figure. 9-2 The CA-IS3021 Block Diagram

9.3. Device Operation Modes

Table 9-2 lists the CA-IS302x functional modes. For optimal performance, ensure that the load capacitance on side A (C_A) is ≤ 40pF, and the load capacitance on side B (C_B) is ≤ 400pF. The maximum static output loading on side A is 3.5mA, while on side B, the maximum static output current is 35mA. For the bidirectional isolation channels, to prevent latch-up action, the A-side outputs comprise special buffers that regulate the logic-low voltage at approximately 700mV, and the maximum input logic-low voltage is 400mV. The internal comparator with hysteresis determines whether the logic-low level comes from the input or output based on the logic-low voltages at SDAA and SCLA pins. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B; thus preventing a latching action. The B side features conventional buffers that do not regulate logic-low output voltage. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device.

Table. 9-1 Truth Table[1]

POWER STATE	INPUT	OUTPUT
V_{DDA} or V_{DDB} < 1.95V	X	Hi-Z
V_{DDA} and V_{DDB} > 2.53V	L	L
V_{DDA} and V_{DDB} > 2.53V	H	Hi-Z
V_{DDA} and V_{DDB} > 2.53V	Hi-Z[2]	Indeterminate

Notes:

1. X = don't care; H = high level; L = low level; Hi-Z = high impedance.
2. Invalid input condition as an I²C system requires that a pull-up resistor to VDD_ is connected on the bus.

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10. Application Information

10.1. I²C bus

The Inter IC (I^2C) bus was developed by Philips Semiconductor in the early 1980s to simplify electronic products by reducing the number of parallel data lines. It is a simple, 2-wire, bidirectional bus for communication between different ICs (system controller, remote sensor, actuator etc. circuitry). 2-wire interfaces use only a data line (SDA) and a clock line (SCL) and allow to connect multiple slaves on the same bus without needing chip-select signals. This design is possible because each slave has its own unique address. 2-wire interfaces transmit an acknowledge bit after a successful read has been completed. Because 2-wire interfaces have only one data line, they can operate in half-duplex mode only, this means data can only be transmitted or received on a given cycle, but not both. Thus, the bus has two roles for nodes: master and addressable slave. This use of one or two fewer lines is a particularly useful advantage for the compact system designs and makes the I^2C bus is currently the industry's most widely used serial bus. The CA-IS302x family of digital isolators is ideal for use in I^2C bus to provide the required isolation between different ground potentials of the system circuitry to prevent ground loop currents that otherwise may falsify the acquired data.

The I^2C bus can operate in Standard mode, Fast mode, or High-speed mode, with maximum data rates of 100kbps (Standard mode), 400kbps (Fast mode), 1.7Mbps (High-speed mode with C_{bus} = 400pF). The CA-IS302x digital isolators can support up to 2.0MHz operating frequency, thus can support most of I^2C communication bus.

10.2. Typical Application

The CA-IS302x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. These devices do not require special power-supply sequencing, the logic levels are set independently on either side by V_{DDA} and V_{DDB}. The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions with 1.95V minimum threshold and 2.53V maximum threshold. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage event is detected on either of the supplies (V_{DDA}≤ 1.95V or V_{DDB} ≤ 1.95V), all bidirectional outputs become high-impedance and are pulled high by the external pullup resistor on the open-drain outputs.

The SDAA, SCLA, SDAB, SCLB pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 35mA for side B, and 3.5mA for side A. So the minimum pullup resistors on the input lines must be selected in such a way that input current drawn is ≤ 3.5mA on side A and output current drawn is ≤ 35mA on side B. The maximum pullup resistors on the input lines and output lines depend on the load and rise time requirements on the respective lines.

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with at least 0.1µF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible. *Figure 10-1* and *Figure 10-2* show typical operating circuit of the CA-IS3020 and CA-IS3022.

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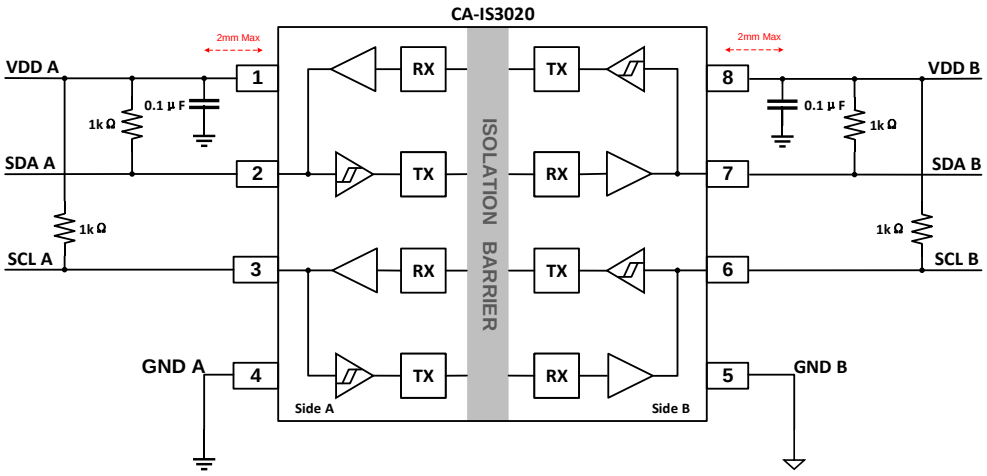

Figure. 10-1 The CA-IS3020 typical application circuit

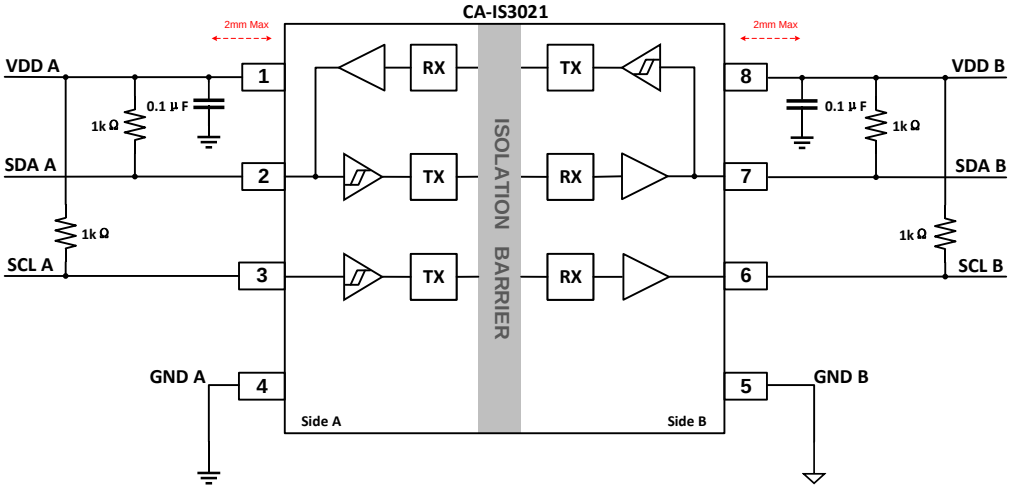

Figure. 10-2 The CA-IS3021 typical application circuit

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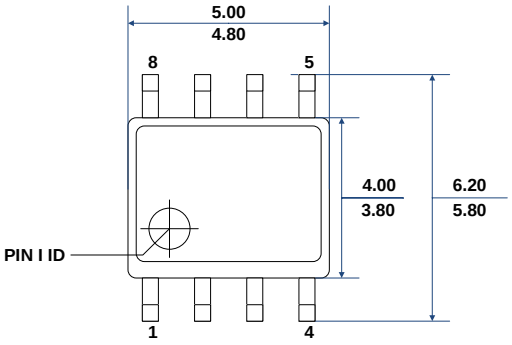
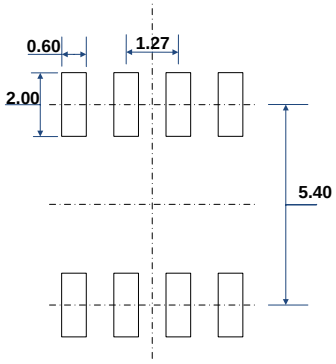
11. Package Information

11.1. 8-Pin Narrow Body SOIC Package

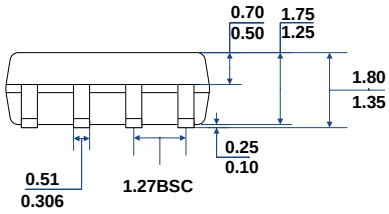
The following diagrams provide the package details and the recommended land pattern details for the CA-IS302x digital isolator in 8-pin narrow body SOIC package. All values for the dimensions are shown in millimeters.



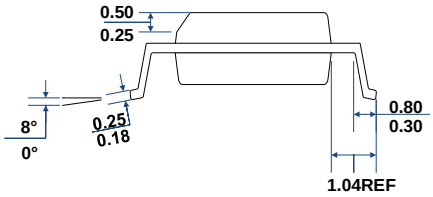
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

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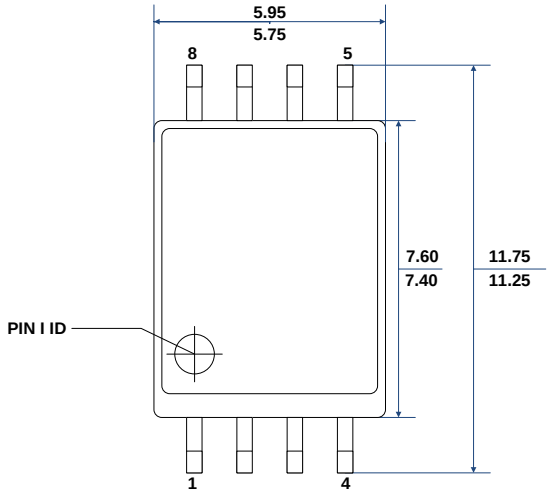
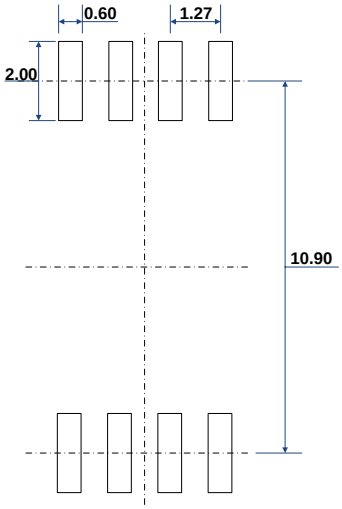
11.2. 8-Pin Wide Body SOIC Package Outline

The following diagrams provide the package details and the recommended land pattern details for the CA-IS302x digital isolator in 8-pin wide body SOIC package. All values for the dimensions are shown in millimeters.



TOP VIEW



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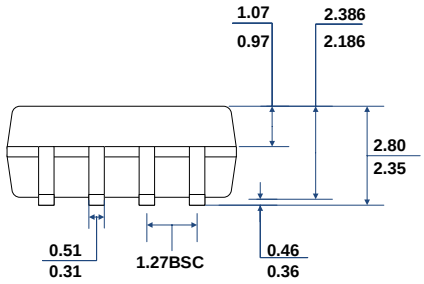
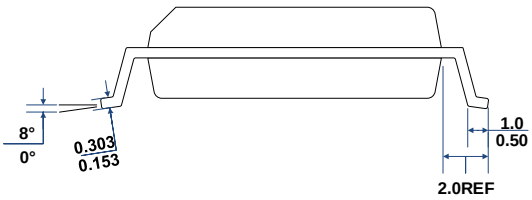


FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

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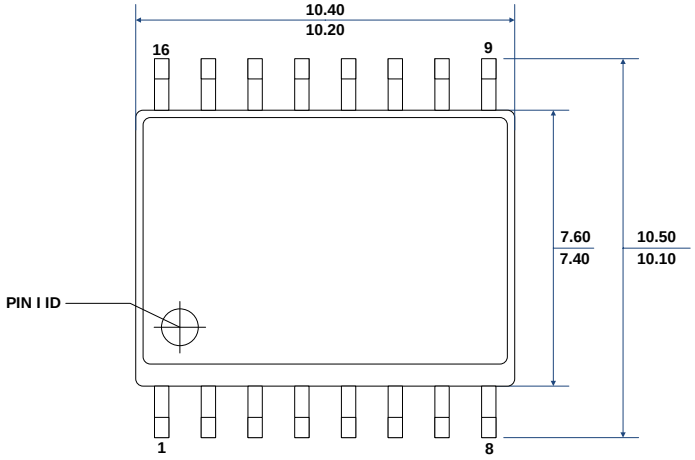
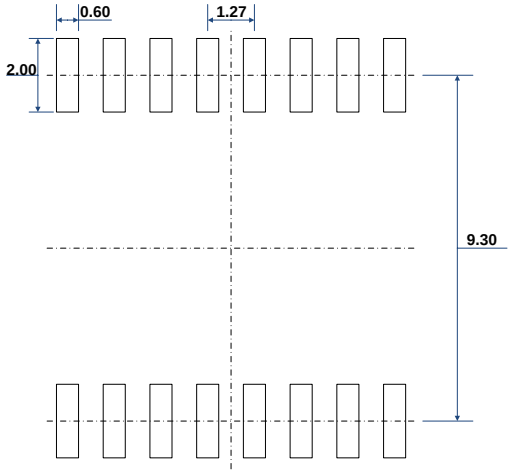
11.3. 16-Pin Wide Body SOIC Package Outline

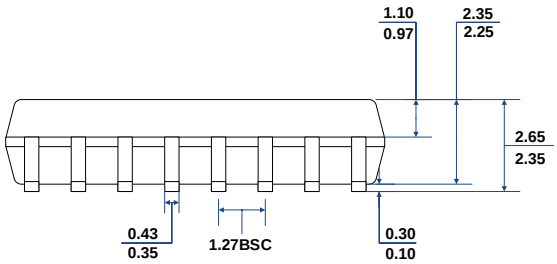
The following diagrams provide the package details and the recommended land pattern details for the CA-IS302x digital isolator in 16-pin wide body SOIC package. All values for the dimensions are shown in millimeters.



TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

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12. Soldering Temperature (reflow) Profile

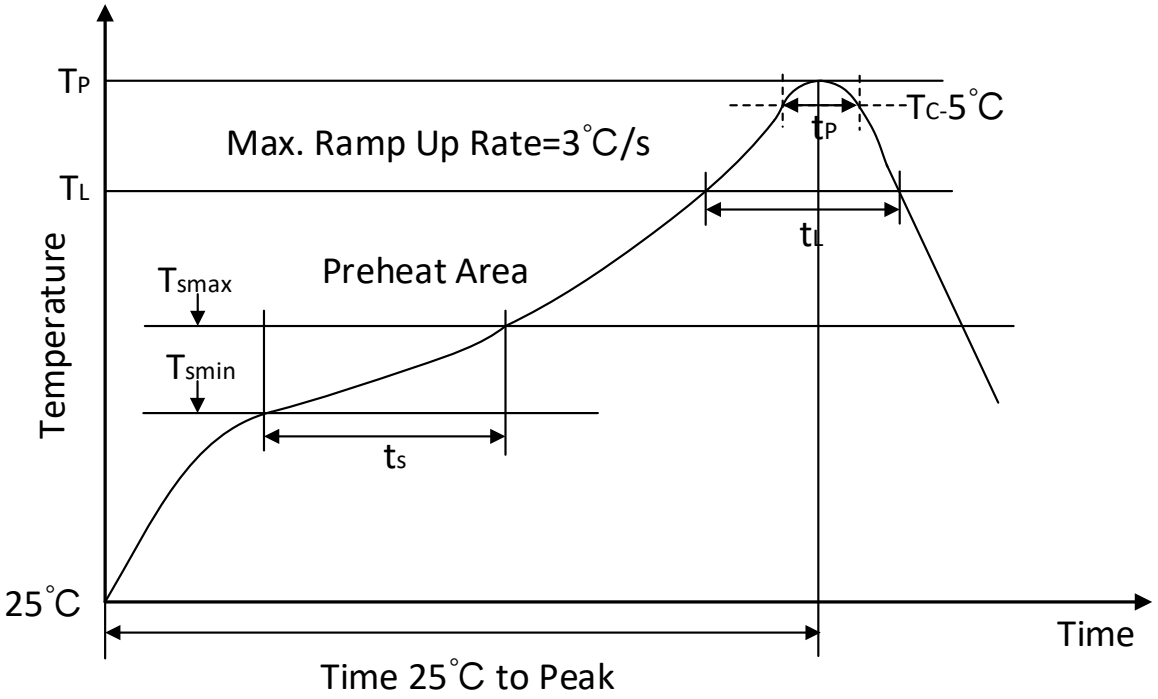

Figure. 12-1 Soldering Temperature (reflow) Profile

Table 12-1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

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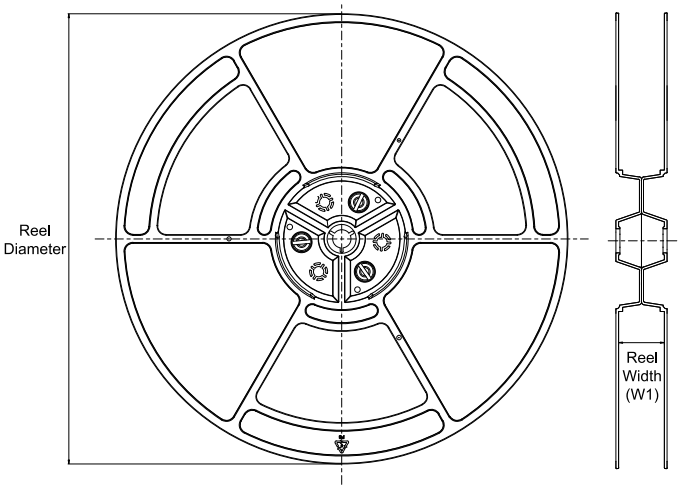
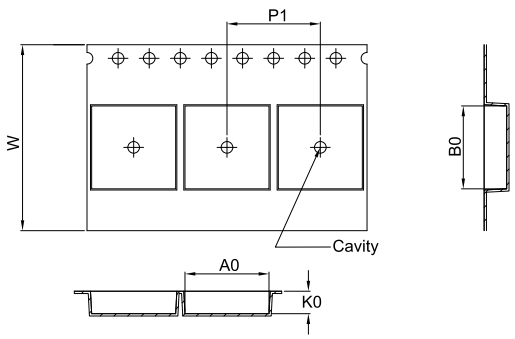
13. Tape and Reel Information

REEL DIMENSIONS

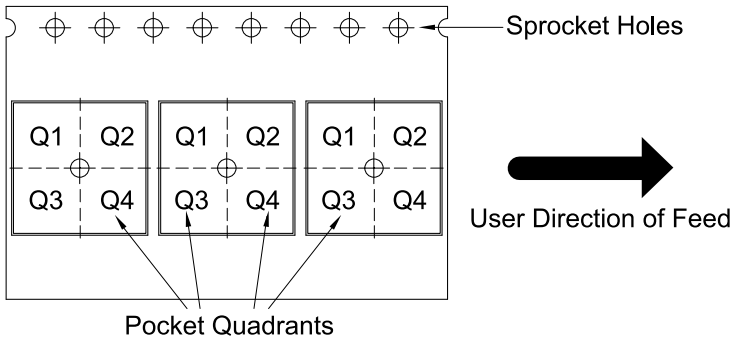


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3020S	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3020G	SOIC	G	8	1000	330	16.4	12.05	6.15	3.3	16.0	16.0	Q1
CA-IS3021S	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IS3021G	SOIC	G	8	1000	330	16.4	12.05	6.15	3.3	16.0	16.0	Q1
CA-IS3020W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3021W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1

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