1. DESCRIPTION

The XD/XL7660 Super Voltage Converters are monolithic CMOS voltage conversion ICs that guarantee significant performance advantages over other similar devices. They are direct replacements for the industry standard XD/XL7660 offering an extended operating supply voltage range up to 10V, with lower supply current. A Frequency Boost pin has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors.

The XD/XL7660 perform supply voltage conversions from positive to negative for an input range of 1.5V to 10V, resulting in complementary output voltages of -1.5V to -10V. Only two non-critical external capacitors are needed, for the charge pump and charge reservoir functions. The XD/XL7660 can be connected to function as a voltage doubler and will generate up to 18.8V with a 10V input. They can also be used as a voltage multipliers or voltage dividers.

Each chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be over-driven by an external clock.

The “LV” terminal may be tied to GND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 10V), the LV pin is left floating to prevent device latchup.

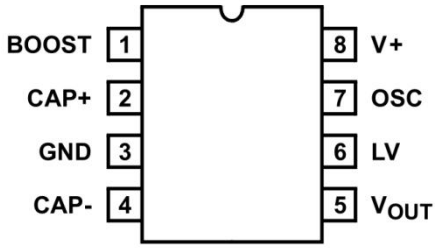
In some applications, an external Schottky diode from VOUT to CAP- is needed to guarantee latchup free operation.

2. FEATURES

- Guaranteed Lower Max Supply Current for All Temperature Ranges
- Wide Operating Voltage Range: 1.5V to 10V
- 100% Tested at 3V
- Boost Pin (Pin 1) for Higher Switching Frequency
- Guaranteed Minimum Power Efficiency of 96%
- Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%
- Improved SCR Latchup Protection
- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication VOUT = (-)nVIN
- Easy to Use; Requires Only Two External Non-Critical Passive Components

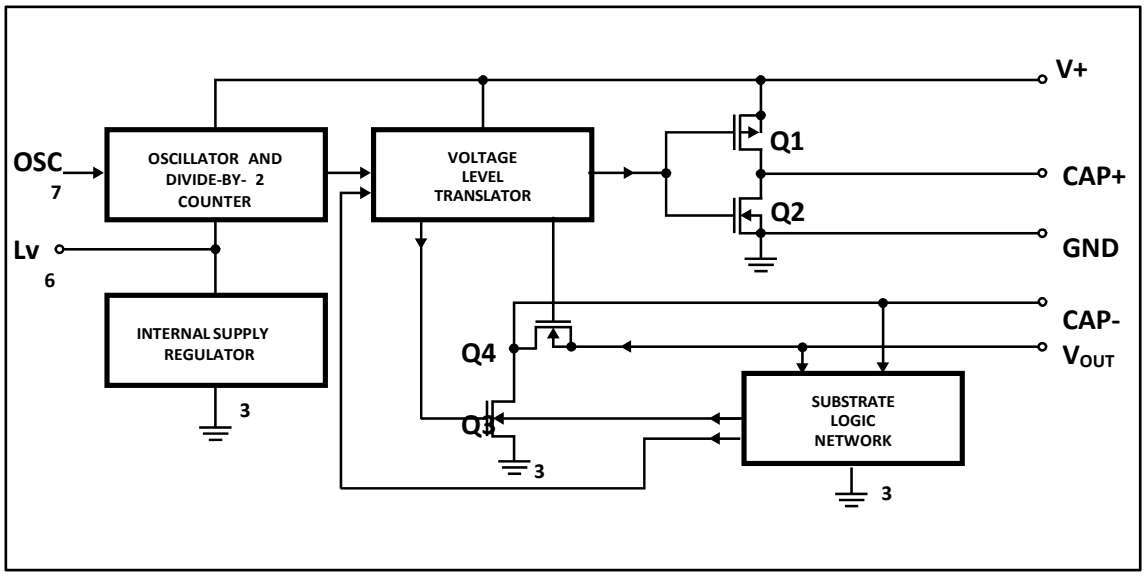
3. PIN CONFIGURATIONS

XD7660
XL7660



(TOP VIEW)

4. FUNCTIONAL BLOCK DIAGRAM



5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VCC	Supply voltage range			+10	V
Lv	Input voltage range	V+ < 5.5V	V	+ 0.3	V
OSC		V+ > 5.5V	-5.5V	+0.3V	V
I_{LV}	Current into Lv	VO<0	-	20	μA
V_{OUT}	Output short Duration	V_{SUPPLY} ⩽ 5.5V	Continuous		
T	Storage Temperature Range		-65	+150	℃
Operating Conditions					
Tamb	Ambient temperature range	Operating	-40	+85	℃

CAUTION:

[1] Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

[2] Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of XD/XL7660.

5.2. Electrical Specifications

XD/XL7660, V+ = 5V, TA = +25°C, OSC = Free running (see Figure 12, "XD/XL7660 Test Circuit" on page 7 and Figure 13 "XD/XL7660 Test Circuit" on page 7), unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Supply Current (Note 11)	I+	R_L = , +25°C	-	80	160	μA
		-40°C < T_A < +85°C	-	-	180	μA
		-55°C < T_A < +125°C	-	-	200	μA
Supply Voltage Range - High (Note 12)	V^+_H	R_L = 10k, LV Open, T_{MIN} < T_A < T_{MAX}	3.0	-	10	V
Supply Voltage Range - Low	V^+_L	R_L = 10k, LV to GND, T_{MIN} < T_A < T_{MAX}	1.5	-	3.5	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA	-	60	100	
		I_{OUT} = 20mA, -25°C < T_A < +85°C	-	-	120	
		I_{OUT} = 20mA, -55°C < T_A < +125°C	-	-	150	
		I_{OUT} = 3mA, V+ = 2V, LV = GND, -40°C < T_A < +85°C	-	-	300	
		I_{OUT} = 3mA, V+ = 2V, LV = GND, -55°C < T_A < +125°C	-	-	400	
Oscillator Frequency (Note 10)	f_{OSC}	C_{OSC} = 0, Pin 1 Open or GND	5	10	-	kHz
		C_{OSC} = 0, Pin 1 = V+	-	35	-	kHz
Power Efficiency	P_{EFF}	R_L = 5k	96	98	-	%
		T_{MIN} < T_A < T_{MAX} R_L = 5k	95	97	-	-
Voltage Conversion Efficiency	V_{OUTEFF}	R_L =	99	99.9	-	%

Electrical Specifications (continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1	-	M
		V+ = 5V	-	100	-	k
XD/XL7660, V+ = 3V, T_A = 25°C, OSC = Free running, Test Circuit Figure 13, unless otherwise specified						
Supply Current (Note 13)	I+	V+ = 3V, R_L = , +25°C	-	26	100	A
		-40°C < T_A < +85°C	-	-	125	A
Output Source Resistance	R_{OUT}	V+ = 3V, I_{OUT} = 10mA	-	97	150	
		-40°C < T_A < +85°C	-	-	200	
Oscillator Frequency (Note 13)	f_{OSC}	V+ = 3V (same as 5V conditions)	5.0	8	-	kHz
		-40°C < T_A < +85°C	3.0	-	-	kHz

NOTES:

[1] Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

[2] In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, on the order of 5pF.

[3] XD/XL7660 can operate without an external diode over the full temperature and voltage range. This device will function in existing designs that incorporate an external diode with no degradation in overall circuit performance.

[4] Derate linearly above 50°C by 5.5mW/°C.

5.3. Typical Performance Curves

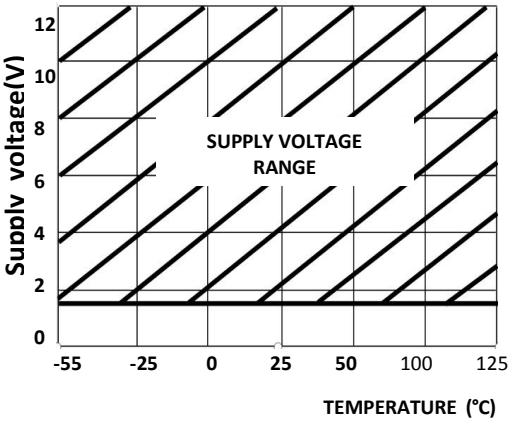


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

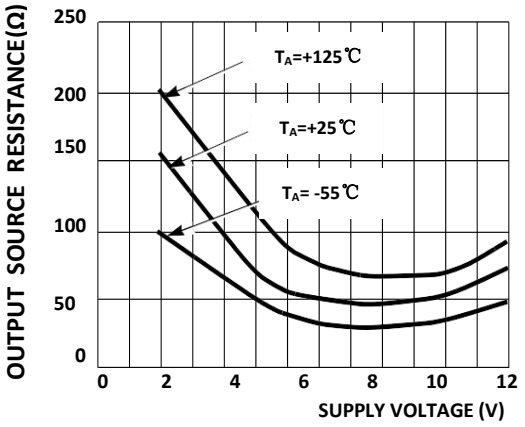


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

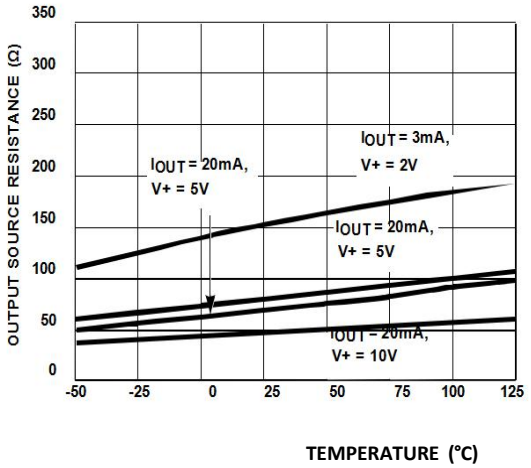


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

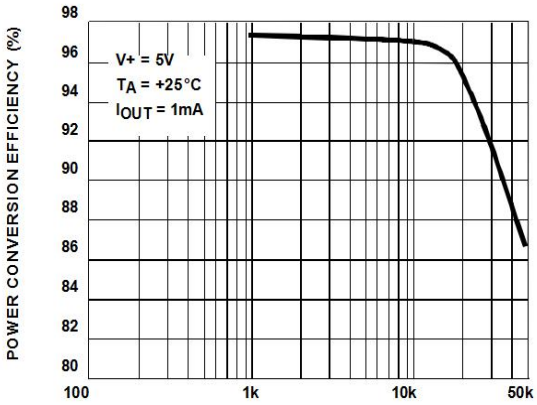


FIGURE 4. POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSCILLATOR FREQUENCY

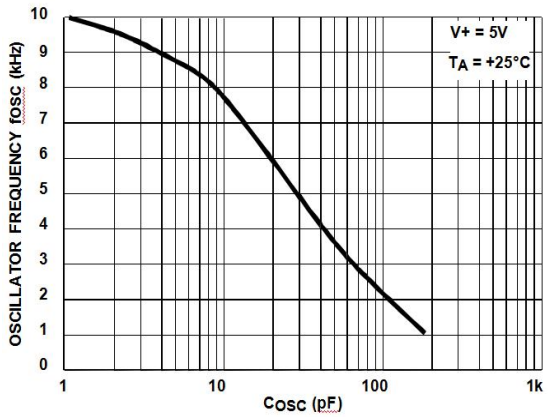


FIGURE 5. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

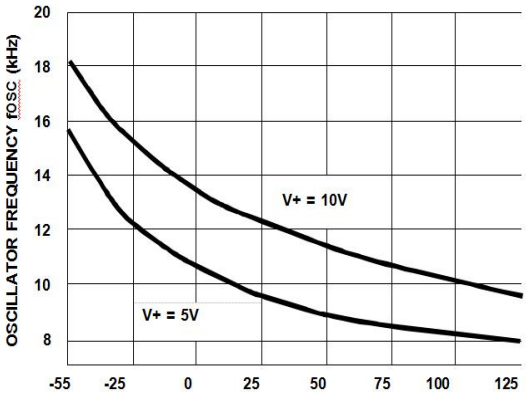


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

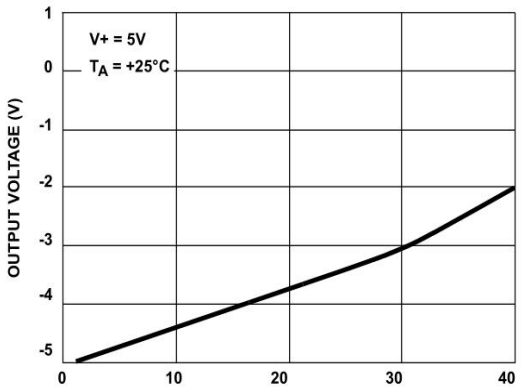


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

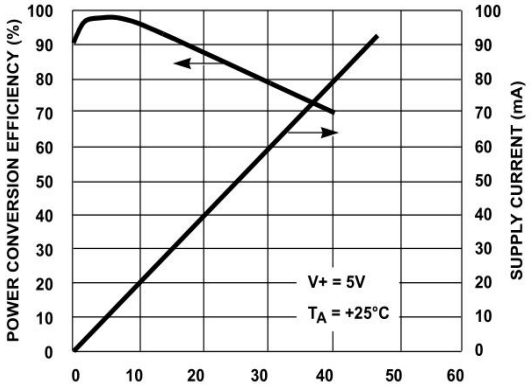


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

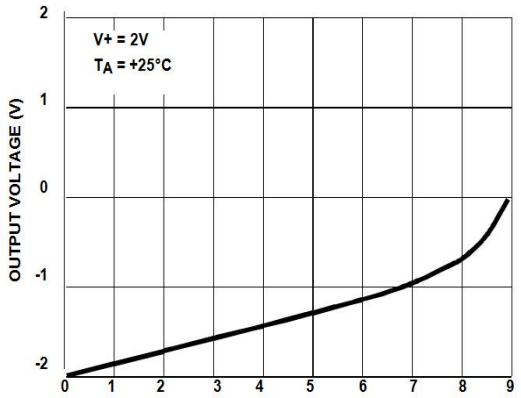


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

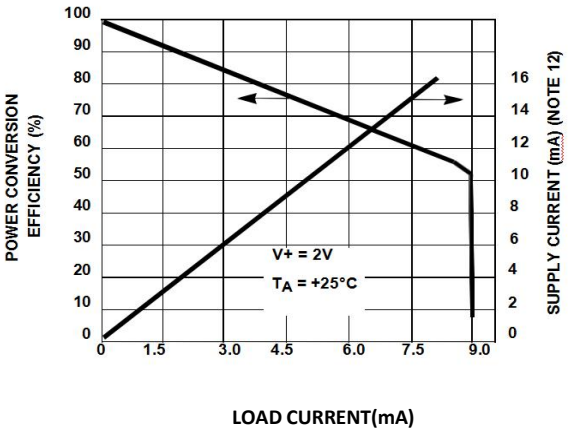


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

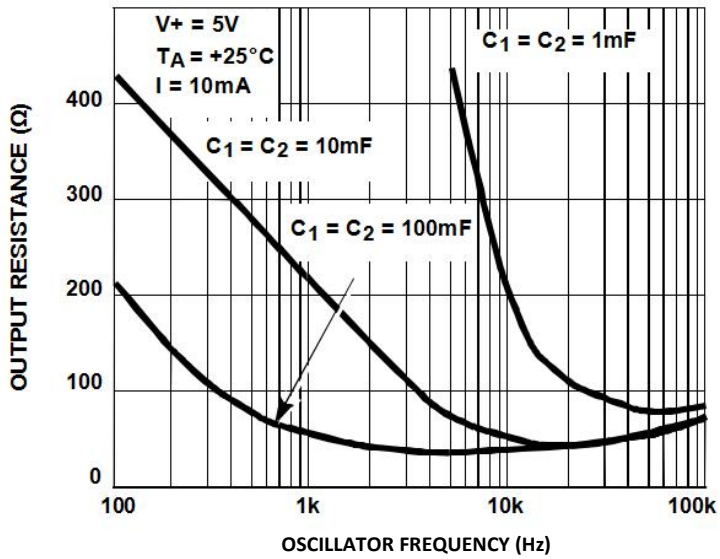


FIGURE 11. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY

NOTE:

These curves include, in the supply current, that current fed directly into the load RL from the V+ (see Figure 12). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the XD/XL7660, goes to the negative side of the load. Ideally, VOUT 2VIN, IS 2IL, so VIN x IS VOUT x IL.

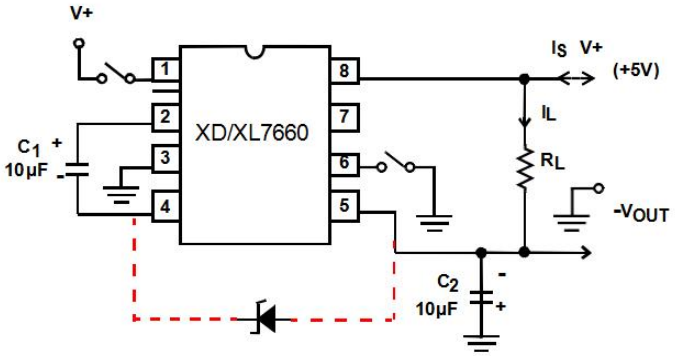


FIGURE 12. XD/XL7660 TEST CIRCUIT

NOTE:

For large values of COSC (>1000pF), the values of C1 and C2 should be increased to 100µF.

6. Detailed Description

The XD/XL7660 contain all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors, which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may best be understood by considering Figure 13, which shows an idealized negative voltage converter.

Capacitor C1 is charged to a voltage, V+, for the half cycle, when switches S1 and S3 are closed. (Note: Switches S2 and S4 are open during this half cycle). During the second half cycle of operation, switches S2 and S4 are closed, with S1 and S3 open, thereby shifting capacitor C1 to C2 such that the voltage on C2 is exactly V+, assuming ideal switches and no load on C2. The XD/XL7660 approach this ideal sit uation more closely than existing non-mechanical circuits.

In the XD/XL7660, the four switches of Figure 13 are MOS power switches; S1 is a P-Channel device; and S2, S3 and S4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S3 and S4 must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON” resistances. In addition, at circuit start-up, and under output short circuit conditions (VOUT = V+), the output voltage must be sensed and the substrate bias adjusted accordingly.

Failure to accomplish this would result in high power losses and probable device latch-up.

This problem is eliminated in the XD/XL7660 by a logic network that senses the output voltage (VOUT) together with the level translators, and switches the substrates of S3 and S4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the XD/XL7660 is an integral part of the anti-latchup circuitry;

however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation, the “LV” pin should be connected to GND, thus disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latchup-proof operation and to prevent device damage.

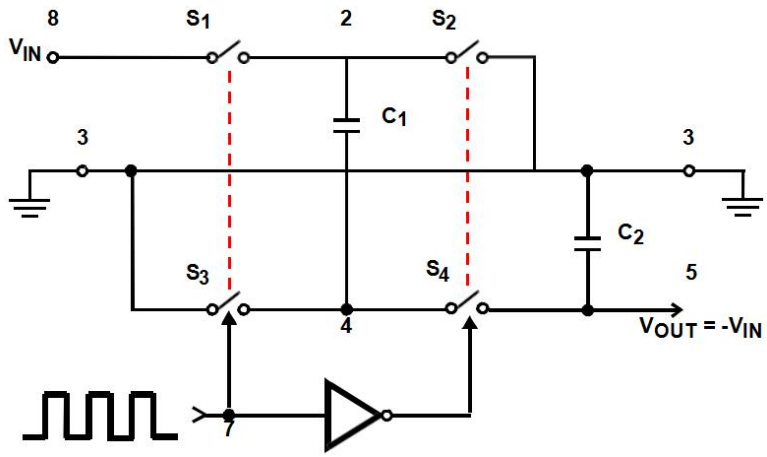


FIGURE 13. IDEALIZED NEGATIVE VOLTAGE CONVERTER

7. Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

[1] The drive circuitry consumes minimal power.

[2] The output switches have extremely low ON resistance and virtually no offset.

[3] The impedance of the pump and reservoir capacitors are negligible at the pump frequency.

The XD/XL7660 approach these conditions for negative voltage conversion if large values of C1 and C2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined as shown in Equation 1:

$$E = \frac{1}{2} C_1 \left(V_1^2 - V_2^2\right) \qquad \text{(EQ. 1)}$$

where V1 and V2 are the voltages on C1 during the pump and transfer cycles. If the impedances of C1 and C2 are relatively high at the pump frequency (see Figure 13) compared to the value of RL, there will be a substantial difference in the voltages, V1 and V2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C1 in order to achieve maximum efficiency of operation.

7.1. Do’ s and Don’ ts

[1] Do not exceed maximum supply voltages.

[2] Do not connect LV terminal to GND for supply voltage greater than 3.5V.

[3] Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.

[4] When using polarized capacitors, the + terminal of C1 must be connected to pin 2 of the XD/XL7660, and the + terminal of C2 must be connected to GND.

[5] If the voltage supply driving the XD/XL7660 has a large source impedance (25 to 30), then a 2.2µF capacitor from pin 8 to ground may be required to limit the rate of rise of input voltage to less than 2V/µs.

[6] If the input voltage is higher than 5V and it has a rise rate more than 2V/µs, an external Schottky diode from VOUT to CAP- is needed to prevent latchup (triggered by

[7] forward biasing Q4’s body diode) by keeping the output (pin 5) from going more positive than CAP- (pin 4).

[8] User should ensure that the output (pin 5) does not go more positive than GND (pin 3). Device latch-up will occur under these conditions. To provide additional protection, a 1N914 or similar diode placed in parallel with C2 will prevent the device from latching up under these conditions, when the load on VOUT creates a path to pull up VOUT before the IC is active (anode pin 5, cathode pin 3).

8. APPLICATION INFORMATION

8.1. Applications

- Simple Conversion of +5V to ±5V Supplies
- Voltage Multiplication VOUT = ±nVIN
- Negative Supplies for Data Acquisition Systems and Instrumentation
- RS232 Power Supplies
- Supply Splitter, VOUT = ±VS

8.2. Typical Applications

The majority of applications will undoubtedly utilize the XD/XL7660 for generation of negative supply voltages.Figure 14 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltage below 3.5V.

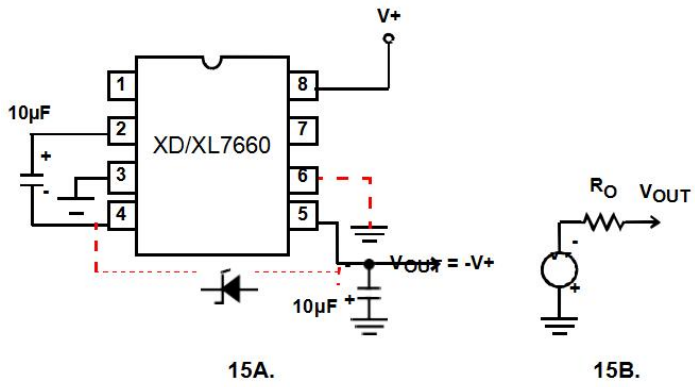


FIGURE 14. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

The output characteristics of the circuit in Figure 15 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 14B. The voltage source has a value of -(V+). The output impedance (RO) is a function of the ON resistance of the internal MOS switches (shown in Figure 13), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for RO is shown in Equation 2：

$$R_0 \cong 2((R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}))\frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

(EQ. 2)

$$f_{PUMP} = \frac{f_{OSC}}{2}$$ (RSWX=MOSFET Switch Resistance)

Combining the four RSWX terms as RSW, we see in Equation 3 that:

$$R_0 \cong 2\times R_{SW1} + \frac{1}{f_{PUMP} \times C_1} + 4\times ESR_{C1} + ESR_{C2} \quad \text{(EQ. 3)}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (see the output source resistance graphs, Figures 2, 3, and 11), typically 23 at +25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the 1/(f_{PUMP} x C1) component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the 1/(f_{PUMP} x C1) term, but may have the side effect of a net increase in output impedance when C1 > 10µF and is not long enough to fully charge the capacitors every cycle. Equation 4 shows a typical application where f_{OSC} = 10kHz and C = C_1 = C_2 = 10µF:

$$R_0 \cong 2\times 23 + \frac{1}{5\times 10^3 \times 10\times 10^6} + 4\times ESR_{C1} + ESR_{C2} \quad \text{(EQ. 4)}$$
$$R_0 \cong 46 + 20 + 5\times ESR_C$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low 1/fPUMP x C1 term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

8.3. System Configuration

ESR also affects the ripple voltage seen at the output. The peak-to-peak output ripple voltage is given by Equation 5:

$$V_{RIPPLE} \cong \left(\frac{1}{2\times f_{PUMP}\times C_2} + 2ESR_{C2}\right)\times I_{OUT} \quad \text{(EQ. 5)}$$

A low ESR capacitor will result in a higher performance output.

8.4. Paralleling Devices

Any number of XD/XL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C2, serves all devices, while each device requires its own pump capacitor, C1. The resultant output resistance is approximated in Equation 6:

$$R_{OUT} = \frac{ROUT(\text{of XD/XL7660})}{n(\text{number of devieces})} \quad \text{(EQ. 6)}$$

8.5. Cascading Devices

The XD/XL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage.However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined as shown in Equation 7:

$$V_{OUT} = -n(VI_N) \qquad \text{(EQ. 7)}$$

Where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual XD/XL7660 ROUT values.

8.6. Changing the XD/XL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods.

By connecting the Boost Pin (Pin 1) to V+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately 3.5 times. The result is a decrease in the output impedance and ripple.

This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, such as 0.1µF, can be used in conjunction with the Boost Pin to achieve similar output currents compared to the device free running with C1 = C2 = 10µF or 100µF. (see Figure 11).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 15. In order to prevent device latchup, a 1k resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10k pull-up resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be one-half of the clock frequency. Output transitions occur on the positive going edge of the clock.

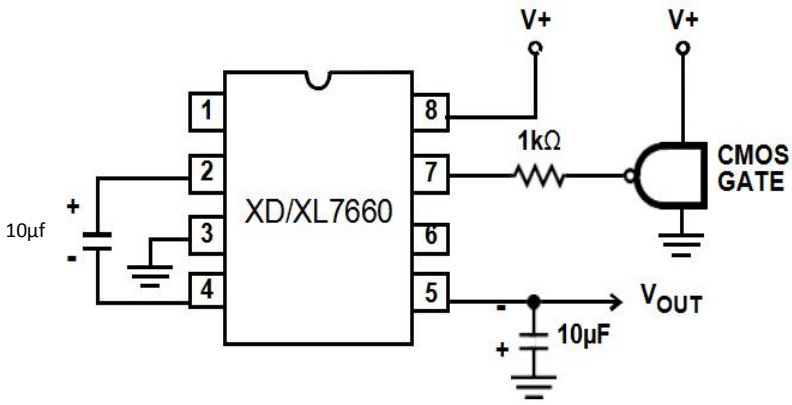


Figure 15. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the XD/XL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 16. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C1) and reservoir (C2) capacitors; this is overcome by increasing the values of C1 and C2 by the same factor by which the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC and V+) will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C1 and C2 (from 10µF to 100µF).

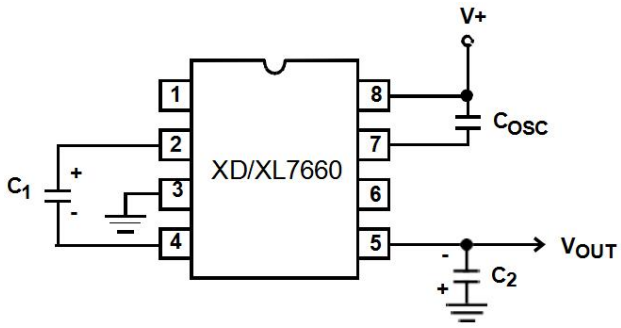


FIGURE 16. LOWERING OSCILLATOR FREQUENCY

8.7. Positive Voltage Doubling

The XD/XL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 17. In this application, the pump inverter switches of the XD/XL7660 are used to charge C1 to a voltage level of V+ -VF, where V+ is the supply voltage and VF is the forward voltage on C1, plus the supply voltage (V+) is applied through diode D2 to capacitor C2. The voltage thus created on C2 becomes (2V+) - (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D1 and D2.

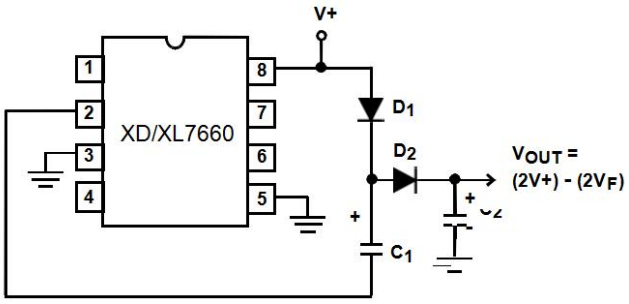


FIGURE 17. POSITIVE VOLTAGE DOUBLER

NOTE: D1 AND D2 CAN BE ANY SUITABLE DIODE.

8.8. Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 18 combines the functions shown in Figure 14 and Figure 17 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be suitable, for example, for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C1 and C3 perform the pump and reservoir functions, respectively, for negative voltage generation, while capacitors C2 and C4 are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher, due to the finite impedance of the common charge pump driver at pin 2 of the device.

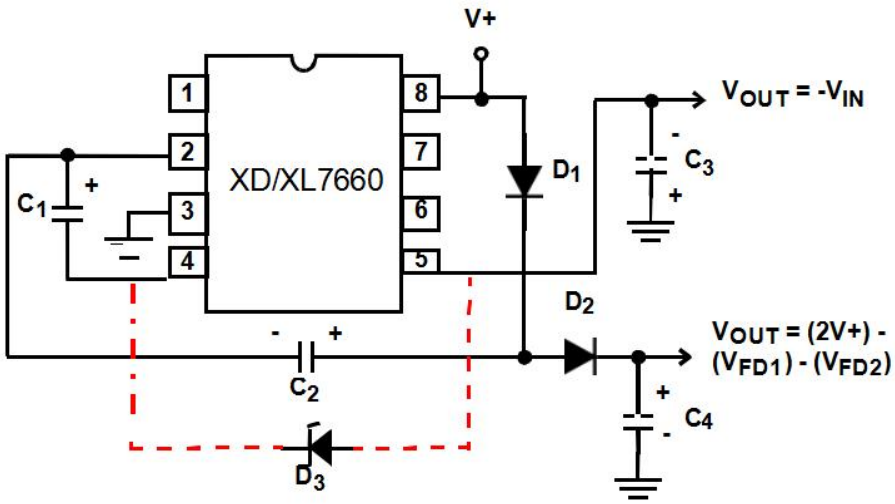


FIGURE 18. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

8.9. Voltage Splitting

The bidirectional characteristics can also be used to split a high supply in half, as shown in Figure 19. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 14, +15V can be converted, via +7.5 and -7.5, to a nominal -15V, although with rather high series output resistance (~250 Ω)

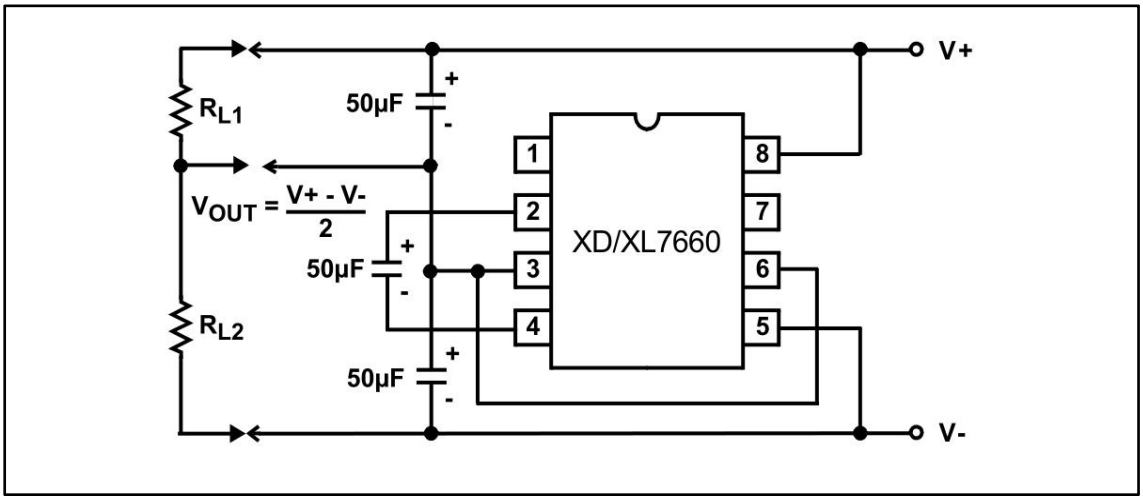


FIGURE 19. SPLITTING A SUPPLY IN HALF

8.10. Regulated Negative Voltage Supply

In some cases, the output impedance of the XD/XL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 20 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable,since the XD/XL7660 output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the XD/XL7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provide an output impedance of less than 5Ω to a load of 10mA.

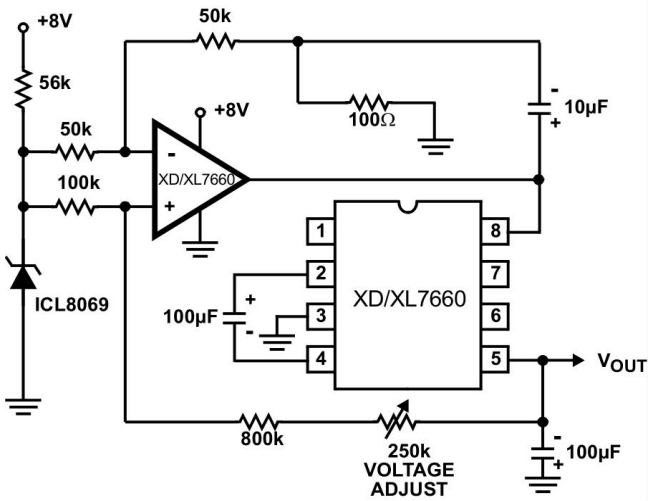


FIGURE 20. REGULATING THE OUTPUT VOLTAGE

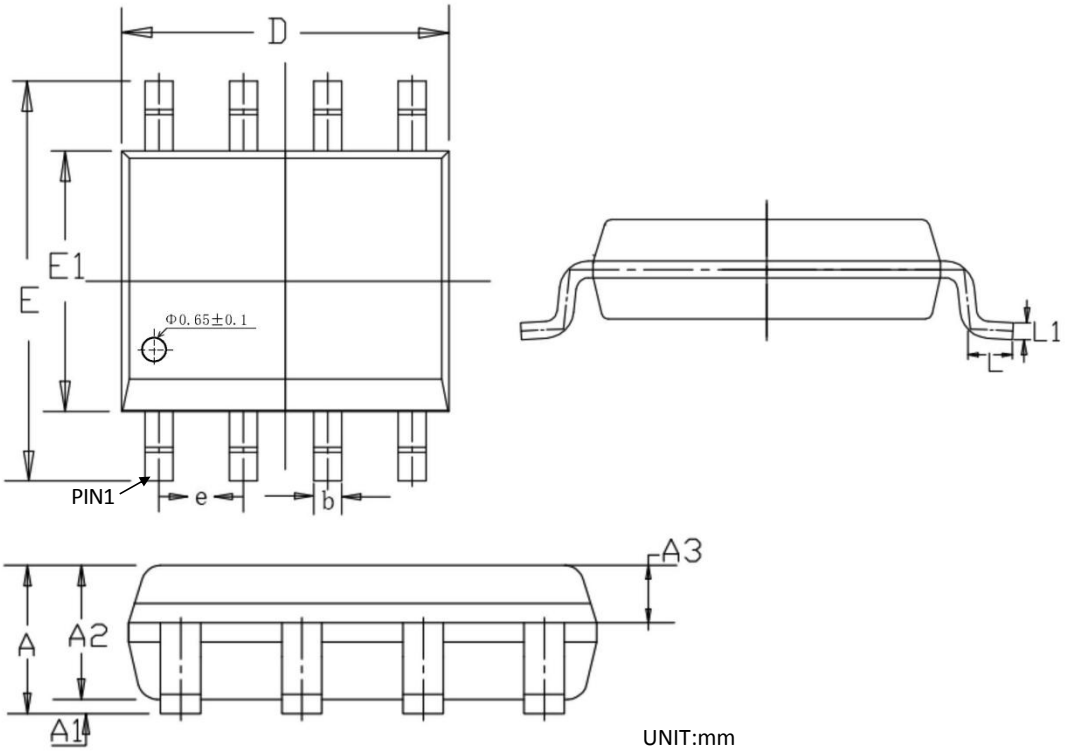
9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL7660	XL7660	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500
XD7660	XD7660	DIP8	9.25 * 6.38	-40 to +85	MSL3	Tube 50	2000

10. DIMENSIONAL DRAWINGS

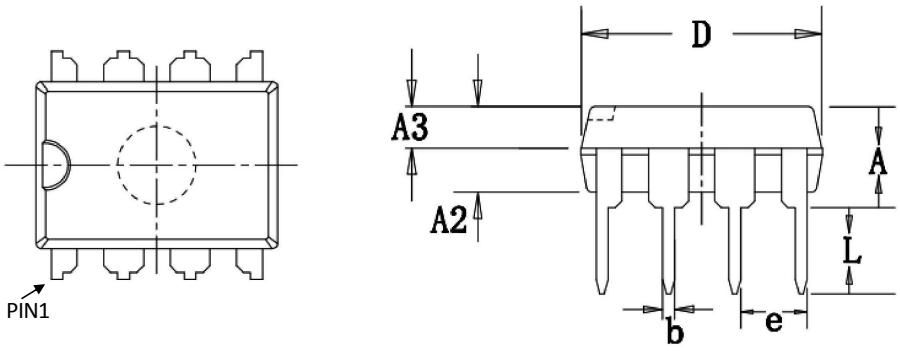
SOP8

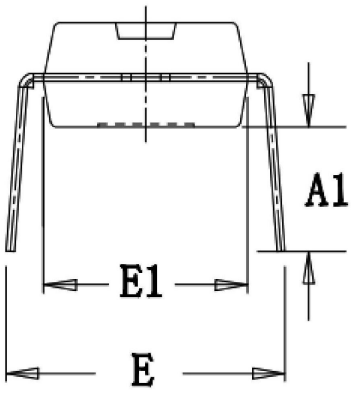


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–