NSA2860
General Sensor Conditioner
Datasheet (EN) 1.4

Product Overview

The NSA2860 is a highly integrated IC for sensor conditioning and transmitting. It can be used for resistive or voltage output sensors like resistive bridge pressure sensor, thermocouple, RTD etc. The NSA2860 integrates a regulator with an external JFET, a 24-bit ADC for primary signal measurement channel, a 24-bit ADC for temperature measurement channel, sensor calibration logic, a pair of programmable current sources and a 16-bit DAC. It can provide digital, 0~5V, 0~10V, 4~20mA, PWM and PDM outputs. With the calibration algorithm built in the internal MCU, the NSA2860 supports to compensate temperature drift of sensor offset and sensitivity up to 2nd order, and non-linearity up to 3rd order.

Key Features

- Low drift voltage reference
- Instrumentation amplifier with programmable gain from 1X to 256X
- 24-bit ADC for primary signal measurement
- 24-bit ADC for temperature measurement
- Internal and external temperature sensor supported
- A pair of programmable current sources
- 16-bit DAC
- 1X~8X digital gain
- Multiple filter settings
- Sensor calibration algorithm embedded in a built-in MCU
- 64 bytes EEPROM
- 4~20mA current loop
- Ratiometric or absolute voltage output
- Specific OWI interface
- SPI/I²C
- PWM/PDM
- High voltage regulator with external JFET or Bipolar
- SSOP16 Package, TSSOP20 Package
- Operation temperature: -40℃~125℃
- RoHS & REACH compliance

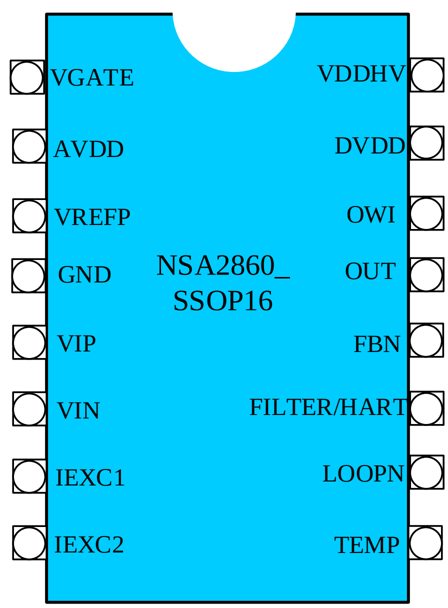
Applications

- Pressure sensor and transmitter
- Thermocouple transmitter
- RTD temperature transmitter

Device Information

Part Number	Package	Body Size
NSA2860_SSOP16	SSOP16	5mm × 6mm
NSA2860_TSSOP	TSSOP20	6.4mm × 6.5mm

Functional Block Diagrams



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1. Pin Configuration and Functions

NSA2860 has two package options: SSOP16 and TSSOP20, the pin configuration is shown as below:

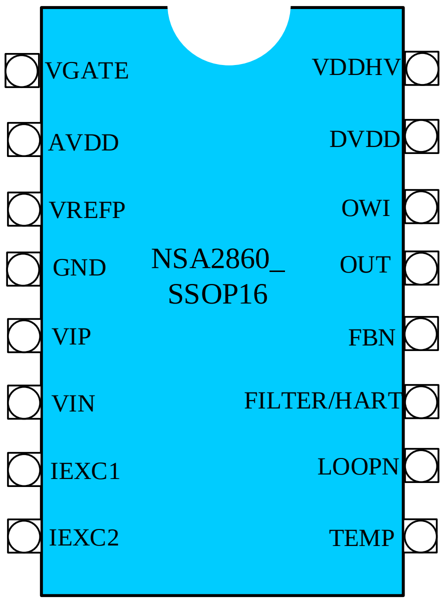


Figure 1.1 SSOP-16 package pin configuration

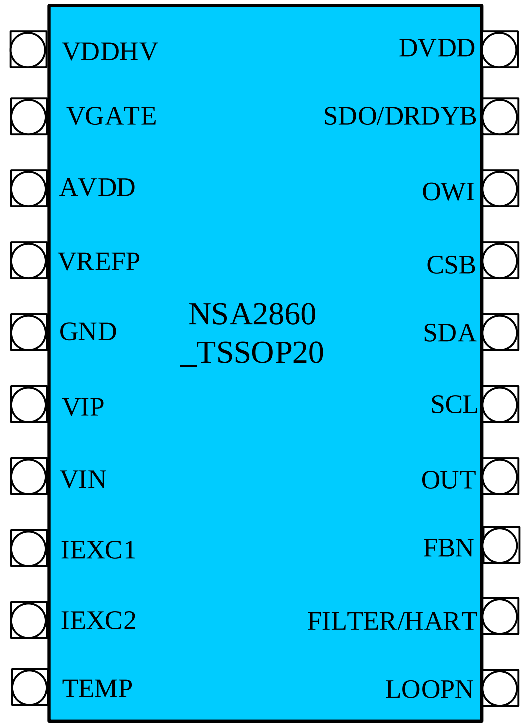


Figure 1.2 TSSOP-20 package pin configuration

Table 1.1 SSOP16 and TSSOP20 Pin Configuration and Description

SSOP16 Pin No.	***TSSOP20 Pin No.***	***Pin Name***	***Type***	***Description***
1	2	VGATE	Analog Output	JFET Regulation Output
2	3	AVDD	Supply	Power Supply
3	4	VREFP	Analog	Reference Voltage Output/Input
4	5	GND	Supply	Ground
5	6	VIP	Analog	Analog input positive
6	7	VIN	Analog	Analog input negative
7	8	IEXC1	Analog	1^{st} constant current source
8	9	IEXC2	Analog	2^{nd} constant current source
9	10	TEMP	Analog	External temperature sensor input (ODR_T ≠ 1111b) External Negative Reference Voltage input (ODR_T = 1111b)
10	11	LOOPN	Analog	Loop negative port
11	12	FILTER/HART	Analog	DAC output filter/HART
12	13	FBN	Analog	Output drive feedback

13	14	OUT	Analog	Driver output pin
14	18	OWI	Digital Input	One-wire interface
15	20	DVDD	Analog	1.8V DVDD digital LDO output
16	1	VDDHV	Supply	Supply with overvoltage/reverse voltage protection
N/A	15	SCL	Digital Input	I²C/SPI clock signal
N/A	16	SDA	Digital I/O	I²C data signal (SDA) or SPI data signal (SDIO)
N/A	17	CSB	Digital Input	I²C/SPI mode selection pin, SPI chip selection
N/A	19	SDO/DRDYB	Digital Input	4-wire SPI date output/data ready interruption

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
VDDHV	$VDDHV_{max}$	-24		28	V	70℃, 1 hour
AVDD	$AVDD_{max}$	-0.3		6.5	V	
Analog Pin Voltage		-0.3		AVDD+0.3	V	
VGATE Pin Voltage	$VGATE_{max}$	-0.3		7.5	V	
LOOPN Pin Voltage	$LOOPN_{max}$	-1.2		0.3	V	
Analog Output Current Limit				25	mA	
Digital Pin Voltage		-0.3		AVDD+0.3	V	25℃
Maximum Junction Temperature	T_j			155	℃	
Storage Temperature		-60		150	℃	
Operation Temperature	T_{A_EXT}	-40		125	℃	Normal temperature range
	T_{A_ADV}	-40		85	℃	Best Performance Temp range
	T_{A_BST}	125		150	℃	Extended temperature range, for 500h max over life time

3. ESD Rating

Ratings		*Value*	*Unit*
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002 Rev E ● All other pins to AVDD/DVDD ● All other pins to GND ● IO pins to IO pins	±2	kV

	Charged device model (CDM), per JESD22-C101F ● All pins	±500	V

4. Electrical Characteristics

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Comments***
Supply and Regulation						
Supply Voltage Range	AVDD	3	5	5.5	V	Supply on AVDD pin
JFET Regulator Output	AVDDJ	4.9	5	5.1	V	JFET_LVL = 0
		3.23	3.3	3.37	V	JFET_LVL = 1
	$PSRR_{AVDDJ}$	100			dB	@DC
		40			dB	@20kHz
DVDD Output	DVDD	1.7	1.8	1.85	V	
Power on Reset	V_{POR_AVDD}		2.5		V	POR threshold during power-up
	V_{POR_HYS}		0.1		V	POR threshold hysteresis
Current (Sensor Not Included)	I_{avdd1}		1.5		mA	4~20mA Transmitter mode (OUT_MODE = 01xb)
	I_{avdd2}		1.65		mA	0~5V voltage output (OUT_MODE = 00xb)
	I_{avdd5}		1.35		mA	Digital output only (OUT_MODE = 111b)
	I_{cmd}		45		µA	COMMAND MODE, SPI/I²C, JFET_DIS = 1
Reference Voltage and Current Source						
Internal Bandgap Reference	V_{BG}	1.119	1.200	1.201	V	Cannot measure directly, proportional with AVDDJ and VREF
VBG TC	V_{BG_TC}		5	20	ppm/℃	-40°C~105℃
VREF (VREFP-VREFN)	V_{REF}		4 or 2.5		V	VREF_DIS = 0
Load on VREF	R_{VREF}	0.5			kohm	
VREF Current Limit	I_{VREF_limit}		20		mA	Short to Ground
Input Current when VREF Driven Externally	I_VREF_EXT	-10		10	nA	VREF_DIS = 1
	IEXC1	0		750	µA	50µA/step

Current Source Outputs with Internal Reference Resistor	IEXC2	0		700	µA	50µA/step, when IEXC2<3:0> ≠ 1111b
External Reference Resistor for Constant Current	R_{IEXC}	20	25	33	kohm	When IEXC2<3:0> = 1111b
IEXC Temperature Drift (Internal Reference Resistor)	I_{EXC_TC}		40	120	ppm/℃	
IEXC1/2 Mismatch				1%		When IEXC1<3:0> = IEXC2<3:0>
$IEXC_{PSRR}$			4		µA/V	IEXC = 350µA
Headroom Voltage for Current Sources		0		AVDD-0.8	V	
IEXC RMS Noise, 0.1~100Hz				5	nA	IEXC = 500µA
Primary Signal Measurement Channel						
PGA Gain	GAIN	1		256		
PGA Gain Error	GAINP_ERR			0.1%		
PGA Gain TC Drift	GAINP_TC		3		ppm/℃	
Offset	OFF			600/GAIN	µV	Input referred, SYSTEM_CHOP_EN = 0
				1	µV	Input referred, SYSTEM_CHOP_EN = 1
Offset TC	OFF_DRIFT		±5		nV/℃	Input referred, SYSTEM_CHOP_EN = 1
PADC Resolution	RES_{RAW}		24		Bits	
PADC Output Data Rate	ODR_P	2.5		2400	Hz	
ENOB of Primary Channel	ENOB_P	Refer to Table 6.1			Bits	Depend on PGAIN and ODR_P
Integral Nonlinearity	INL			15	ppm of FS	
Input CMRR of Primary Channel	CMRR		120		dB	
PSRR of Primary Channel	PSRR	90	120		dB	
Temperature Measurement Channel (Internal and External Temperature Sensor)						

TADC Resolution	RES_T		24		Bit	
TADC Gain	GAIN_T	1		4		1, 2, 4
TADC Output Data Rate	ODR_T	2.5		2400	Hz	
TADC ENOB	ENOB_T		Refer to Table 6.2, 6.3			
Error of Internal Temperature Sensor			±1.5	±3	℃	-40~125 ℃
TEMP Input Impedance			1		Gohm	
Analog Input Pins						
Analog Input Voltage	VIP, VIN	GND+0.4		AVDD-1.2	V	PGA on (Gain>2)
		GND+0.1		AVDD-0.1	V	PGA off, Buffer on
		GND-0.1		AVDD+0.1	V	PGA off, Buffer off
Differential Input Voltage Range (VIP-VIN)	V_{range}		±VREF /GAIN		V	VREF: ADC Reference Voltage
VINP, VINN Input Pins Leakage Current	$I_{leakage}$			±1	nA	DIAG_ON = 0
DAC and Output Buffer						
DAC Resolution			16		Bit	
DAC Full Scale	VFSDAC		5V, 3.3V, 1.2V or AVDD			Depend on DAC_REF<1:0>
DNL of DAC	DNL			1	LSB	
INL of DAC	INL			10	LSB	
DAC Output RMS Noise	V_{rms}		0.5		mV	0~5V Absolute Voltage Output Mode
Output Load Resistance	R_{load}	1			kohm	Voltage Output Mode
Output Load Capacitance	C_{load}			150	nF	Voltage Output Mode
Output Shorted Current Limit	I_{short_lmt}	10		25	mA	Output Short to VDD or GND
Clamp High Level	V_{clamph}	0.5		1	VFSDAC	Set by CLAMP_HIGH<7:0>
Clamp Low Level	V_{clampl}	0		0.5	VFSDAC	Set by CLAMP_LOW<7:0>

4~20mA Current Loop						
Loop Reference Resistor	R_{loop}		50		ohm	
Loop Current Noise	I_{rms}		0.2		µA	0.1Hz~10Hz
Downscale Alarm Current	I_{faulth}		3.375		mA	
Upscale Alarm Current	I_{faultl}		21.75		mA	
Diagnostic and Alarm						
Burnout Current	I_{diag}		100		nA	
Fault Alarm High	FAULT_HIGH	98%			VDD	
Fault Alarm Low	FAULT_LOW			2%	VDD	
OSC						
ADC Clock	FOSC_MOD		614.4		kHz	
Clock Rate Error	FOSC_ERR	-1%		1%		-40~125℃
PDM/PWM						
PDM Modulation Frequency	F_{PDM}	19.2		153.6	kHz	
PWM Frequency	F_{PWM}		300		Hz	
PWM Resolution	R_{PWM}		12		Bit	
EEPROM						
Programming Temperature	T_{EEP}	-40		105	℃	
Programming Supply Voltage	V_{EEP}	4.5		5.5	V	
Time for EEPROM Programming	T_{EEP}		0.8		s	
Endurance			10		k	
Date Retention		10			A	@150℃
Serial Interface						
Communication Data Rate	F_{sclk}			10	MHz	SPI Interface
				400	kHz	I²C Interface
				50	kHz	OWI Interface

5. Register Description

The register map of the NSA2860 includes two parts, normal registers and EEPROM registers. The normal registers include data registers and some control registers, while the EEPROM registers are mainly configuration registers and calibration coefficients. All EEPROM registers should be written by external interface on command mode (register ‘CMD’ = ‘0x00’).

5.1. Normal Registers

IF_CTRL (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x00	7, 0	SDO_ACTIVE	1’b1 1’b1	Set either of these two bits to: 0: SPI3-wire; 1: SPI4-wire (SDO as serial output)
	6, 1	LSB_FIRST	1’b0 1’b0	Set either of these two bits to: 0: SPI MSB first; 1: SPI LSB first
	5, 2	SOFTRESET	1’b0 1’b0	Set either of these two bits to 1 to reset the chip. Return to 0 after reset.

STATUS (Read Only)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x02	7 – 3	ERROR_CODE<4:0>	5’b00000	Bit6=1: VIP open or short to VREF; Bit5=1: VIP short to GND; Bit4=1: VIN open or short to VREF; Bit3=1: VIN short to GND.
	2	CRC_ERR	1’b0	1: CRC error detected during EEPROM loading; When CRC error is asserted, EEPROM register bits ‘OWI_DIS’, ‘OWI_AC_EN’, ‘OWI_WINDOW’, ‘JFET_DIS’, ‘VREF_DIS’, ‘EEPROM_LOCK’ are forced to 0.
	1	LOADING_END	1’b0	1: EEPROM loading end flag
	0	DRDY	1’b0	1: Set after a new data updated and automatically cleared after a register reading to PDATA/TDATA or before the next data's coming.

PDATA (Read Only, Primary Channel Data Register)

Address	*Bit*	*Register Name*	*Default*	*Description*
0x06	7 – 0	PDATA<23:16>	0x00	Signed, 2’s complement: When ‘RAW_P’ = 1, store the ADC output of primary channel; When ‘RAW_P’ = 0, store the calibrated primary channel data.
0x07	7 – 0	PDATA<15:8>	0x00	
0x08	7 – 0	PDATA<7:0>	0x00	

TDATA (Read Only, Temperature Channel Data Register)

Address	*Bit*	*Register Name*	*Default*	*Description*

0x09	7 – 0	TDATA<23:16>	0x00	Signed, 2's complement: When 'RAW_T' = 1, store the ADC output of temperature channel; When 'RAW_T' = 0, store the calibrated temperature data, LSB = 1/2^16℃. Real Temperature = TDATA/2^16+25 ℃
0x0a	7 – 0	TDATA<15:8>	0x00	
0x0b	7 – 0	TDATA<7:0>	0x00	

DAC_DATA (R/W, DAC Input Data Register)

Address	Bit	Register Name	Default	Description
0x12	7 – 0	DAC_DATA<15:8>	0x00	DAC input data, unsigned; When 'RAW_P' = 0, set by the internal calibration logic, read only, When 'DAC_BLANK'= 1 and 'RAW_P' = 1, set externally through serial interface.
0x13	7 – 0	DAC_DATA<7:0>	0x00	
0x14	0	DAC_BLANK	1'b0	Blank DAC input update when 'RAW_P' = 1, should be set before writing DAC_MSB and DAC_LSB and cleared after the writing is finished.

COMMAND (R/W, Command Register)

Address	Bit	Register Name	Default	Description
0x30	7 – 0	CMD<7:0>	0x03	0x00: Command mode, all EEPROM can be written only in command mode; 0x01/0x02: Reserved; 0x03: Active mode; 0x33: Enter EEPROM Program Mode

QUIT_OWI (Write Only)

Address	Bit	Register Name	Default	Description
0x61	7 – 0	QUIT_OWI<7:0>	0x00	Write '0x5D' to this register to quit OWI communication. If 'QUIT_OWI_CNT' = 0x00, quit OWI communication permanently; If 'QUIT_OWI_CNT' is not 0x00, quit OWI mode temporarily for some certain time and then get back to OWI mode.

QUIT_OWI_CNT (R/W)

Address	Bit	Register Name	Default	Description
0x62	7 – 0	QUIT_OWI_CNT<7:0>	0x00	Time for temporarily quit OWI communication Mode. 0x00: Quit forever, 0x01: 50ms, 0x02: 100ms … 0xFF: 12.8s

EE_PROG (R/W)

Address	Bit	Register Name	Default	Description
0x6a	7 – 0	EE_PROG<7:0>	0x00	Write '1E' to this register to start EEPROM Programming. Automatically cleared to '0x00' after programming is finished.

VDD_CHECK (R/W)

Address	Bit	Register Name	Default	Description
0x70	0	VDD_CHECK	1'b0	Write '1' to force AVDD/2 as the input of temperature ADC

5.2. EEPROM Registers

SYS_CONFIG1 (R/W)

Address	Bit	Register Name	Default	Description
0xa1	7	CAL_MODE	1'b0	0: One segment calibration with the 2nd order temperature coefficients; 1: Two segment calibration with the 1st order temperature coefficients
	6	BURNOUT_EN	1'b0	1: Enable the 100nA burnout current sources and diagnosis
	5	FAULT_ON	1'b0	1: When any fault is detected, pull analog output to a fixed level of voltage or loop current.
	4	FAULT_LVL	1'b0	0: Low alarm output (voltage output), 3.375mA (current output); 1: High alarm output (voltage output), 21.75mA (current output)
	3	OWI_AC_EN	1'b0	0: Single-port OWI communication mode; 1: Dual-port OWI communication mode
	2	OWI_WINDOW	1'b0	0: OWI can be entered during a 10ms~80ms window after powering up or soft reset; 1: Infinite window, OWI can be entered any time after powering up
	1	OWI_DIS	1'b0	1: OWI disabled (won't be effective until next power on reset or soft reset after EEPROM is programmed)
	0	INT_EN	1'b0	1: Enable data ready interruption (through SDO/DRYB pin, active low)

SYS_CONFIG2 (R/W)

Address	Bit	Register Name	Default	Description
0xa2	7	JFET_DIS	1'b0	1: Disable JFET regulator
	6	JFET_LVL	1'b0	0: JFET regulator outputs 5V 1: JFET regulator outputs 3.3V
	5	VREF_DIS	1'b0	1: Disable reference buffer, and reference voltage can be forced externally
	4	VREF_LVL	1'b0	0: VREFP = 4V; 1: VREFP = 2.5V
	3	T_OUT_EN	1'b0	1: When not in OWI mode, TADC data outputs through OWI pin in PWM format
	2 - 0	OUT_MODE<2:0>	3'b000	000: Voltage output;

				001: Reserved, should not be used; 010/011: Current loop output; 100: PDM output; 101: PWM output; 110: Reserved, should not be used; 111: Disable DAC

Current_EXC (R/W)

Address	Bit	Register Name	Default	Description
0xa3	7 – 4	IEXC1<3:0>	4'b0000	IEXC1/2: Set IEXC1 and IEXC2 current value or mode; 0000: Disabled; 0001: 50µA; 0010: 100µA; … 1110: 700µA; 1111 for IEXC1: 750µA; 1111 for IEXC2: Use external reference resistor
	3 – 0	IEXC2<3:0>	4'b0000	

PCH_Config1 (R/W)

Address	Bit	Register Name	Default	Description
0xa4	7 – 4	GAIN_P<3:0>	4'b0000	Primary Channel Gain 0000: 1X, 0001: 2X, 0010: 4X, 0011: 6X, 0100: 8X, 0101: 12X, 0110: 16X, 0111: 24X, 1000: 32X, 1001: 48X, 1010: 64X, 1011: 96X, 1100: 128X, 1101: 192X, 1110: 256X, 1111: 1X and disable buffer.
	3 – 0	ODR_P<3:0>	4'b0000	PADC output data rate setting 0000: 2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101: 75Hz, 0110: 37.5Hz, 0111: 18.75Hz, 1000: 10Hz (with 60Hz notch), 1001: 10Hz (with 50Hz notch), 1010: 5Hz (with 60Hz notch), 1011: 5Hz (with 50Hz notch), 1100: 2.5Hz (with 60Hz notch), 1101: 2.5Hz (with 50Hz notch), 1110, 1111: PADC disabled.

PCH_Config2 (R/W)

Address	Bit	Register Name	Default	Description
0xa5	7 – 6	DAC_REF<1:0>	2'b00	DAC full scale reference 00: 5V, 01: 3.3V, 10: 1.2V, 11: AVDD (ratiometric output)
	5 – 3	Reserved<2:0>	3'b000	Should be 3'b000
	2	SYS_CHOP_EN	1'b0	0: Disable system chopping; 1: Enable system chopping
	1	INPUT_SWAP	1'b0	1: Swap the polarity of inputs of PADC
	0	RAW_P	1'b0	0: Update calibrated sensor data into 'PDATA' register. 'DAC_DATA' will be set by internal calibration logic;

				1: Update raw primary ADC data into 'PDATA' register after conversion, and allow DAC to be set externally

TCH_Config (R/W)

Address	Bit	Register Name	Default	Description
0xa6	7	EXT_TEMP	1'b0	0: Internal temperature sensor selected; 1: External temperature sensor selected (TEMP pin as external temperature sensor input)
	6 – 5	GAIN_T<1:0>	2'b00	Gain for temperature channel (external temperature sensors only) 00: 1X, 01: 2X, 10/10: 4X
	4 – 1	ODR_T	4'b0000	TADC output data rate, similar as ODR_P 0000: 2.4kHz, 0001: 1.2kHz, 0010: 600Hz, 0011: 300Hz, 0100: 150Hz, 0101: 75Hz, 0110: 37.5Hz, 0111: 18.75Hz, 1000: 10Hz (with 60Hz notch), 1001: 10Hz (with 50Hz notch), 1010: 5Hz (with 60Hz notch), 1011: 5Hz (with 50Hz notch), 1100: 2.5Hz (with 60Hz notch), 1101: 2.5Hz (with 50Hz notch), 1110, 1111: TADC disabled When TADC is disabled, the negative reference voltage (VREFN) for PADC is driven externally through TEMP pin.
	0	RAW_T	1'b0	0: Store the calibrated TADC data into 'TDATA' register; 1: Store the direct TADC output into 'TDATA' register

CLAMPH (R/W)

Address	Bit	Register Name	Default	Description
0xa7	7 – 0	CLAMPH<7:0>	0x00	Set clamping high level, (1- CLAMPH *2^ (-9)) * VFSDAC

CLAMPL (R/W)

Address	Bit	Register Name	Default	Description
0xa8	7 – 0	CLAMPL<7:0>	0x00	Set clamping low level, CLAMPL *2^ (-9) * VFSDAC

OFFSET0 (R/W)

Address	Bit	Register Name	Default	Description
0xa9	7 – 0	OFF0<15:8>	0x00	Sensor calibration coefficient, offset at T0. LSB = 1/2^15, RANGE (-1, +1)
0xaa	7 – 0	OFF0<7:0>	0x00	

CTC1 (R/W)

Address	Bit	Register Name	Default	Description
0xab	7 – 0	CTC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1st order temperature coefficient of offset. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1st order temperature coefficient of offset for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xac	7 – 0	CTC1<7:0>	0x00	

CTC2 (R/W)

Address	Bit	Register Name	Default	Description
0xad	7 – 0	CTC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2^{nd} order temperature coefficient of offset. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1^{st} order temperature coefficient of offset for segment 1. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xae	7 – 0	CTC2<7:0>	0x00	

S0 (R/W)

Address	Bit	Register Name	Default	Description
0xaf	7 – 0	S0<15:8>	0x00	Sensor calibration coefficient, sensitivity at T0. LSB = 1/2^15 (unsigned), RANGE (0, 2)
0xb0	7 – 0	S0<7:0>	0x00	

STC1 (R/W)

Address	Bit	Register Name	Default	Description
0xb1	7 – 0	STC1<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 1^{st} order temperature coefficient of sensitivity. LSB = 1/2^22, RANGE (-0.00781, +0.00781); CAL_MODE = 1: the 1^{st} order temperature coefficient of sensitivity for segment 0. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xb2	7 – 0	STC1<7:0>	0x00	

STC2 (R/W)

Address	Bit	Register Name	Default	Description
0xb3	7 – 0	STC2<15:8>	0x00	Sensor calibration coefficient, CAL_MODE = 0: the 2^{nd} order temperature coefficient of sensitivity. LSB = 1/2^29, RANGE (-6.1e-5, 6.1e-5); CAL_MODE = 1: the 1^{st} order temperature coefficient of sensitivity for segment 1. LSB = 1/2^22, RANGE (-0.00781, +0.00781)
0xb4	7 – 0	STC2<7:0>	0x00	

KS (R/W)

Address	Bit	Register Name	Default	Description
0xb5	7 – 0	KS<15:8>	0x00	Sensor calibration coefficient, the 2^{nd} order nonlinearity coefficient. LSB = 1/2^15, RANGE (-1, +1)
0xb6	7 – 0	KS<7:0>	0x00	

KSS (R/W)

Address	Bit	Register Name	Default	Description
0xb7	7 – 0	KSS<15:8>	0x00	Sensor calibration coefficient, the 3rd order nonlinearity coefficient. LSB = 1/2^16, RANGE (-0.5, +0.5)
0xb8	7 – 0	KSS<7:0>	0x00	

SCALE_OFF (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xb9	7 – 0	SCALE_OFF<23:16>	0x00	SCALE offset coefficient, LSB = 1/2^23, RANGE (-1, +1)
0xba	7 – 0	SCALE_OFF<15:8>	0x00	
0xbb	7 – 0	SCALE_OFF<7:0>	0x00	

SCALE_S (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xbc	7 – 0	SCALE_S<23:16>	0x00	SCALE sensitivity coefficient (unsigned), LSB = 1/2^16 (unsigned), RANGE (0, 256)
0xbd	7 – 0	SCALE_S<15:8>	0x00	
0xbe	7 – 0	SCALE_S<7:0>	0x00	

T0 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xbf	7 – 0	T0<7:0>	0x00	Temperature sensor calibration coefficient, reference temperature point. Real reference temperature: REAL_T0 = T0+25. LSB = 1, RANGE (-128, +127)

KTS (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc0	7 – 0	KTS<7:0>	0x00	Temperature sensor calibration coefficient, the 2nd order nonlinearity coefficient for external temperature sensor. LSB = 1/2^7, RANGE (-1, +1)

MTO (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc1	7 – 0	MTO<15:8>	0x00	Temperature sensor calibration coefficient, offset coefficient of external temperature sensor. MTO: LSB = 1/2^15, RANGE (-1, +1)
0xc2	7 – 0	MTO<15:8>	0x00	

KT (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc3	7 – 0	KT<15:8>	0x00	Temperature sensor calibration coefficient, sensitivity coefficient of external temperature sensor. KT: LSB = 1/2^12, RANGE (-8, +8)
0xc4	7 – 0	KT<15:8>	0x00	

DAC_OFF (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc5	7 – 0	DAC_OFF<15:8>	0x00	DAC calibration coefficient, DAC offset. LSB = 1/2^15, RANGE (-1, +1)
0xc6	7 – 0	DAC_OFF<7:0>	0x00	

DAC_GAIN (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc7	7 – 0	DAC_GAIN<15:8>	0x00	DAC calibration coefficient, DAC gain coefficient. LSB = 1/2^16, RANGE (-0.5, +0.5)
0xc8	7 – 0	DAC_GAIN<7:0>	0x00	

PADC_OFF (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xc9	7 – 0	PADC_OFF<23:16>	0x00	PADC calibration coefficient, PADC offset. LSB = 1/2^23, RANGE (-1, +1)
0xca	7 – 0	PADC_OFF<15:8>	0x00	
0xcb	7 – 0	PADC_OFF<7:0>	0x00	

PADC_GAIN (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xcc	7 – 0	PADC_GAIN<15:8>	0x00	PADC calibration coefficient, PADC gain. LSB = 1/2^16, RANGE (-0.5, +0.5)
0xcd	7 – 0	PADC_GAIN<7:0>	0x00	

P0 (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xce	7 – 0	P0 <7:0>	0x00	Sensor calibration coefficient, reference pressure point for nonlinearity calibration. LSB = 1/2^7, RANGE (-1, 1)

SPARE (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xcf	7 – 0	SPARE1<7:0>	0x00	SPARE Register 1
0xd0	7 – 0	SPARE2<7:0>	0x00	SPARE Register 2
0xd1	7 – 0	SPARE3<7:0>	0x00	SPARE Register 3
0xd2	7 – 0	SPARE4<7:0>	0x00	SPARE Register 4
0xd3	7 – 0	SPARE5<7:0>	0x00	SPARE Register 5
0xd4	7 – 0	SPARE6<7:0>	0x00	SPARE Register 6
0xd5	7 – 0	SPARE7<7:0>	0x00	SPARE Register 7
0xd6	7 – 0	SPARE8<7:0>	0x00	SPARE Register 8

PDM_FREQ (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd7	7 – 6	DIG_GAIN<1;0>	2'b00	ADC digital gain 00: 1X, 01: 2X, 10: 4X, 11: 8X
	5 – 4	PDM_FREQ<1:0>	2'b00	PDM modulation frequency

				00: 19.2kHz, 01: 38.4kHz, 10: 76.8kHz, 11: 153.6kHz
	3 – 0	Reserved	2’b00	

RESERVED

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd8	7 – 0	RESERVED	-	NOVOSENSE Information, customer should not erase these bits

EEPROM_LOCK (R/W)

Address	*Bit*	*Register Name*	*Default*	*Description*
0xd9	7	EEPROM_LOCK	1’b0	1: EEPROM lock, set 1 and then EEPROM can’t be programmed (won’t be effective until next power on reset or soft reset after EEPROM is programmed).
	6 – 0	PartID (read only)	7’b0000001	NOVOSENSE chip ID, customer should not erase these bits

6. Function Description

6.1. Overview

The NSA2860 is a highly integrated sensor conditioner for voltage output sensors like Wheatstone bridge pressure sensor, thermocouple and RTD. The chip consists of five parts: the analog front-end module, the digital module, the analog output module, the power supply module and the serial interface. The block diagram of the NSA2860 is shown in Figure 6.1.

The analog front-end module includes a primary signal measurement channel with an instrumentation amplifier followed by a 24-bit ∑Δ ADC, a temperature measurement channel also with a 24-bit ∑Δ ADC, for precise sensor signal measurement.

The digital module is composed of registers, EEPROM, control logic, and built-in MCU. The sensor calibration algorithm is implemented with the built-in MCU and can supports up to 2^{nd} order temperature drift compensation of offset and sensitivity for the sensor. It can also compensate the nonlinearity of sensor output up to 3^{rd} order. The configuration parameters and coefficients for calibration are stored in the EEPROM of 64 bytes.

The analog output module includes a 16-bit DAC and a flexible configurable output driver which can be configured to support several voltage output modes, 4~20mA current loop mode, PDM output and PWM output. The power supply module includes a sensor voltage driver, a pair of current sources and a high-voltage JFET regulator. The NSA2860 supports three serial interfaces: SPI, I^2C and OWI, writing and reading registers of configuration, calibration coefficients and data.

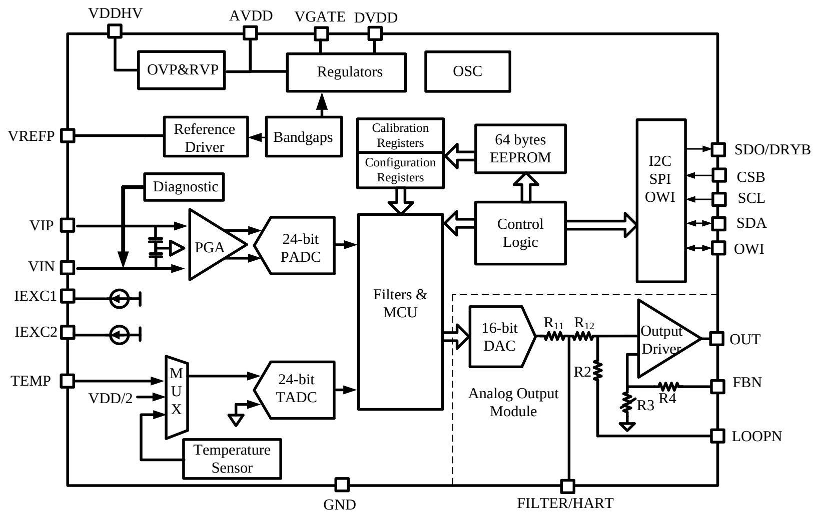


Figure 6.1 Block diagram of the NSA2860

6.2. Analog Front-End Module 1: Primary Signal Channel

The primary signal measurement channel includes an instrumentation PGA, and a 24-bit sigma-delta ADC (PADC) followed by digital filters.

6.2.1. PGA+ADC

The PGA is a gain programmable instrumental amplifier, which can be configured to 1X, 2X, 4X, 6X, 8X, 16X, 24X, 32X, 48X, 64X, 96X, 128X, 192X, 256X. The NSA2860 has a built-in RFI filter for RFI-immunity enhancement.

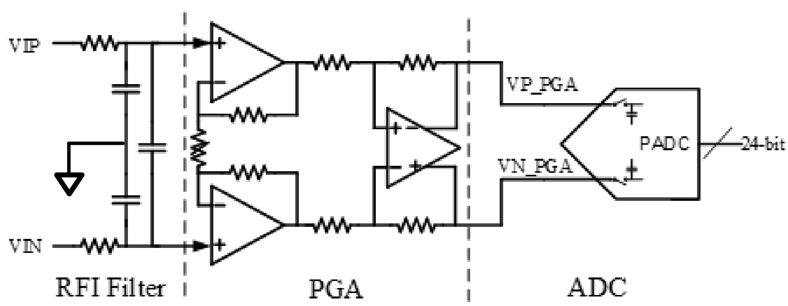


Figure 6.2 Primary signal channel (PGA+ADC)

The PADC performs analog-to-digital conversion. The output of the ADC is digitally filtered with 24-bit resolution. The reference voltage of the ADC is VREF, and the allowable differential input range is ±VREF/GAIN_P. The PADC output can be expressed by the following equation:

$$PDATA_{RAW} = \frac{VIP - VIN}{VREF} * GAIN\_P * 2^{23}$$

$PDATA_{RAW}$ can be read out from 'PDATA' registers (Reg0x06-Reg0x08) only when 'RAW_P' is set to 1; otherwise, the built-in MCU calibrates the sensor using the calibration coefficients and temperature data stored in 'TDATA' and puts the calibrated digital output of the primary channel onto the 'PDATA' registers.

6.2.2. The Input Common-Mode Voltage of PGA

The PGA is of differential input and differential output. The output voltages of the PGA can be expressed as:

$$VP\_PGA = VCMin + GAIN\_P * VDin/2$$

$$VN\_PGA = VCMin - GAIN\_P * VDin/2$$

VCMin and VDin in the formula are common-mode voltage and differential voltage of the PGA input voltage. To avoid the saturation of the amplifiers, both VP_PGA and VN_PGA should meet the following limitation:

$$\mathrm{AGND} + 0.1\mathrm{V} < \mathrm{VP(N)}_{\mathrm{PGA}} < \mathrm{AVDD} - 0.1\mathrm{V}$$

From above, the input common-mode voltage should satisfy the following limitation:

$$AGND + 0.1V + GAIN\_P * VDin(max)/2 < VCMin < AVDD - 0.1V - GAIN\_P * VDin(max)/2$$

Besides, the input of the PGA amplifiers is PMOS transistor, so the PGA input should meet:

$$VIP(N) < AVDD \ - 1V$$

For voltage-driven bridge sensors, the common-mode voltage of its output is usually close to VREF/2. One can easily meet the limitation by choosing a proper 'GAIN_P' and make VDin (max) <0.8*VREF/GAIN_P. '0.8' here is considered to give some margin for the sensor sensitivity and the amplifier voltage swing. For current-driven sensors, more careful settings are needed to maximize the dynamic range of the PADC.

6.2.3. Digital Filter

The bandwidth and output data rate (ODR) of the digital filter can be set by 'ODR_P'. ODR can be set from 2.4 kHz to 2.5 Hz. The lower ODR, the lower noise the PADC output will have, at the cost of slower time response. Table 6.1 shows the effective number of bits (ENOB) of the PADC output with different ODR_P settings. The relationship between ENOB and RMS noise is:

$$ENOB_{RMS} = 24 - log_2(RMS_{ADC})$$

RMS_{ADC} is the RMS value of ADC output noise in LSB. The relationship between RMS ENOB ($ENOB_{RMS}$) and noise-free ENOB ($ENOB_{NF}$) is shown as below:

Table 6.1 $ENOB_{rms}$ of PADC under different ODR setting (VREF = 4V, 'SYS_CHOP_EN' = 0)

ODR (Hz)	Gain														
	1	2	4	6	8	12	16	24	32	48	64	96	128	192	256
2400	17.9	18.0	17.8	17.8	17.8	17.6	17.8	17.7	17.6	17.5	17.3	16.9	16.5	16.1	15.6
1200	18.3	18.4	18.3	18.3	18.2	18.2	18.2	18.0	18.0	17.8	17.5	17.2	16.8	16.3	16.0
600	18.7	18.6	18.5	18.7	18.6	18.6	18.6	18.4	18.4	18.1	17.9	17.6	17.1	16.7	16.3
300	19.0	18.9	19.0	19.0	18.8	18.9	18.8	18.8	18.6	18.6	18.3	18.0	17.6	17.1	16.7
150	19.7	19.5	19.7	19.6	19.6	19.6	19.6	19.4	19.3	19.0	18.9	18.5	18.0	17.6	17.2
75	20.7	20.9	20.6	20.6	20.7	20.6	20.4	20.1	20.1	19.8	19.5	19.0	18.6	18.1	17.7
37.5	21.2	21.4	21.1	21.1	21.0	21.0	21.0	20.8	20.7	20.3	20.0	19.6	19.2	18.7	18.3
18.75	21.8	21.9	21.5	21.7	21.6	21.6	21.4	21.3	21.2	20.8	20.5	20.1	19.7	19.2	18.8
10*	22.3	22.3	22.0	22.1	22.1	22.1	22.0	21.8	21.6	21.2	21.0	20.5	20.1	19.6	19.2
5*	22.7	22.7	22.5	22.6	22.6	22.5	22.4	22.3	22.0	21.7	21.3	21.0	20.6	20.1	19.7
2.5*	23.0	23.1	23.0	23.0	23.0	22.9	22.9	22.7	22.5	22.1	21.8	21.5	21.1	20.6	20.2

*For ODR of 10Hz, 5Hz and 2.5Hz, two filter settings can be selected but with the same $ENOB_{RMS}$

*When ODR_P≤10Hz, the 50 or 60Hz notch filter will be activated. Users can choose the proper notch filter for different applications. The error of the clock rate is designed to be less than 1% to minimize the effect to the notch filter.

6.2.4. System Chopping

When 'SYS_CHOP_EN' = 1, the system chopping mode of primary signal channel is enabled. When this mode is used, the input-referred offset of the primary signal channel can be very small. Meanwhile, the system chopping can also improve the immunity of RFI/EMI. ENOB will be 0.5-bit higher when system chopping is enabled, with the actual ODR is about half of the set ODR_P when ODR_P<=600Hz. For ODR_P>600Hz, the actual ODR is 1/4 of setting ODR_P at minimum.

6.3. Analog Module 2: Temperature Measurement Channel

The temperature measurement channel is to measure the working temperature of the sensor for the temperature compensation of the sensed signal. This channel works independently of the primary signal measurement channel. The NSA2860 supports both internal temperature sensor and external temperature sensor, selected by register bit 'EXT_TEMP' bit. The temperature sensor's output is digitized by a 24-bit ADC (TADC) and also digitally filtered. The ODR setting of the temperature measurement channel is the same as the primary signal channel, set by 'ODR_T'. When the temperature difference between the sensor element and the NSA2860 chip is acceptable, internal temperature sensor can be used. Otherwise, a proper external temperature measurement scheme should be chosen, such as diode, RTD or the bridge resistor itself, etc. Through different 'RAW_T' settings, either the direct TADC data or the calibrated temperature data can be read from 'TDATA' registers.

6.3.1. Internal Temperature Sensor

The internal temperature sensor is factory calibrated, with its calibration coefficients stored at EEPROM registers reg0xC1, reg0xC2 and reg0xC3. When 'RAW_T' is set to 0 and 'GAIN_T' is set to 4X automatically, the NSA2860 can provide a temperature reading in degree Celsius, in the format of:

$$T = TDATA/2\,^\wedge 16 + 25℃$$

For example, 'TDATA = 0x1FF24B' corresponding to 56.95 ° C. The relationship between the noise of the internal temperature sensor and 'ODR_T' setting is shown in Table 6.2.

Table 6.2 RMS noise of internal temperature sensor under different ODR_T

ODR (Hz)	2400	1200	600	300	150	75	37.5	18.75	10	5	2.5
RMS Noise in ℃	0.0079	0.0060	0.0045	0.0038	0.0032	0.0020	0.0015	0.0011	0.0008	0.0008	0.0007

6.3.2. External Temperature Sensor

When external temperature sensor mode is selected, the temperature sensing signal input from the TEMP pin is buffered for TADC conversion. The reference voltage of the TADC is also VREF. The gain of the TADC can be 1X, 2X and 4X. The relationship between $TDATA_{RAW}$ and the temperature input is:

$$TDATA_{RAW} = VTEMP * GAIN\_T/VREF * 2^{23}$$

When RAW_T = 0, the built-in MCU calibrated the offset, sensitivity and nonlinearity of the measured temperature signal. Please refer to application note NOVOSENSE provided for calibration description details. The external temperature sensing can be done in many ways, including RTD, diode and sensor bridge resistance itself. Figure 6.3 gives an example using a low TC drift resistor to sense the bridge resistance, which is usually proportional to the temperature of the sensor element. In case the bridge sensor is current driven, the bridge voltage can be used as temperature sensing input directly.

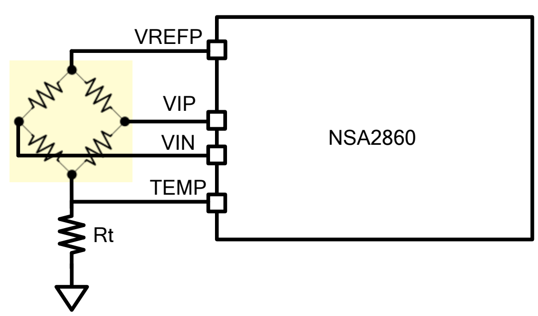


Figure 6.3 External temperature sensing using sensor bridge and a reference resistor

The output data rate of TADC can be set by 'ODR_T', similar as the primary signal channel. The relationship between ODR_T and the ENOB of TADC is shown in Table 6.3.

Table 6.3 ENOB of TADC under different ODR_T (External temperature sensor mode)

ODR_T (Hz)	ENOB		
	GAIN_T = 1	GAIN_T = 2	GAIN_T = 4
2400	17.7	17.5	16.9
1200	18.1	17.9	17.2
600	18.5	18.1	17.2
300	18.8	18.3	17.4
150	19.1	18.5	17.6
75	19.5	18.9	18.0
37.5	19.4	18.6	17.6
18.75	19.9	18.7	18.1
10	20.2	19.4	18.5
5	20.2	19.6	18.5
2.5	20.9	19.9	18.8

6.4. Analog Output Stage

The analog output stage of the NSA2860 consists of a 16-bit DAC and an output buffer with feedback network. Through register configuration and external connection, the NSA2860 provides a lot of output modes such as absolute voltage output (0~5V, 0~3.3V, 0~1.2V), ratiometric voltage output (0~AVDD), 0~10V voltage output, PDM output, PWM output, and 4~20mA current loop. The output mode of analog output stage can be configured by 'OUT_MODE' registers, which is an independent configuration from analog front-end ADC.

6.4.1. 16-bit DAC

The voltage output of the DAC is expressed by the following equation,

$$VOUT = \frac{DAC\_DATA < 15:0 >}{2\,^\wedge 16} * VFSDAC$$

'DAC_DATA' stores the DAC input data in an unsigned format. VFSDAC is the full-scale range of DAC, which is configured by 'DAC_REF'. When 'RAW_P' = 0, the 'DAC_DATA' is updated by the internal MCU with the calibrated output data.

6.4.2. Analog Output Clamping

The DAC full-scale range is clamped by the clamping voltage configured by 'CLAMP_HIGH' and 'CLAMP_LOW'.

The low clamping voltage is defined by the following equation,

$$VOUT\_LOW = \frac{CLAMP\_LOW < 7:0 >}{2\,^\wedge 9} * VFSDAC$$

The high clamping voltage is defined by the following equation:

$$VOUT\_HIGH = (1\text{-}\frac{CLAMP\_HIGH < 7:0 >}{2\,^\wedge 9}) * VFSDAC$$

When 'RAW_P' = 1, the 'DAC_DATA' stops updating internally, but can be configured externally through serial interface, and the offset error and full-scale range error of analog output stage should also be measured and calibrated externally. In this case, the 'DAC_BLANK' bit should be used to erase the glitch generated during the 'DAC_DATA' updating. Set 'DAC_BLANK' bit as 1 before refreshing the 'DAC_DATA', and 0 after that.

The DAC output noise can be reduced by a low-pass RC filter, which is comprised by the internal 120kohm resistor and external capacitor between FILTER/HART pin and GND pin. For example, a 47nF external capacitor will limit the signal bandwidth as low as 30Hz. However, in some fast response applications, smaller external filtering capacitor should be chosen.

6.4.3. Voltage Output

When OUT_MODE = 3'b000, analog output stage is configured as voltage output mode. A class-AB output buffer is used to drive large load and the OUT pin and FBN pin should be shorted together as shown in Figure 6.4. The gain of output buffer is configured by 'DAC_REF' to provide several types of full-scale output range, such as absolute output (0~5V, 0~3.3V, 0~1.2V) and ratiometric output (0~AVDD), as listed in Table 6.4. The internal bandgap reference is used for absolute output.

Table 6.4 'DAC_REF' and output mode

DAC_REF<1:0>	*Output Mode*	*Output Voltage Range*
2'b00	Absolute	0~5V
2'b01	Absolute	0~3.3V
2'b10	Absolute	0~1.2V
2'b11	Ratiometric	0~AVDD

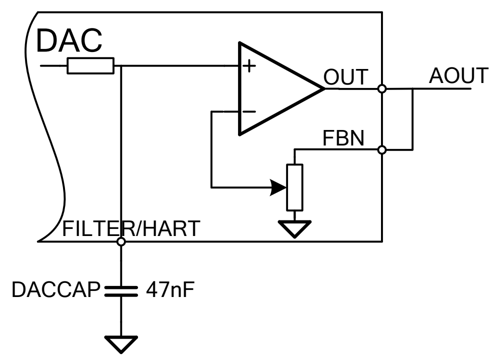


Figure 6.4 Configuration for voltage output mode

0~10V full-scale output range is also available as shown in Figure 6.5 with a few external components, where DAC_REF<1:0> = 2'b00.

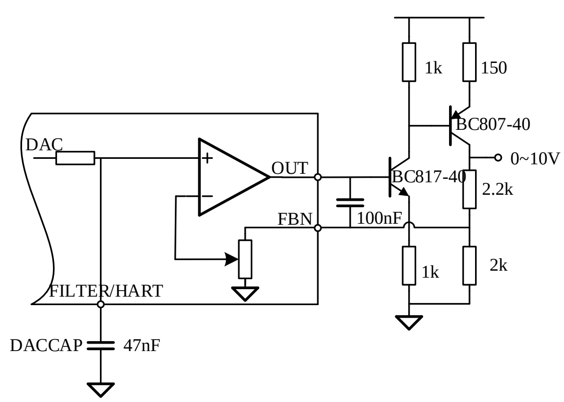


Figure 6.5 Configuration for 0~10V output mode

6.4.4. 4~20mA Current Loop

When OUT_MODE = 3'b01x and DAC_REF<1:0> = 2'b00, analog output stage is configured as 4~20mA current loop mode. Internal bandgap reference with very low temperature drift is used for DAC reference. When using 50ohm external reference resistor, the loop current can be expressed as followed:

$$\mathrm{ILOOP} = \mathrm{DAC\_DATA} < 15:0 > /2^{\wedge}16 * 24\mathrm{mA}$$

The loop current transfer function is also shown in Figure 6.7. The minimum of ILOOP is about 1.5mA, which is determined by the self-operation current of the NSA2860. To remain above the 4mA lower limit for 4~20mA current loop, the total current consumed by the NSA2860 and sensor element should be less than 3.5mA.

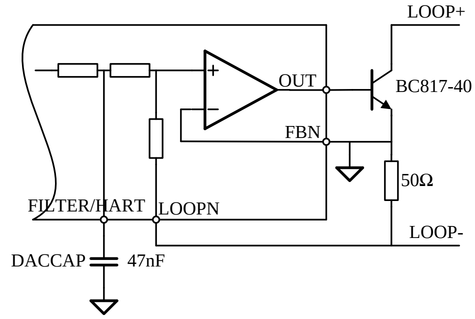


Figure 6.6 Configuration for 4~20mA current loop mode

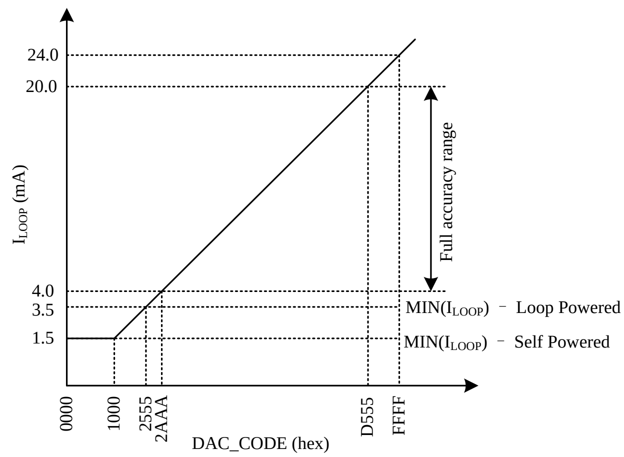


Figure 6.7 Loop current transfer function

The FILTER/HART pin can not only be used for noise filtering, but also for HART communication in current loop mode. As shown in Figure 6.8, the 500mVpp HART signal can be modulated into current loop as 1mApp current through a 470pF capacitor.

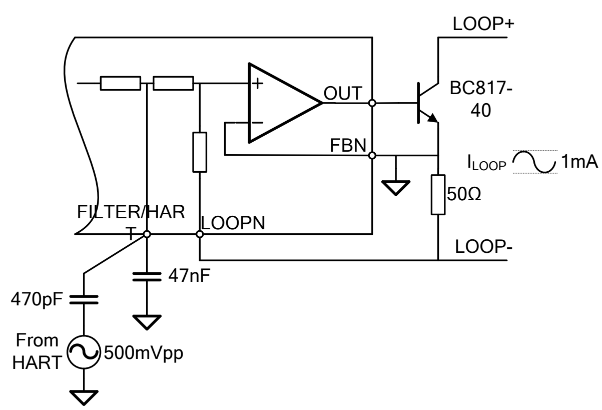


Figure 6.8 Configuration for HART communication

6.4.5. PDM

When ‘OUT_MODE’ = 3’b100, analog output stage is configured as PDM output mode. The ‘DAC_DATA’ is converted to 1-bit PDM single by a 1-order modulator internally and outputted through OUT pin. An external RC filter should be connected to OUT pin to filter the PDM signal to analog voltage. Digital isolation output can also be realized by external level shifter and isolation device. ‘PDM_FREQ’ is used to set the PDM output frequency. The equivalent output resistance at OUT pin is about 20ohm. As a result, when using external RC filter, the equivalent resistance load should be less than 20kohm as to make sure the output error is less than 1‰. Two-stage low-pass RC filter in series is recommended as shown in Figure 6.9. Some RC filter examples are provided in Table 6.5.

Table 6.5 RC filter examples for PDM output

R1 (kohm)	C1 (nF)	R2 (kohm)	C2 (nF)	Ripple（mV/V）	0~90% Settling Time(us)
100	22	100	22	0.12	14
100	100	0	0	2.5	24
100	220	0	0	1.2	50

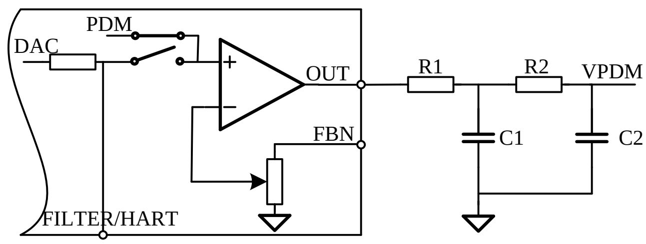


Figure 6.9 RC filter for PDM output

6.4.6. PWM

Both primary signal channel and temperature measurement channel support PWM output.

When 'OUT_MODE' = 3'b101, primary channel output data will present on the OUT pin in PWM format. The PWM carrier frequency is fixed at 300Hz, and the PWM output duty cycle is decided by DAC_DATA<15:4> with 12-bit resolution,

$$\text{PWM Duty Cycle of Primary Channel} = \text{DAC\_DATA}\,[15{:}\,4]/4096$$

When 'TOUT_EN' = 1 and the chip is not in OWI mode, the OWI pin is used as the output pin for Temperature Channel data in PWM format and the PWM output duty cycle is defined below:

$$\text{PWM Duty Cycle of Temperature Channel} = \text{TDATA} < 23{:}\,12 >/4096$$

6.5. Power Management and Sensor Drive

The NSA2860 internally includes a precision bandgap reference with very low temperature drift, less than 0.1% during full temperature range (-40~85℃). This reference voltage is used in the constant voltage or current driving circuits for sensors, JFET regulator, clock generator and ADC/DAC etc.

6.5.1. Sensor Driver

6.5.1.1. Sensor Driver

The VREFP pin can provide a constant voltage to drive the bridge sensors, which is also the reference voltage for PADC and TDAC (in external Temperature Sensor Mode). The constant driving voltage can be selected as either 4V or 2.5V via the EEPROM register bit 'VREF_LVL'. When 'VREF_DIS' = 1, VREFP pin can be driven from the external reference voltage.

When TADC is activated (ODR_T ≠ 4'b1111), the negative reference voltage (VREFN) for PADC is internally connected to GND; when TADC is disabled (ODT_T = 4'b1111), the negative reference voltage (VREFN) for PADC is driven externally through TEMP pin.

6.5.1.2. Constant Current Drive

A pair of constant current sources is available for current-driven pressure sensors, RTD sensors and external diode temperature sensors. The constant driving current can be configured with internal or external reference resistor as shown in Figure 6.10. When 'IEXC2' ≠ 4'b1111, an internal reference resistor is used and the current output through IEXC1 and IEXC2 pins are separately configured by 'IEXC1' and 'IEXC2' with the mismatch less than 1%.

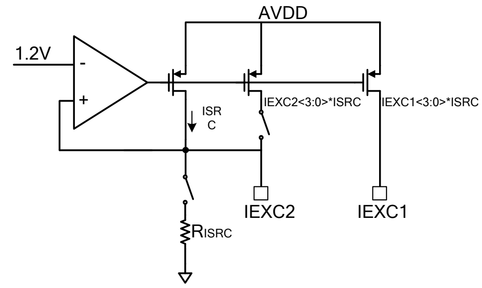


Figure 6.10 Constant Current Driver

When 'IEXC2' = 4'b1111, external reference resistor is applied at IEXC2 pin instead of internal reference resistor. The temperature drift of current source will be smaller when using accurate reference resistor externally. The current source is only available at IEXC1 pin, which is equal to IEXC1<3:0>*1.2V/RISRC_EXT.

6.5.2. JFET Regulator

By tuning the gate of external JFET (for example, BSS169) through VGATE pin, the JFET regulator integrated in the NSA2860 can convert the external high voltage supply to 5V (JFET_LVL = 0) or 3.3V (JFET_LVL = 1) and supply it to the VDDHV pin (Figure 6.11) or AVDD pin. An external NPN bipolar (for example, BCX5610) with a 50kohm resistor is also suitable for this regulation in case the high voltage supply is higher than 8V (Figure 6.12).

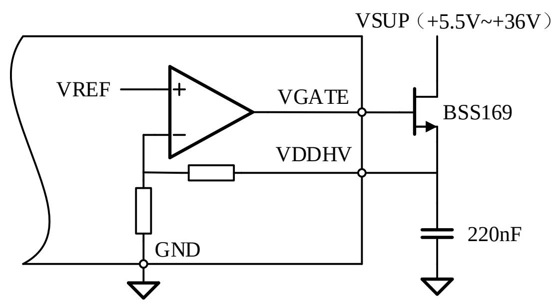


Figure 6.11 Regulation with external JFET

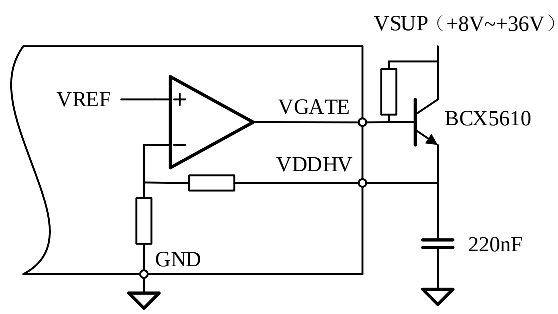


Figure 6.12 Regulation with external NPN Bipolar

6.5.3. Internal LDO

A 1.8V LDO is integrated in the NSA2860 to provide power supply for the internal digital circuits. A 100nF decoupling capacitor should be connected to DVDD pin externally.

6.5.4. Power on Reset

A POR block is integrated in the NSA2860 for power on reset and EEPROM loading. When AVDD<2.5V, the chip is in reset state. After AVDD>2.5V, the POR output is released and EEPROM is loaded afterwards. The POR circuits have 100mV hysteresis, i.e. the chip won't go into the reset state again until the AVDD is dropped as low as 2.4V.

6.6. Built-in MCU Core and Control Logics

6.6.1. Work Modes

Two Different work modes are supported by the NSA2860, command mode and active mode, which can be configured by the register 'CMD' (Reg0x30).

6.6.1.1. Command Mode

The command mode can be entered by writing the register 'CMD' with 0x00, which is used for configuring the chip outside. All the EEPROM registers (from Reg0xA1 – Reg0xD9) can be modified only in this mode.

6.6.1.2. Active Mode

The active mode is the default mode after powering up, which can also be entered by writing the register 'CMD' with 0x03. In this mode, the primary measurement channel and the temperature channel continuously update their measured values into the 'PDATA' or 'TDATA' registers, and the selected output mode will be activated simultaneously. When the register bit 'RAW_P/T' = 1, the ADC conversion results will be put into the 'PDATA' or 'TDATA' directly; otherwise, every time the primary measurement channel ADC conversion ends, the built-in MCU core performs sensor calibration flow once with the latest temperature value measured. When the register bit 'INT_EN' = 1, the SDO_DRDYB pin is used to indicate that new data are ready for reading via the serial interface with an active low voltage level, and this pin will come back to high level after the data reading or about 100us before next new data's coming.

Even without the SDO_DRDYB pin, the shadow registers inside the NSA2860 can also guarantee a non-glitch reading by keeping the 'PDATA' and 'TDATA' registers stable during once serial interface reading. Note that, the multiple bytes of one measured data should be read out together in once multi-byte serial interface reading command.

6.6.2. EEPROM

64 bytes EEPROM is contained in the NSA2860 to store the chip configurations and sensor calibration coefficients.

6.6.2.1. Loading

The contents of the EEPROM will be loaded into the EEPROM registers automatically after power up or soft-reset with the CRC checking. If the calculated CRC result does not match with what has been stored in the EEPROM, the 'CRC_ERROR' bit will be set and the analog output state will be decided according to the fault diagnostic and alarm configurations. Another status register bit 'LOADING_END' will be set after the loading completes.

6.6.2.2. Programming

After EEPROM registers will not be programmed into the EEPROM directly after OWI writing. The contents of the EEPROM registers will be programmed into the EEPROM by the following sequence:

Set the register byte 'COMMAND' (Reg0x30) with 0x33 to enter EEPROM programming mode;

Write the register byte 'EE_PROG' (Reg0x6A) with 0x1E to start EEROM programming.

During EEPROM programming, a new CRC check code will be generated according to the contents of the EEPROM registers and will be programmed to the EEPROM simultaneously. The content of the 'EE_PROG' register will come back to 0x00 automatically to indicate the programming is done. Another power cycler or soft-reset is needed to reload the EEPROM contents back to the EEPROM registers to check the programmed value.

6.6.2.3. Lock and Unlock

The EEPROM inside the NSA2860 can be locked by setting the 'EEPROM_LOCK' bit and programming it into the EEPROM. After locked, the EEPROM cannot be programmed again, and only a special EVA-kits provided by NOVOSENSE can unlock it.

6.6.3. Built-in MCU Core

The NSA2860 is integrated with a built-in MCU core, which performs signal processing, sensor calibration, EEPROM loading and programming etc. The MCU's program code is pre-stored in the internal ROM, which cannot be modified by customers. Please contact NOVOSENSE if a customized MCU program code is needed.

6.6.4. Calibration

The calibration inside the NSA2860 is divided into two parts. The first is the DAC calibration, which can lower the offset and sensitivity error induced by the DAC block. The second is sensor calibration, which can compensate sensor offset, sensitivity, temperature drift up to 2^{nd} order, and non-linearity up to 3^{rd} order. Please refer to application note NOVOSENSE provided.

6.7. Fault Detection and Alarm

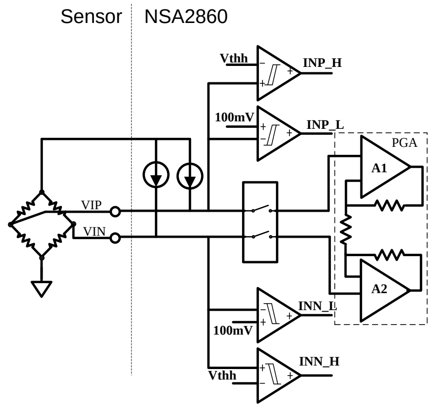


Figure 6.13 Fault detection

6.7.1. Fault Detection

Setting register bit 'BURNOUT_EN' = 1 enables the fault diagnosis. When diagnosis is enabled, a pair of 100nA burnout current sources is applied to the input of the primary signal channel. Four comparators will be activated to monitor the input voltages. Two comparators compare the input voltage to 100mV and the other two comparators compare the input voltages to upper limit level VTHH. VTHH depends on register bit 'VREF_DIS'. If 'VREF_DIS' = 0, VTHH = VEXT-100mV; otherwise VTHH = AVDD-1.1V. If any of the comparators' output is asserted, fault is detected and reported in the 'STATUS' register (reg0x02).

6.7.2. Alarm

If any fault is detected and register bit 'FAULT_ON' is set to 1, the alarm function of the NSA2860 will be triggered. The output will be forced to near GND or AVDD if it is not in current loop mode. Register bit 'FAULT_LVL' is used to set fault level to pulling down to 'GND' ('FAULT_LVL' = 0) or pulling up to 'AVDD' (FAULT_LVL = 1). If it is in current loop output mode, the loop current will be forced to 3.375mA ('FAULT_LVL' = 0) or 21.75mA ('FAULT_LVL' = 1). Together with the clamping function, fault can be easily distinguished from signal saturation.

7. Serial Interface

Three different serial interfaces (OWI, SPI and I^2C) are supported in the NSA2860 to configure registers, program EEPROM and read measured data. When register bit 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is defined as the OWI entering window. If a specific 24 bits OWI entering pattern is detected via OWI pin in this window, the chip enters OWI communication mode, otherwise enters I^2C or SPI communication mode. Then, CSB pin is used to further select between I^2C and SPI methods: high voltage level or floating indicates the I^2C method, low voltage level indicates the SPI method. When 'OWI_WINDOW' = 1, the OWI window's length becomes infinite.

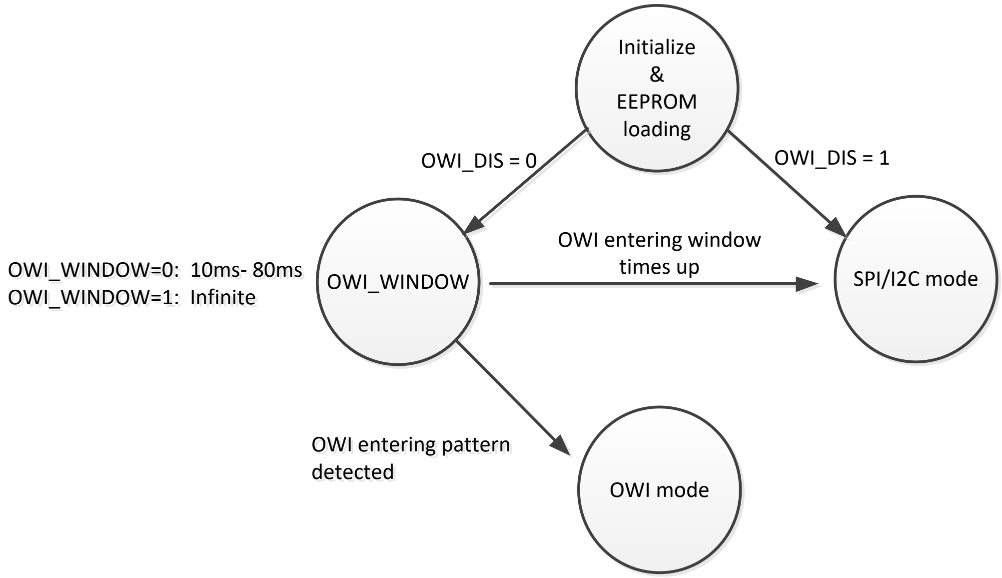


Figure 7.1 Definition of serial communication mode

7.1. OWI Protocol

The NOVOSENSE self-owned One Wire Interface (OWI) protocol integrated in the NSA2860 can support serial communication under all 0~5V, 0~10V and 4~20mA output modes with no extra communication wires added. This protocol identifies the data bit transferred by the duty cycle of one rising-to-rising period. Duty cycle more than 5/8 means a logical 1, and less than 3/8 means a logical 0.

7.1.1. Timing Spec

Table 7.1 OWI Timing Spec

Symbol	*Description*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{period}	OWI bit period		20		4000	µs
t_{pulse_0}	Duty cycle for 0		1/8	1/4	3/8	t_{period}
t_{pulse_1}	Duty cycle for 1		5/8	3/4	7/8	t_{period}
t_{start}	Start low pulse time		20		4000	µs
t_{stop}	Stop condition time		2			t_{period}

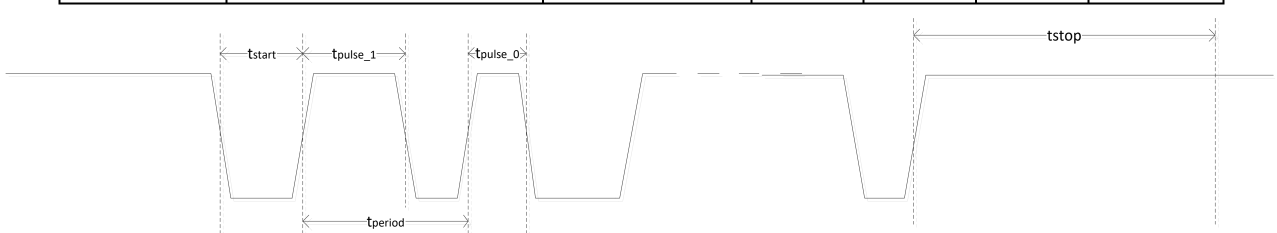


Figure 7.2 OWI Timing

7.1.2. Enter OWI Mode

If 'OWI_WINDOW' = 0, the time between 10ms and 80ms after powering up is OWI entering window. If a special 24 bits OWI entering pattern (0xB5A6C0, as shown below) is detected via OWI pin in this window, the chip enters OWI communication mode. Under this setting, the OUT pin is disabled during the OWI window and OWI mode; the OWI pin and the OUT pin can be shorted together to support 3-wire sensor products.

If 'OWI_WINDOW' = 1, the OWI window's length becomes infinite, the OUT pin is activated during OWI window and OWI mode, and the OWI pin and OUT pin cannot be shorted together.

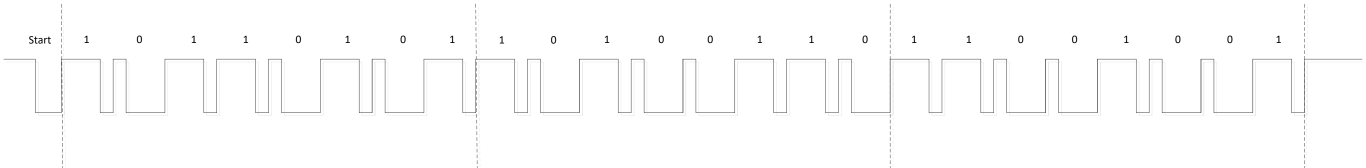


Figure 7.3 OWI Entering Pattern

In OWI communication, the bit period is determined by the period of the last bit of OWI entering pattern, and cannot be changed during the entire communication, so the bit period during OWI communication should keep the same as the OWI entering pattern.

7.1.3. OWI Protocol

The OWI protocol used is defined as follows:

a) Idle State

During inactivity of the bus, OWI line is pulled-up to high voltage level.

b) Start Condition

When OWI line is in idle state, a low pulse (return to high) with a pulse width between 20μs to 4ms indicates a start condition. Every command has to be initiated by a start condition sent by the master. The master can only generate the start condition when the OWI line is in idle state.

c) Stop Condition

After the write or read operation ends, the bus comes back to the idle state automatically. During any time of a transmission, the bus can be set back to the idle state by forcing the OWI line to reach a constant high or low voltage level for at least two times of the bit period (t_{period})

d) Addressing

After the start condition, the master sends the addressing information, consisting of an 8-bit register address (MSB first), 2-bit byte number and a read/write bit (0–write, 1–read). The register address indicates which register you will write into or read from; the byte number indicates how many bytes will write/read continuously: 00: 1 byte, 01: 2 bytes, 10: 3 bytes, 11: 4 bytes; the read/write-bit indicates it a read operation (0) or write operation (1).

e) Write Operation

During transmission from master to slave (WRITE), the read/write bit is followed by 1/2/3/4 bytes (according to the byte NO. bits) transmitted data (MSB first), and the addressed register and follows will be refreshed to the written data after a stop condition.

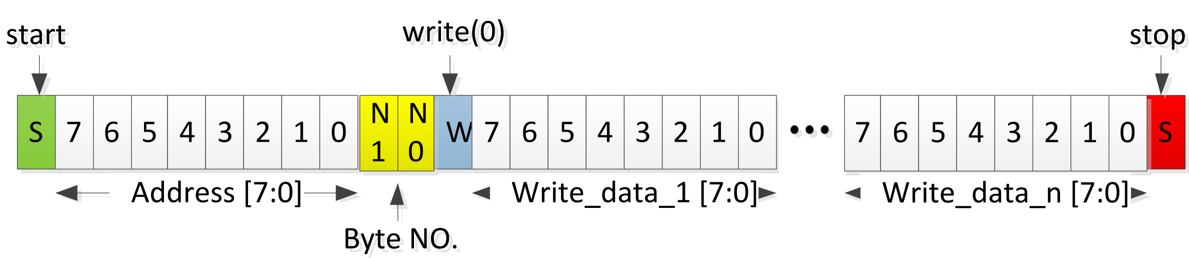


Figure 7.4 OWI Write Operation

f) Read Operation

During transmission from slave to master (READ), the master should set its OWI port as input after the read/write bit is sent, then the slave begins to transmit 1/2/3/4 bytes (according to the byte NO. bits) data (MSB first), which is the content in the addressed register and CRC data. Each data byte includes 8 bits of data and 2 bits of parity check code C1 and C0,

C1 = Read_data [7] ^ Read_data [5] ^ Read_data [3] ^ Read_data [1];

C0 = Read_data [6] ^ Read_data [4] ^ Read_data [2] ^ Read_data [0].

The master can check the transmission with the parity check code. After all data bytes transmitted, the slave goes back to idle state automatically.

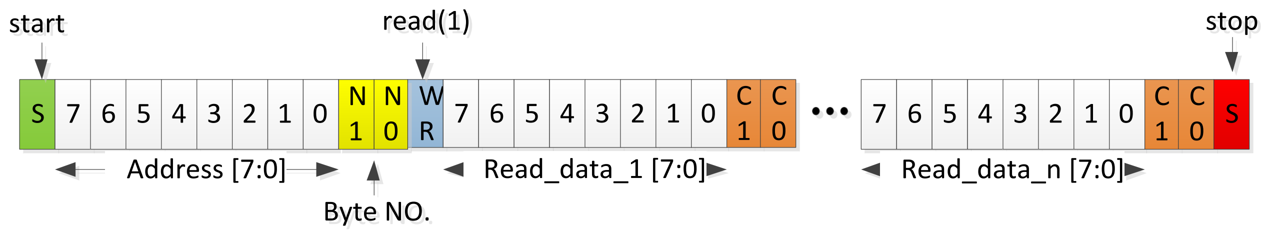


Figure 7.5 OWI Read Operation

7.1.4. Pins and Configurations

There are two pins (OWI and OUT) and two register bits (OWI_AC_EN and OWI_WINDOW) related to the OWI communication. Different applications can be supported via different configurations. Please refer to Table 7.2 for details.

OWI_AC_EN:

0, single-port communication method with the OWI pin used for both input and output port, which is typically used in 0~5V analog-output products;

1, dual-port communication method with the OWI pin as the slave input port and the OUT pin as the slave output port, which is typically used in the 0~10V and 4~20mA products.

OWI_WINDOW:

0, OWI mode should be entered between a 10ms and 80ms window after powering up;

1, the window is infinite and the OWI mode can be entered any time after powering up.

Table 7.2 Pin configurations for OWI communications

OWI_AC_EN	*OWI_Window*	*Windows*	*Input Port*	*Output Port*	*Output Mode*	*OUT Pin State Mode*	*Shorten OUT and OWI*	*Typical Applications*
0	0	10ms-80ms	OWI	OWI	OD	Hz	Supported	3-wire modules with 0~5V output (short OUT and OWI pins), external pull-up resistor is needed.
0	1	Infinite	OWI	OWI	OD	Signal Output	Not Supported	Cases that signal out and OWI communication are used simultaneously, external pull-up resistor is needed.
1	0	10ms-80ms	OWI	OUT	Push-Pull	OWI output	Supported	3-wire modules with 0~10V output, 2-wire modules with 4~20mA output. 0~5V output modules with big load capacitor.
1	1	Infinite	OWI	OUT	Push-Pull	OWI output	Supported	Isolated Transmitter using OWI/OUT pins for isolated communication.

7.1.5. Dual-Port OWI Communication (OWI_AC_EN = 1)

The special dual-port OWI communication is supported by the NSA2860 for applications in 4~20mA and 0~10V output products with no extra communication wires added. The protocol is shown in Figure 7.6, with the OWI pin as the slave input port, and the OUT pin as the slave output port.

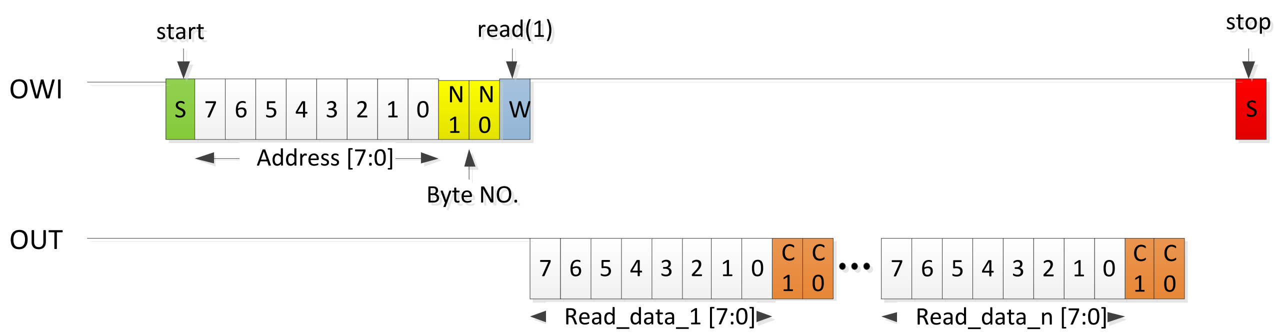


Figure 7.6 Dual Ports OWI Communication

As shown in Figure 7.7, in 4~20mA output applications, data transmission from the master to the chip is implemented by adding a square-waved signal on the power supply wire and AC coupling it onto the OWI pin with an external capacitor. The chip to master transmission data is modulated to the loop current (1: 10mA, 0: 4mA) and can be read out by the master through a comparator circuit. Limited by the response time of the current loop, the bit period of this OWI communication method should be no less than 100µs. The advantage of this kind of communication method is that the LOOP+/LOOP- wires are multiplexed for communications and no extra communication wires are needed. Similarly, in the 0~10V output applications, data transmission from the master to chip is also implemented by signal coupling from the power supply to the OWI pin, and data from chip to the master is put on the OUT pin. Also, only three wires (VDD, GND, OUT) are needed for a 0~10V product with no extra communication wires.

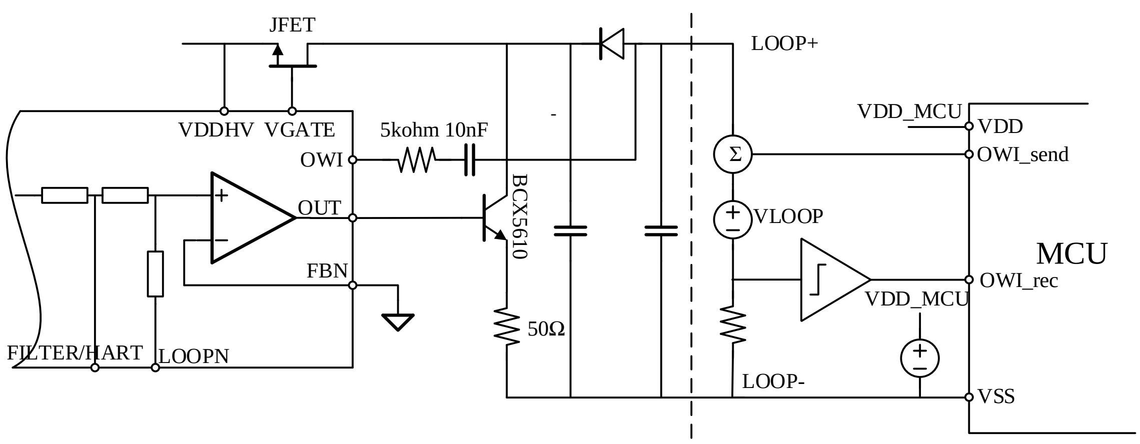


Figure 7.7 Typical circuit for the dual ports OWI communication in the 4~20mA applications

7.1.6. Quit OWI Communication

Writing Reg0x61 with 0x5d during OWI mode can temporarily or permanently quit the OWI communication for output voltage or current measuring. The register byte 'OWI_QUIT_CNT' is used to set the quit time with the LSB = 50ms (0x00 means permanently quit), and the chip will be back into OWI mode again after the quit time's up.

7.2. SPI Interface

7.2.1. Interface Specification

Table 7.3 SPI interface specifications

Symbol	Parameter	Condition	Min	Max	Unit
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		ns
t_{sclk_h}	SLCK high pulse		20		ns
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in Table 7.3.

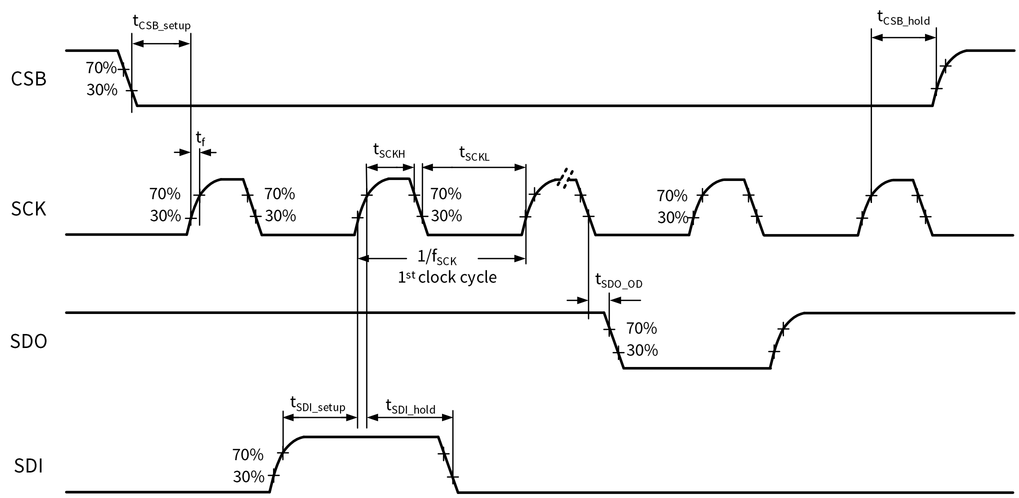


Figure 7.8 SPI Timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 7.9, the instruction phase is divided into a number of bit fields.

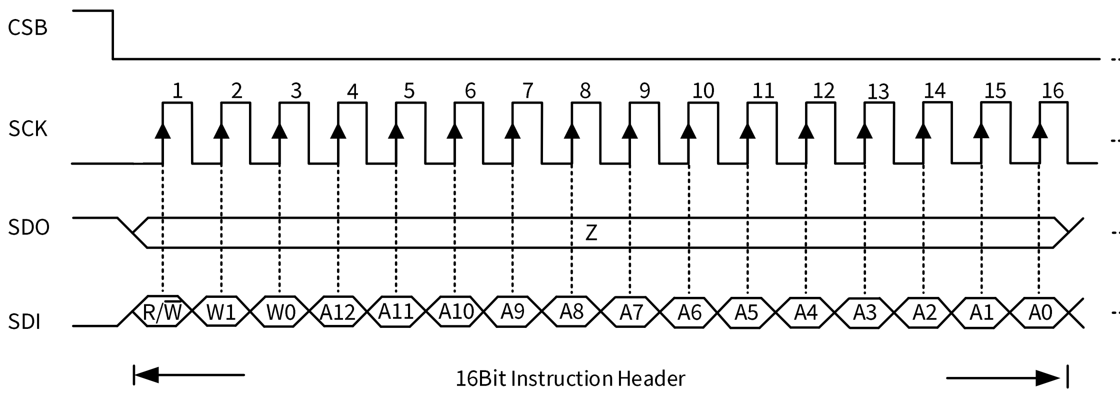


Figure 7.9 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read operation is being requested; otherwise a write operation is requested.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 7.4). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions to high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 7.4 W1 and W0 settings

W1:W0	***Action***	***CSB Stalling***
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for the entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). There can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed (Figure 7.10).

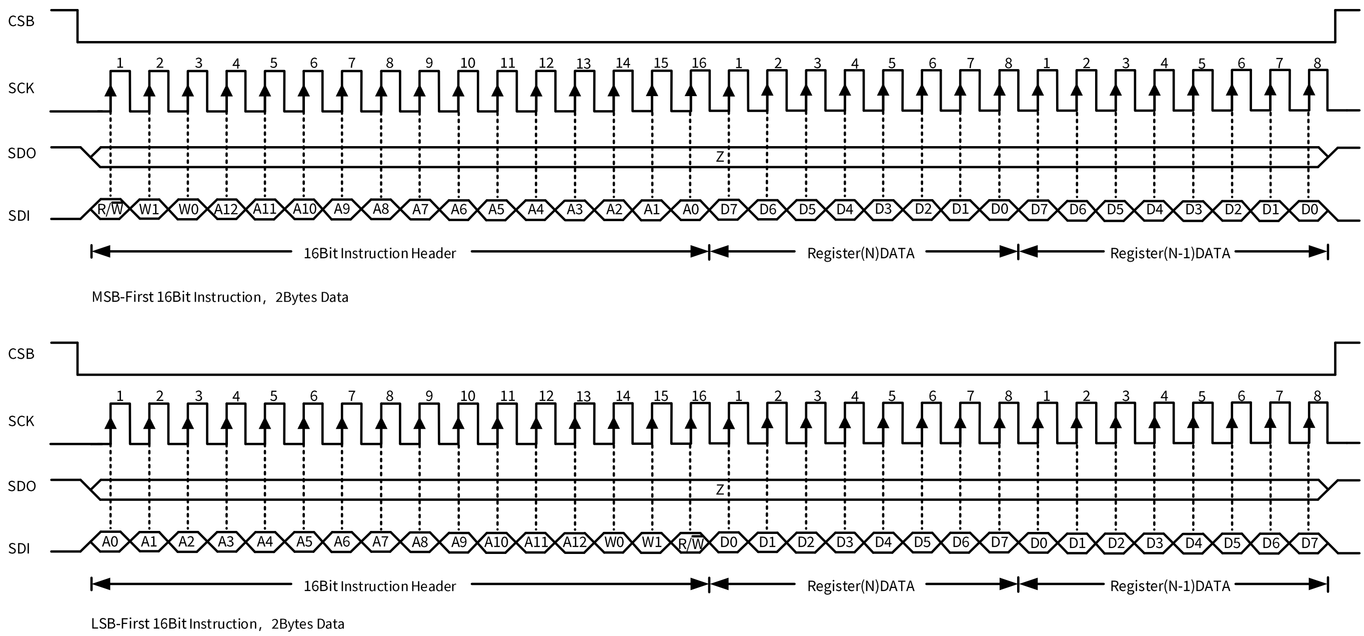


Figure 7.10 MSB First and LSB First Instruction and Data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

7.3. I²C Interface

I²C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I²C device address of NSA2860 is shown below. The LSB bit of the 7-bit device address is configured via SDO/ADDR pin.

Table 7.5 I²C Address.

A7	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*	*W/R*
1	1	0	1	1	0	1	0/1

Table 7.6 Electrical specification of the I²C interface pins

Symbol	*Parameter*	*Condition*	*Min*	*Max*	*Unit*
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		µs
t_{HIGH}	SCL high pulse		0.6		µs
t_{SUDAT}	SDA setup time		0.1		µs
t_{HDDAT}	SDA hold time		0.0		µs
t_{SUSTA}	Setup Time for a repeated start condition		0.6		µs
t_{HDSTA}	Hold time for a start condition		0.6		µs
t_{SUSTO}	Setup Time for a stop condition		0.6		µs
t_{BUF}	Time before a new transmission can start		1.3		µs

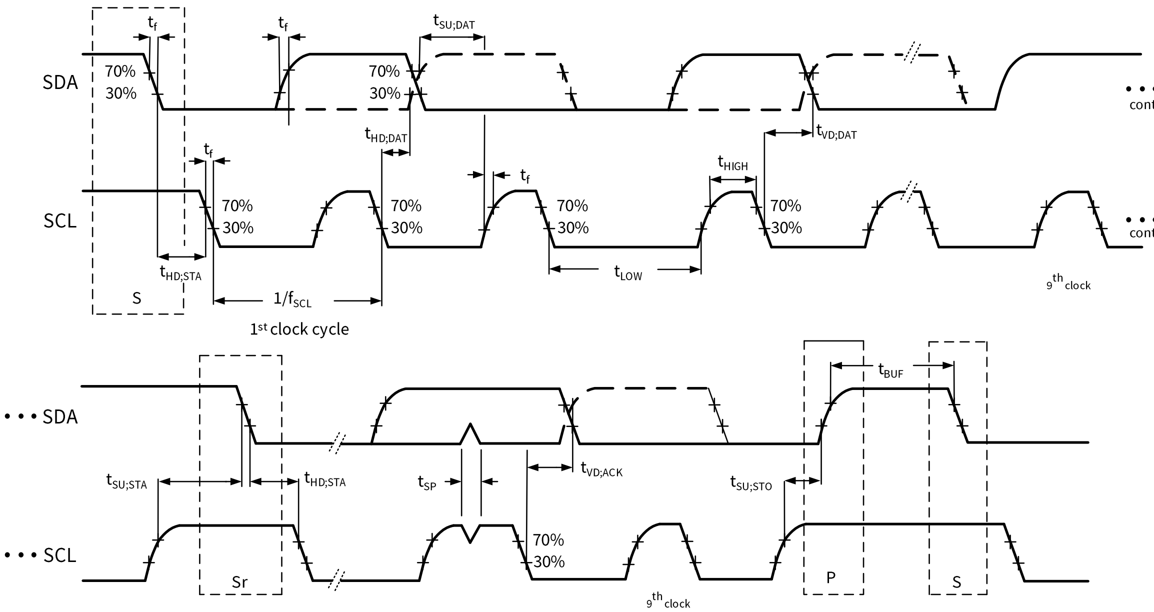


Figure 7.11 I²C Timing Diagram

The I²C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change values at SDA only when SCL is low.

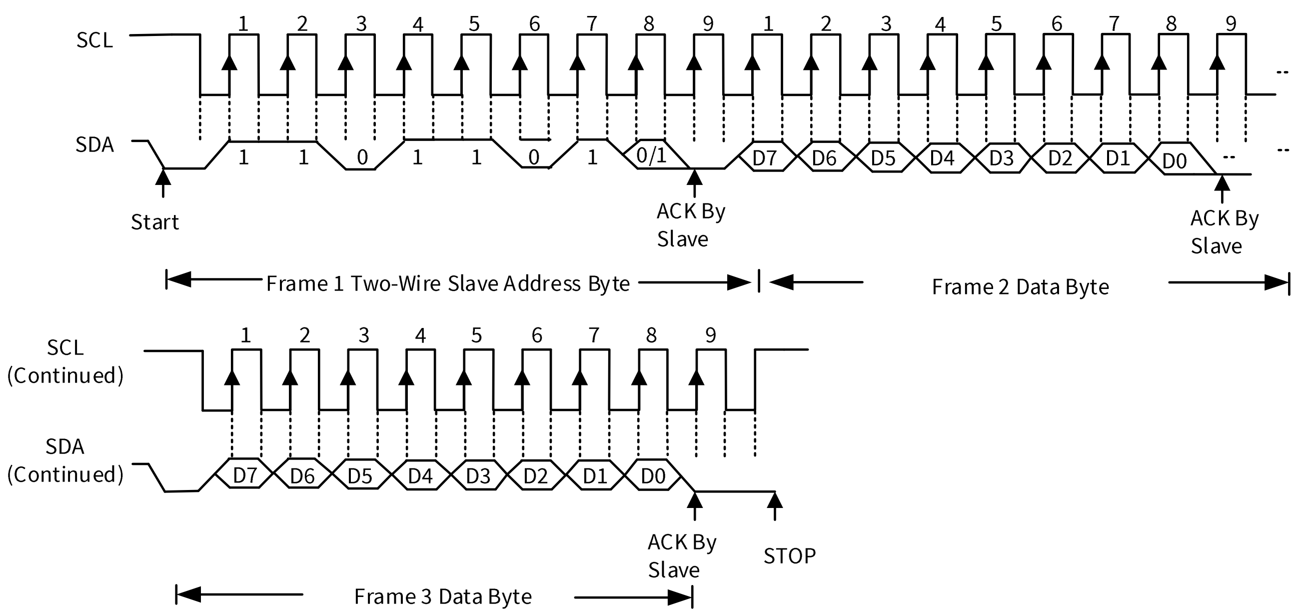


Figure 7.12 I²C Protocol (When *SDO/ADDR =1*)

NSA2860 can support single-byte read/write and multi-byte read/write operations. The transfer format is shown in Figure 7.13 and Figure 7.14.

Byte Write

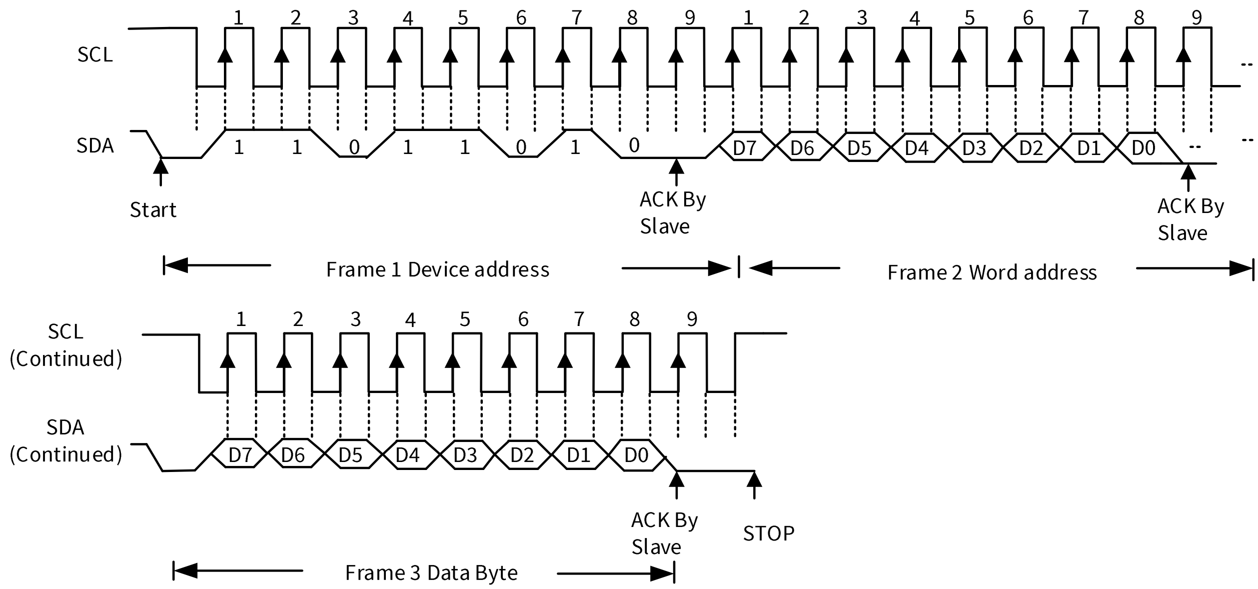


Figure 7.13 I²C Write Byte (When *SDO/ADDR =1*)

Random Read

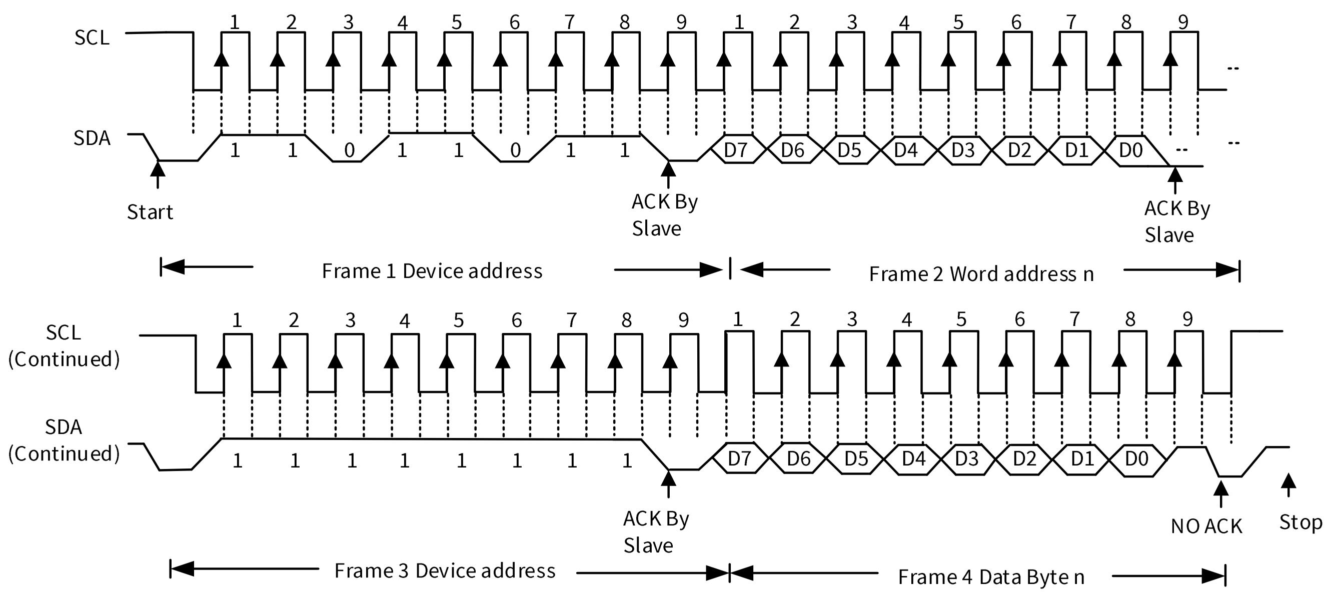
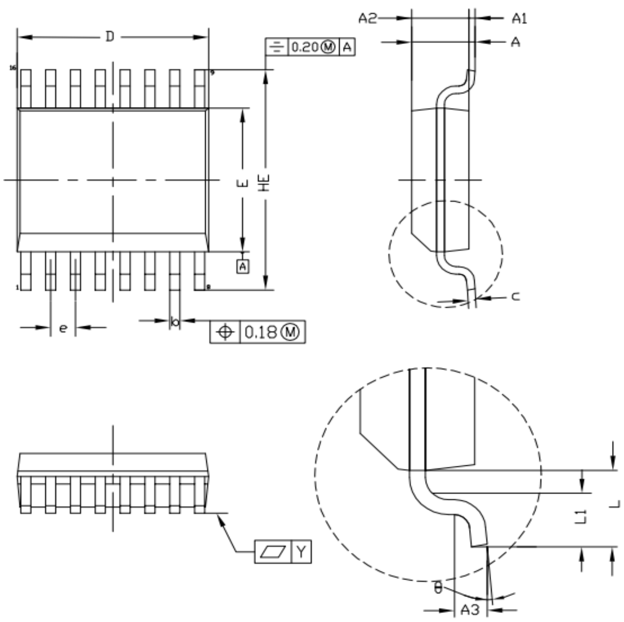


Figure 7.14 I²C Read Byte *(When SDO/ADDR =1*)

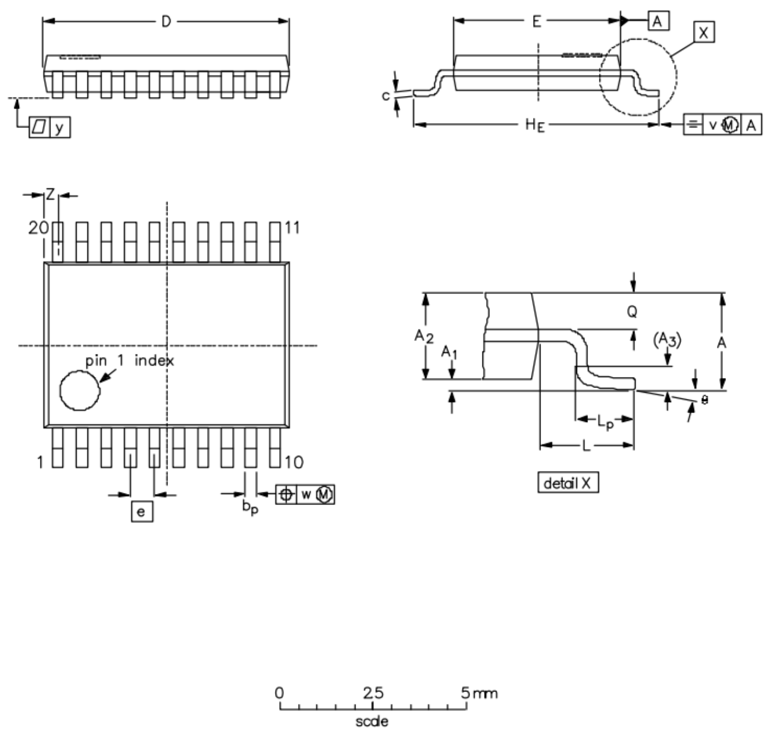
8. Package Information



※ CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 8.1 SSOP16 Package



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D (1)	E (2)	e	HE	L	Lp	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Figure 8.2 TSSOP20 Package

9. Typical Applications

9.1. Application 1: 0~5V Voltage Output Sensor

Function as absolute or ratiometric voltage output pressure sensor, with bridge driven by constant current source. Internal temperature sensor output is used for temperature compensation. For OWI communication, OWI can be separated with VOUT or shorted to VOUT pin.

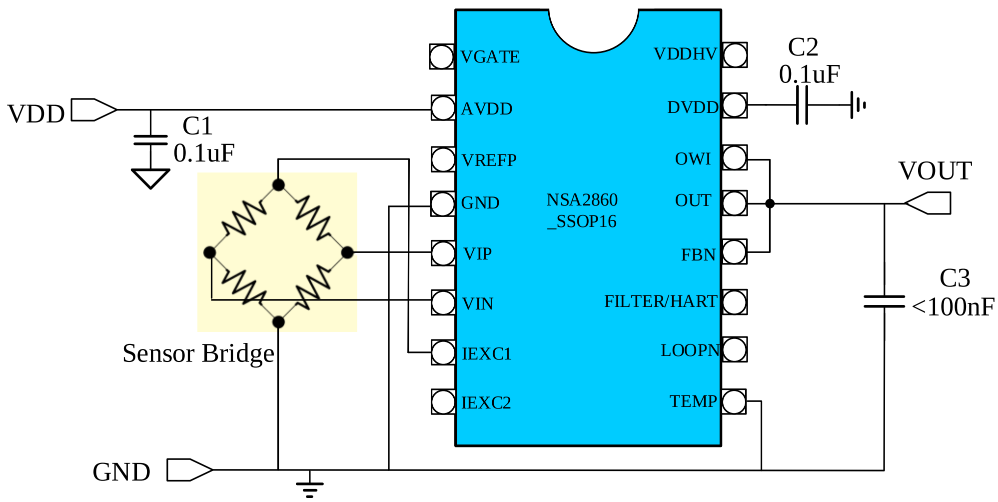


Figure 9.1 Absolute/ratiometric 0~5V voltage output

9.2. Application 2: 0~10V Output Pressure Transmitter

Below is an absolute 0~10V voltage output pressure transmitter with external JFET regulator. The sensor bridge is supplied by VREFP and an external diode is used as temperature sensor. C5 (>50V) is the AC coupling capacitor used for dual-port OWI communication, R1 is for protecting OWI pin, and C6 is an optional filtering capacitor.

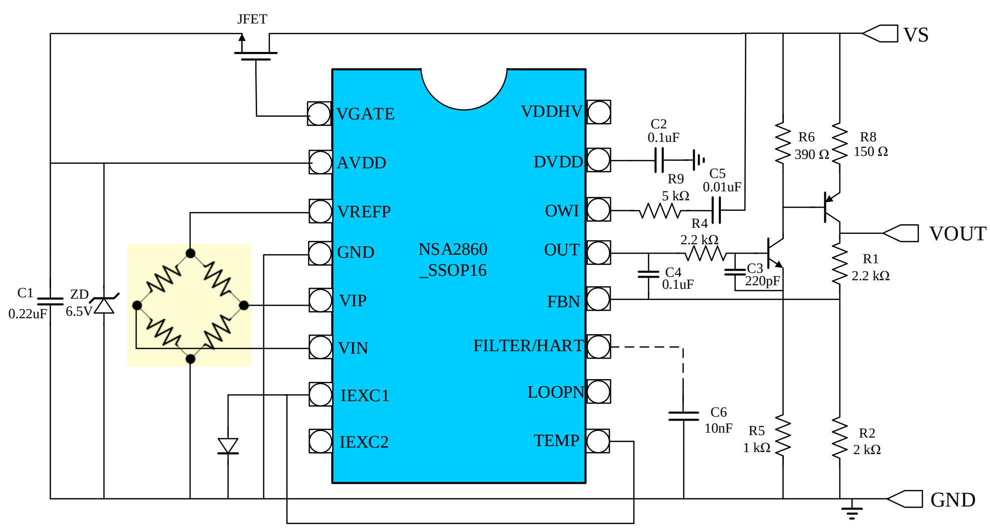


Figure 9.2 0~10V output pressure transmitter

9.3. Application 3: 4~20mA Pressure Transmitter 1

Use external JFET to supply AVDD. Sensor is driven by constant current. R4 (Low TC) is connected to IEXC2 (‘IEXC2’ set as 4’b1111) to generate low drift constant current. Bridge voltage is used as the external temperature sensor. R5 is 50ohm precision resistor with low TC for loop current feedback. Dual-port OWI communication is used with OWI pin as the input port, and the output data is modulated on the loop current. No extra wire is needed for communication.

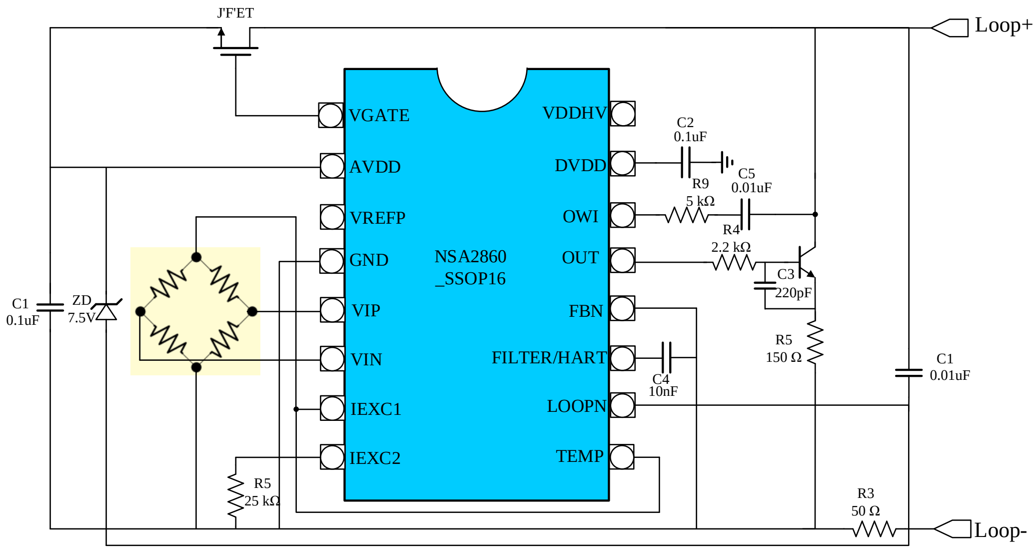


Figure 9.3 4~20mA output pressure transmitter (with JFET)

9.4. Application 4: 4~20mA Pressure Transmitter 2

Similar as application 3, except an NPN transistor and a 50kΩ resistor is used to replace the JFET, sensor is driven by VREFP and a low TC resistor is used to sensing the sensor temperature.

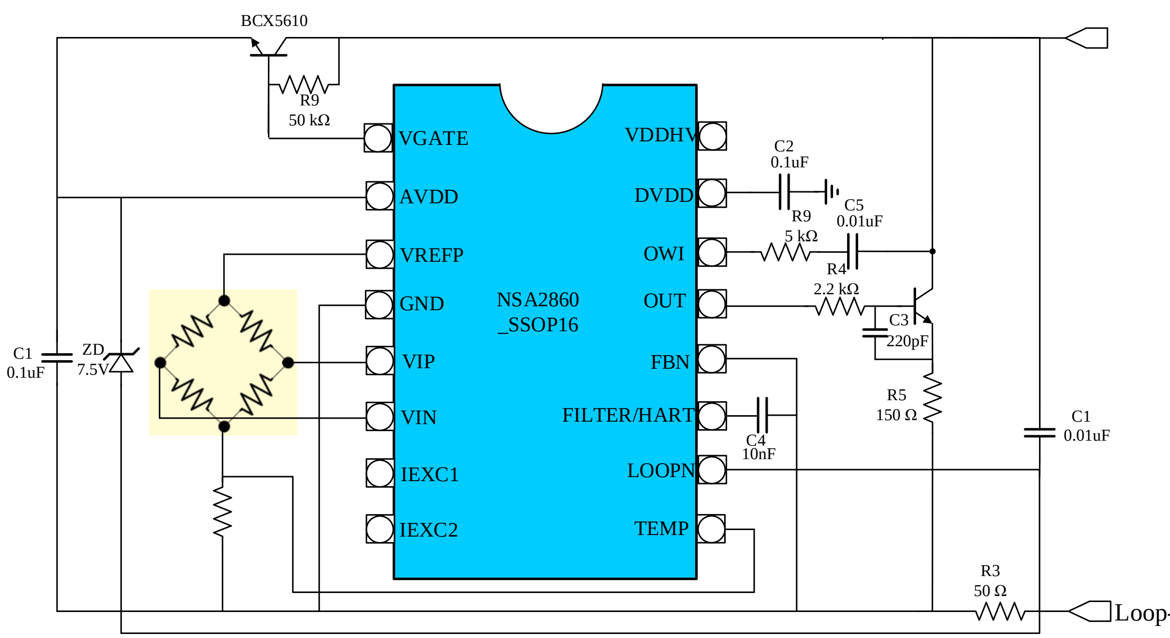


Figure 9.4 4~20mA output pressure transmitter (with bipolar)

9.5. Application 5: Isolated Pressure Sensor Transmitter

The NSA2860 is supplied with isolated power. 'OWI_AC' and 'OWI_WINDOW' are set '1' to allow the user to use OWI for communication between the NSA2860 and the external MCU through two channel digital isolator.

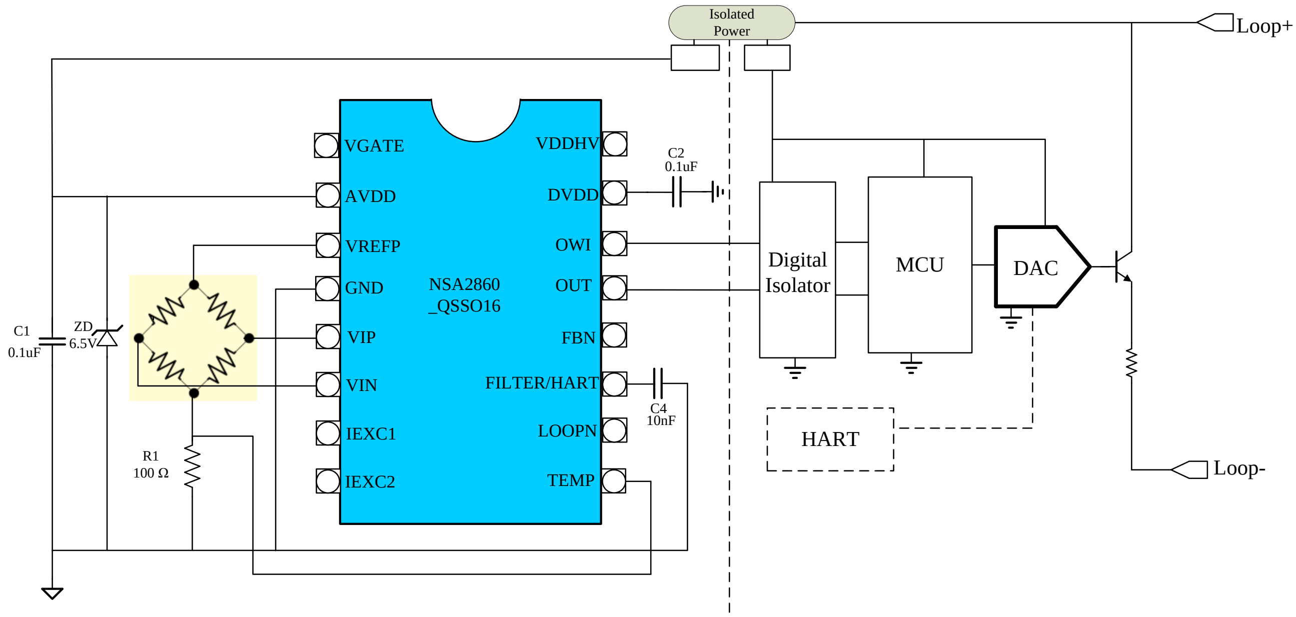


Figure 9.5 Isolated pressure transmitter

9.6. Application 6: Thermal Couple 4~20mA Temperature Transmitter

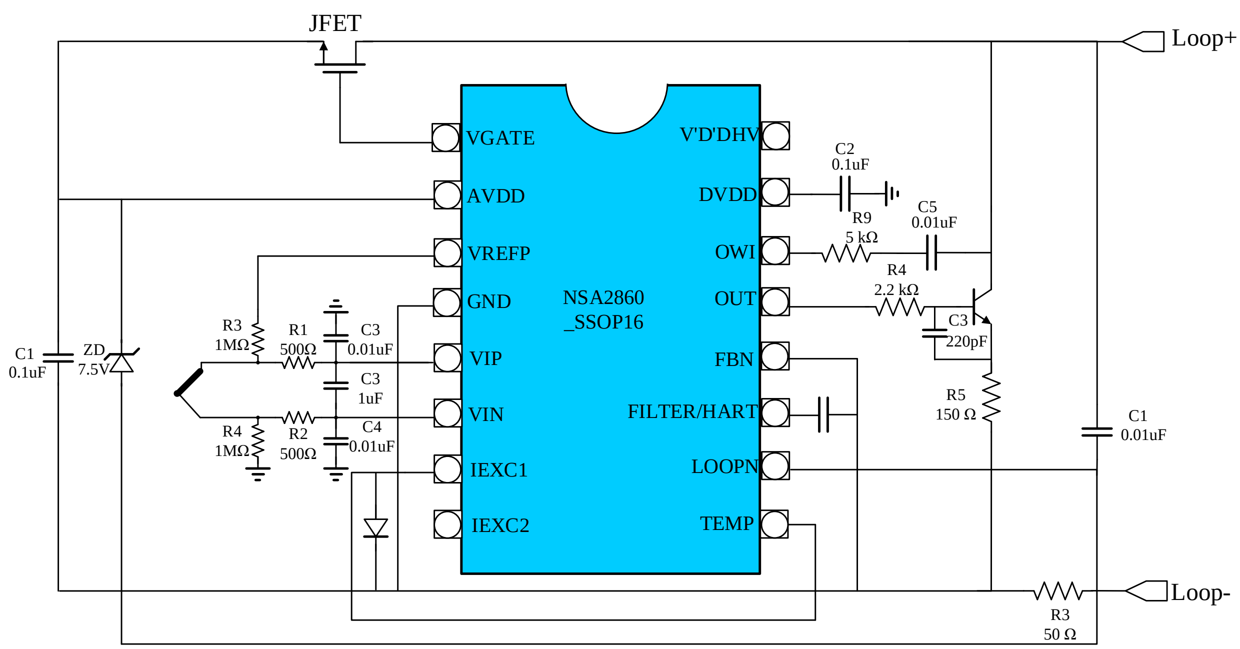


Figure 9.6 Thermocouple 4~20mA temperature transmitter

9.7. Application 7: 4~20mA 3-Ware RTD Temperature Transmitter

'VREF_DIS' set as 1, VREFP and VREFN is set externally.

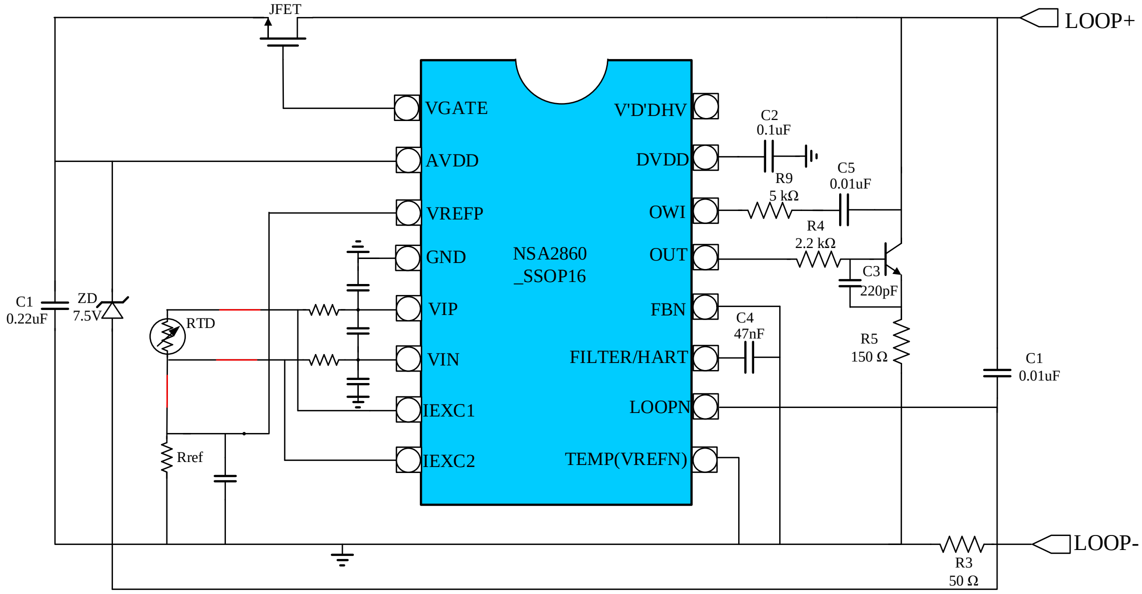


Figure 9.7 RTD temperature transmitter

9.8. Non-Isolated Pressure Transmitter with Hart

Use TSSOP20 package. The MCU communicate with NSA2860 through SPI interface. The HART modem (AD5700 here for example), modulate the loop current through a 470pF capacitor.

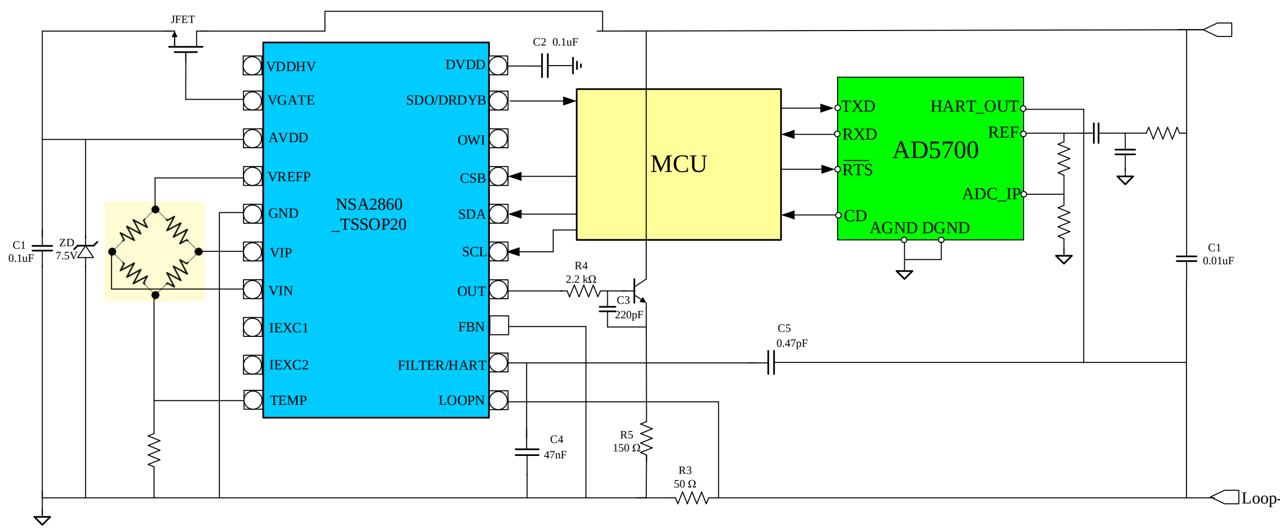


Figure 9.8 Non-isolated Pressure Transmitter with HART

10. Tape/Reel Information

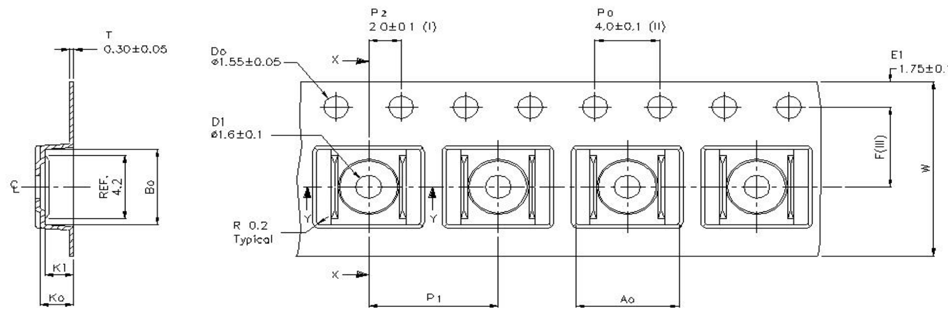


Figure 10.1 Tape/reel diagram for SSOP16

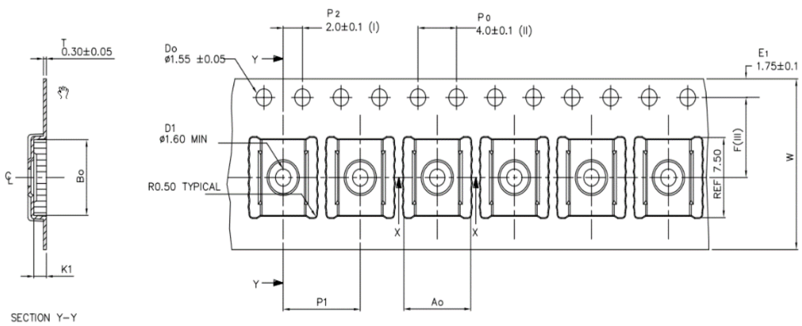
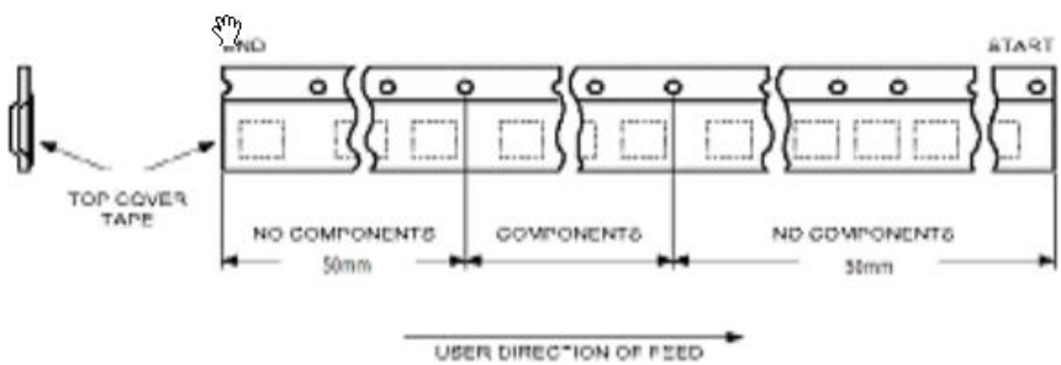


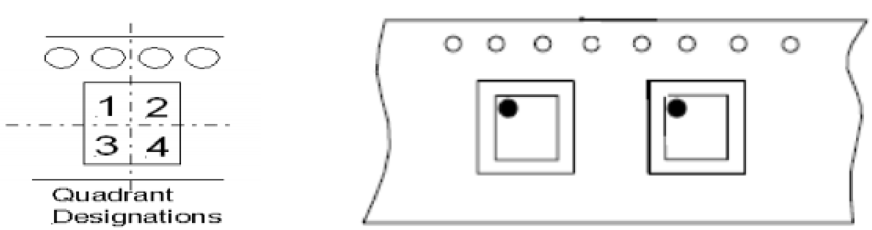
Figure 10.2 Tape/reel diagram for TSSOP20

Part No.	Package type	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)	F (mm)	P1 (mm)	W (mm)
NSA2860-SSOP16	SSOP16	6.5±0.1	5.3±0.1	2.2±0.1	1.9±0.1	5.5±0.1	8.0±0.1	12.0±0.3
NSA2860-TSSOP	TSSOP20	6.95±0.1	7.1±0.1	1.6±0.1	1.3±0.1	7.5±0.1	8.0±0.1	16.0±0.3

There is no component at the head and the tail of each tape/reel, where the space is 50cm, as shown in the following figure.



Pin 1 is located at the first quadrant, as shown in the following figure.



11. Ordering Information

Part Number	Temperature	MSL	Package Type	SPQ
NSA2860_SSOP16	-40℃ to 150℃	1	SSOP16	2500
NSA2860_TSSOP	-40℃ to 125℃	1	TSSOP20	2500

12. Revision History

Revision	Description	Date
1.0	Initial Version	2016/9/25
1.1	1. Fix some spell errors 2. Update the internal temperature sensor noise data 3. Update the external temperature sensor noise data 4. Add figure 7.8	2016/10/1
1.2	1. Modify the range of KTS from (-0.5, 0.5) to (-1,1) 2. Add order information	2017/1/10
1.3	1. Add tape/reel information	2017/3/21
1.4	Modify the format	2023/11/26

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