CA-IS305x Isolated CAN Transceivers

1 Features

- Meets ISO11898-2 requirements
- Dielectric withstand voltage of up to 5000 V_{RMS}
- Logic side I/O voltage range supports 2.5V ~ 5 V
- Signal transmission rate up to 1 Mbps
- High common mode transient immunity: 150 kV/μs (typical value)
- –40 V to 40 V bus fault protection
- Low loop delay:
  – 150 ns (typical value)
  – 210 ns (maximum value)
- Driver (TXD) dominant timeout function
- Thermal shutdown protection
- The bus is capable of supporting at most 110 nodes
- Non-interference bus without power-up nodes
- Temperature range: –40°C to 125°C
- Safety and regulation certificates:
  In conformity with DIN VDE V 0884-11(VDE V 0884-11) and DIN EN &IEC 62368-1 VDE certificates (under application)
  UL 1577 certified, 5 kV_{RMS} per minute
  IEC 62368-1 and IEC 61010-1 certifications, 5kV_{RMS} reinforced insulation
  EN 62368-1 and EN 61010-1 certifications, 5kV_{RMS} reinforced insulation
  GB 4943.1-2011 and GB 8898-2011 certifications, CQC reinforced insulation

2 Applications

- CAN bus
- Industrial field network
- Building and greenhouse environment control automation
- Security and protection system
- Transportation
- Medical treatment
- Telecommunication

3 Summary

CA-IS305x is an isolated controller area network (CAN) physical layer transceiver, which meets the technical specifications of ISO11898-2 requirements. The device takes an on-chip silicon dioxide (SiO_2) capacitor as an isolation layer, and a completely isolated interface is created between a CAN protocol controller and a physical layer bus and can be used with an isolated power supply to isolate noise and interference and prevent damage to sensitive circuits.

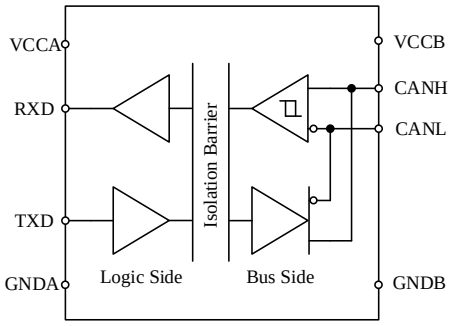
CA-IS305x can respectively provide differential receiving and transmitting capacities for the CAN protocol controller and the physical layer bus, and the signal transmission rate is up to 1 Mbps. Because of current-limiting, over-voltage, ground loss protection (–40V to 40V) and thermal shutdown functions, the device can prevent output short circuit, and the common mode voltage range is –12V to 12V.

CA-IS305x with the rated temperature range of –40°C to 125°C is packaged in a wide SOIC8 and a wide SOIC16.

Device information

Device model	Package	Package size (nominal value)
CA-IS3050 CA-IS3052	SOIC8-WB(G)	5.85 mm × 7.50 mm
	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3050	SOP8(U)	9.50 mm × 6.57 mm

Simplified functional block diagram



4 Ordering Guide

Tab. 4- 1 Valid Ordering Part Number

Model	VCC1（V）	VCC2（V）	Transmission speed (kbps)	Rated voltage (V)	Package
CA-IS3050G	2.5~5.5	4.5~5.5	1000	5000	SOIC8-WB
CA-IS3050W	2.5~5.5	4.5~5.5	1000	5000	SOIC16-WB
CA-IS3052G	2.5~5.5	4.5~5.5	1000	5000	SOIC8-WB
CA-IS3052W	2.5~5.5	4.5~5.5	1000	5000	SOIC16-WB
CA-IS3050U	2.5~5.5	4.5~5.5	1000	3750	SOP8

Contents

5 Revision history

Revision 0: initial version.

Revision 0 to Revision A

- Update 7.2 ESD Ratings
- Update 7.5 Insulation Specifications
  - DTI updated from 14um to 19um
- Update 7.7 Electrical Characteristics
  - CMTI typical value updated to 150kV/us
  - CMTI minimum value updated to 100kV/us

Revision A to Revision B

- Update 7.6 Safety-Related Certifications

Revision B to Revision C

- Add DUB8 package material number

Revision C to Revision D

- Update V_{ISO} of CA-IS3050U to 3750V
- Update V_{IOTM} of CA-IS3050U to 5300V

Revision D to Revision E

- Change tape data
- Add welding information

6 Pin Configuration and Functions

6.1 CA-IS3050

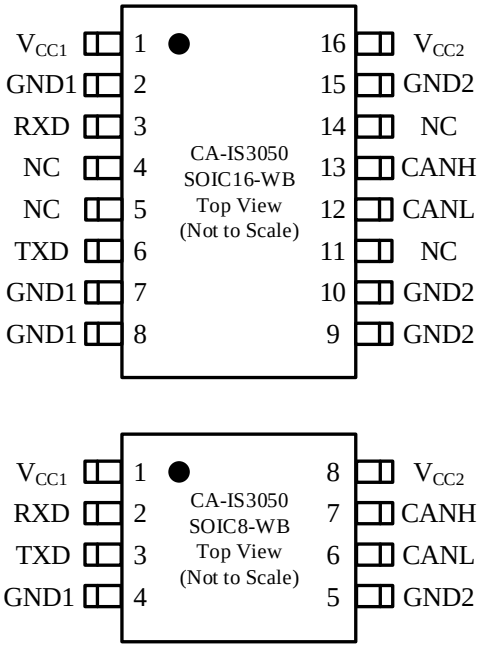


Figure. 6-1 Pin Configuration

Tab. 6-1 Pin Function Description

Pin name	Pin number		Type	Description
	SOIC16	SOIC8/SOP8		
V_{CC1}	1	1	Power supply	Logic side power input
GND1	2	–	Ground	Ground, logic side
RXD	3	2	Output	Receiver output data
NC	4	–	Nil	No connection, please do not connect the pin
NC	5	–	Nil	No connection, please do not connect the pin
TXD	6	3	Input	Driver input data
GND1	7	4	Ground	Ground, logic side
GND1	8	–	Ground	Ground, logic side
GND2	9	5	Ground	Ground, bus side
GND2	10	–	Ground	Ground, bus side
NC	11	–	Nil	No connection, please do not connect the pin
CANL	12	6	Input/output	Low-level CAN voltage input/output
CANH	13	7	Input/output	How-level CAN voltage input/output
NC	14	–	Nil	No connection, please do not connect the pin
GND2	15	–	Ground	Ground, bus side
V_{CC2}	16	8	Power supply	Bus side power input

6.2 CA-IS3052

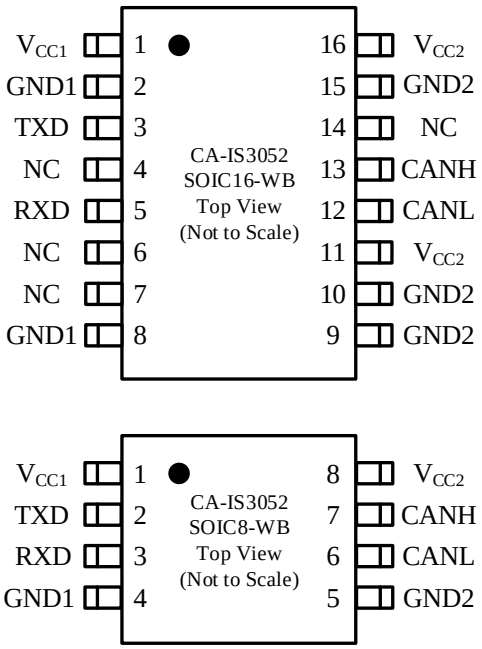


Figure. 6-2 Pin Configuration

Tab. 6-2 Pin Function Description

Pin name	Pin number		Type	Description
	SOIC16	SOIC8		
V_{CC1}	1	1	Power supply	Logic side power input
GND1	2	–	Ground	Ground, logic side
TXD	3	2	Input	Driver input data
NC	4	–	Nil	No connection, please do not connect the pin
RXD	5	–3	Output	Receiver output data
NC	6	–	Nil	No connection, please do not connect the pin
NC	7	–	Nil	No connection, please do not connect the pin
GND1	8	4	Ground	Ground, logic side
GND2	9	5	Ground	Ground, bus side
GND2	10	–	Ground	Ground, bus side
V_{CC2}	11	–	Power supply	Bus side power input
CANL	12	6	Input/output	Low-level CAN voltage input/output
CANH	13	7	Input/output	How-level CAN voltage input/output
NC	14	–	Nil	No connection, please do not connect the pin
GND2	15	–	Ground	Ground, bus side
V_{CC2}	16	8	Power supply	Bus side power input

7 Specifications

7.1 Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC1} or V_{CC2}	Power voltage[2]	–0.5	6.0	V
V_I	Logic side input voltage (TXD)	–0.5	V_{CC1} + 0.5[3]	V
V_{CANH} or V_{CANL}	Bus side voltage (CANH and CANL)	–40	40	V
I_O	Receiver output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	–65	150	°C

Notes:
1. Products may be permanently damaged when the rating is equal to or exceeds the absolute maximum rating. This is only maximum rating, but you cannot infer whether the products can normally work or not based on the conditions or under any other conditions exceeding the specifications as shown in technical standard operation chapters. The reliability of the products may be affected when the products work for a long time under the conditions exceeding the maximum rating.
2. All input/output logic voltage is measured relative to the logic side ground GND1, differential bus voltage is measured relative to the bus side ground GND2.
3. The maximum voltage shall not exceed 6V.

7.2 ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), in accordance with ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
	Charged device model (CDM), in accordance with JEDEC specification JESD22-C101, all pins[2]	±1500	

Notes:
1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Parameters			Minimum value	Typical value	Maximum value	Unit
V_{CC1}	Logic side power voltage		3	3.3	5.5	V
V_{CC2}	Bus side power voltage		4.5	5	5.5	V
V_I or V_{IC}	Bus pin voltage (single-terminal or common-mode)		–12		12	V
V_{IH}	Input high voltage	Driver (TXD)	2		V_{CC1} + 0.3	V
V_{IL}	Input low voltage	Driver (TXD)	–0.3		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	Output high-level current	Driver	–70			mA
		Receiver	–2			
I_{OL}	Output low-level current	Driver			70	mA
		Receiver			2.5	
T_A	Environmental temperature		–40		125	°C
T_J	Junction temperature		–40		150	°C
P_D	Total power consumption	V_{CC1} = 5.5V, V_{CC2} = 5.25V, T_A = 125°C, R_L = 60Ω, TXD input signals are 500 kHz square waves (duty ratio of 50%)			200	mW
P_{D1}	Logic side power consumption				25	mW
P_{D2}	Bus side power consumption				175	mW
$T_{J(shutdown)}$	Thermal shutdown temperature[1]		155	165	180	°C

Notes:
1. The operation at temperature exceeding the thermal shutdown temperature may affect the reliability of the device.

7.4 Thermal Information

Heat meter		SOIC8-WB	SOIC16-WB	SOP8	Unit
$R_{\theta JA}$	Heat resistance of chip junction to environment	110.1	86.5	73.3	°C/W
$R_{\theta JC(top)}$	Heat resistance of chip junction to shell (top)	51.7	49.6	63.2	°C/W

$R_{\theta JB}$	Heat resistance of chip junction to board	66.4	49.7	43.0	°C/W
ψ_{JT}	Characteristic parameters of chip junction to top	16.0	32.3	27.4	°C/W
ψ_{JB}	Characteristic parameters of chip junction to board	64.5	49.2	42.7	°C/W
$R_{\theta JC(bottom)}$	Heat resistance of chip junction to shell (bottom)	n/a	n/a	n/a	°C/W

7.5 Insulation Specifications

Parameters		Test conditions	Numerical value		Unit
			W/G	U	
CLR	External clearance[1]	Measure the shortest over-the-air distance from the input terminal to the output terminal	8	6.1	mm
CPG	External creepage[1]	Measure the shortest distance along the shell from the input terminal to the output terminal	8	6.8	mm
DTI	Distance through the insulation	Minimum internal clearance (internal distance)	19	19	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	In accordance with IEC 60664-1	I	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	I-III	
DIN V VDE V 0884-11:2017-01[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	560	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	400	V_{RMS}
		DC voltage	849	560	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method in accordance with IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	6250	5000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, after input/output safety test of the sub-category 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the sub-category 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1, routine test (100% production test) and preprocessing $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Contaminant level		2	2	
UL 1577					
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	3750	V_{RMS}

Notes:

1. Creepage distances and clearance requirements are applied in accordance with isolation standards of the applied specific devices. Pay attention to keep the creepage distance and the clearance distance of circuit board design to make sure that mounting pads of isolators on printed circuit boards will not shorten the distance. The creepage distances and the clearances on the printed circuit boards are equal in some cases. The technique like inserting grooves into the printed circuit boards is applied for helping to increase these specifications.
2. This standard is only applicable to safety electrical insulation within safety level. The safety level shall be guaranteed by the aid of appropriate protection circuits.
3. The test is implemented in the air or oil to determine the inherent surge immunity of isolation barriers.
4. Characterization charge is discharging charge (pd) caused by partial discharge.
5. All the pins on two sides of the gate are connected together to form double-terminal devices.

7.6 Safety-Related Certifications

VDE (applying)	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	UL1577 device program certification	Certified according to GB4943.1-2011 and certified according to GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017
	SOP8-G: 5000 VRMS； SOP16-W: 5000 VRMS	Reinforced insulation, maximum operating voltage of 600 V_{RMS}; (only applicable to the altitude of 5000m and below)	5000 V_{RMS} in accordance with reinforced insulation EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017, maximum operating voltage of 600 V_{RMS}
	Certificate number: E511334	Certificate number SOP8-G: CQC20001257122 SOP16-W: CQC20001257121	CB certificate number: JPTUV-112092； DE 2-028117 AK certificate number: AK 50476720 0001； AK 50476727 0001

7.7 Electrical Characteristics

Unless otherwise specified, all voltages refer to respective grounds, 3 V ≤ V_{CC1} ≤ 5.5 V, 4.5 V ≤ V_{CC2} ≤ 5.5 V. All minimum/maximum value specifications are applicable to the whole recommended operating range. Unless otherwise specified, all typical specifications are measured under the conditions of T_A = 25°C and V_{CC1} = V_{CC2} = 5 V.

Parameters			Test conditions	Minimum value	Typical value	Maximum value	Unit
Power supply current							
I_{CC1} Logic side power supply current			VI = 0 V or V_{CC1}, V_{CC1} = 3.3 V		1.8	2.8	mA
			VI = 0 V or V_{CC1}, V_{CC1} = 5 V		2.3	3.6	
I_{CC2} Bus side power supply current		Dominant	V_I = 0 V, R_L = 60 Ω		52	73	mA
		Recessive	V_I = V_{CC1}		8	12	
Driver							
$V_{O(D)}$ Bus output voltage (dominant)		CANH	V_I = 0 V, R_L = 60 Ω; see Figure 8-1 and Figure 8-2	2.9	3.4	4.5	V
		CANL		0.8		1.5	
$V_{O(R)}$ Bus output voltage (recessive)			V_I = 2 V, R_L = 60 Ω; see Figure 8-1 and Figure 8-2	2	2.5	3	V
$V_{OD(D)}$ Differential output voltage (dominant)			V_I = 0 V, RL = 60 Ω; see Figure 8-1, Figure 8-2 and Figure 8-3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω; see Figure 8-1, Figure 8-2 and Figure 8-3	1.4		3	V
$V_{OD(R)}$ Differential output voltage (recessive)			V_I = 3 V, RL = 60 Ω; see Figure 8-1 and Figure 8-2	–12		12	mV
			V_I = 3 V, non-load	–0.5		0.05	V
$V_{OC(D)}$ Common mode output voltage (dominant)			See Figure 8-7	2	2.5	3	V
$V_{OC(pp)}$ Common mode output voltage peak value					0.3		V
I_{IH} High-level input current, TXD input			V_I = 2 V			5	μA
I_{IL} Low-level input current, TXD input			V_I = 0.8 V	–5			μA
$I_{OS(SS)}$ Short-circuit steady-state output current			V_{CANH} = –12 V, CANL open circuit; see Figure 8-10	–105	–72		mA
			V_{CANH} = 12 V, CANL open circuit; see Figure 8-10		0.36	1	
			V_{CANL} = –12 V, CANH open circuit; see Figure 8-10	–1	–0.5		
			V_{CANL} = 12 V, CANH open circuit; see Figure 8-10		71	105	
CMTI (Common Mode Transient Immunity)			V_I = 0 V or V_{CC1}; see Figure 8-11	100	150		kV/μs
Receiver							
V_{IT+} Positive input threshold voltage					0.8	0.9	V
V_{IT-} Negative input threshold voltage				0.5	0.65		V
V_{HYS} Input voltage hysteresis window				100	125		mV
V_{OH} Output high voltage, V_{CC1} = 5 V			IOH = –4 mA; see Figure 8-6	V_{CC1} – 0.8	4.6		V
			IOH = –20 μA; see Figure 8-6	V_{CC1} – 0.1	5		
V_{OH} Output high voltage, V_{CC1} = 3.3 V			IOH = –4 mA; see Figure 8-6	V_{CC1} – 0.8	3.1		V
			IOH = –20 μA; see Figure 8-6	V_{CC1} – 0.1	3.3		
V_{OL} Output low voltage			IOH = 4 mA; see Figure 8-6		0.2	0.4	V
			IOH = 20 μA; see Figure 8-6		0	0.1	
C_I CANH and CANL ground input capacitance			TXD is 3V, VI = 0.4xsin(2πft) + 2.5 V, f = 1MHz		13		pF
C_{ID} Input differential capacitance			TXD is 3V, VI = 0.4xsin(2πft), f = 1MHz		5		pF
R_{IN} CANH and CANL input capacitance			TXD is 3V	15	30	40	kΩ
R_{ID} Differential input resistance			TXD is 3V	30		80	kΩ
$R_{I(m)}$ Input resistance matching (1 – [$R_{IN(CANH)}$ / $R_{IN(CANL)}$])			VCANH = VCANL	–5%	0%	5%	
CMTI (common mode transient immunity)			VI = 0 V or VCC1; see Figure 8-11	100	150		kV/μs

7.8 Sequential Characteristics: Device

Unless otherwise specified, all voltages refer to respective grounds, 3 V ≤ V_{CC1} ≤ 5.5 V, 4.5 V ≤ V_{CC2} ≤ 5.5 V. All minimum/maximum value specifications are applicable to the whole recommended operating range. Unless otherwise specified, all typical specifications are measured under the conditions of T_A = 25°C and V_{CC1} = V_{CC2} = 5 V.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
t_{loop1}	Total loop delay, driver input to receiver output, recessive to dominant	see Figure 8-8	110		210	ns
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive		110		210	ns

7.9 Sequential characteristics: Driver and Receiver

Unless otherwise specified, all voltages refer to respective grounds, 3 V ≤ V_{CC1} ≤ 5.5 V, 4.5 V ≤ V_{CC2} ≤ 5.5 V. All minimum/maximum value specifications are applicable to the whole recommended operating range. Unless otherwise specified, all typical specifications are measured under the conditions of T_A = 25°C and V_{CC1} = V_{CC2} = 5 V.

Parameters		Test conditions	Minimum value	Typical value	Maximum value	Unit
Driver						
t_{PLH}	Propagation delay, output is changed from recessive to dominant	see Figure 8-4	35	75	130	ns
t_{PHL}	Propagation delay, output is changed from dominant to recessive		35	55	100	
t_r	Differential output signal rise time			40	60	
t_f	Differential output signal fall time			40	60	
t_{TXD_DTO}[1]	Dominant timeout period	C_L = 100 pF; see Figure 8-9	300	450	700	μs
Receiver						
t_{PLH}	Propagation delay, output is changed from low level to high level	see Figure 8-6	70	110	140	ns
t_{PHL}	Propagation delay, output is changed from high level to low level		55	80	100	
t_r	Output signal rise time				6	
t_f	Output signal fall time				6	

Remarks:

1. Once the time of the driver entering the dominant status exceeds t_{TXD_DTO}, the driver is turned off by the dominant timeout function, so that the bus is released to be recessive and prevented from local deadlock and constant dominant state. The driver can restore dominant transmission functions only after entering the recessive status.

8 Test Circuit

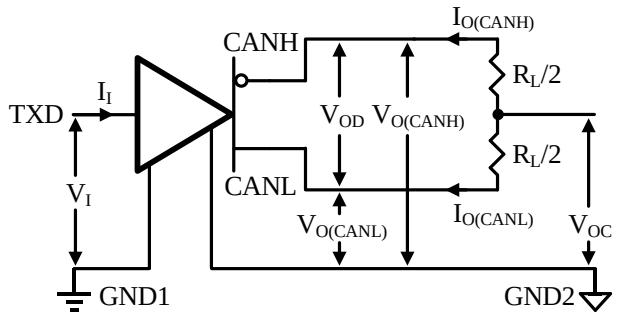


Figure. 8-1 Driver Voltage and Current Definition

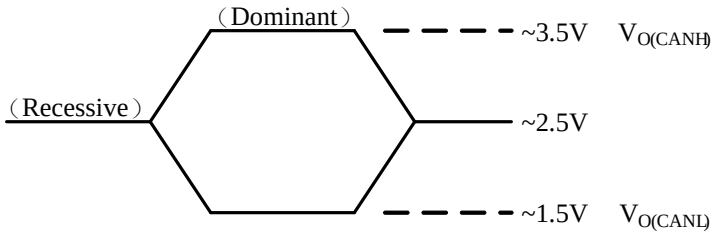


Figure. 8-2 Bus Logic State Voltage Definition

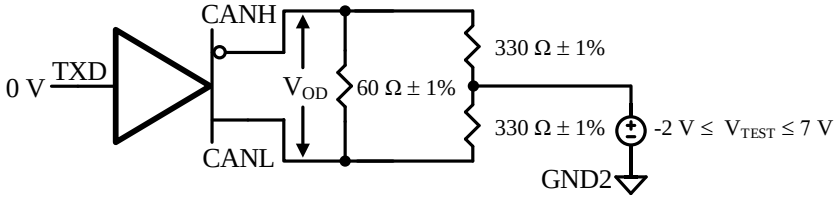
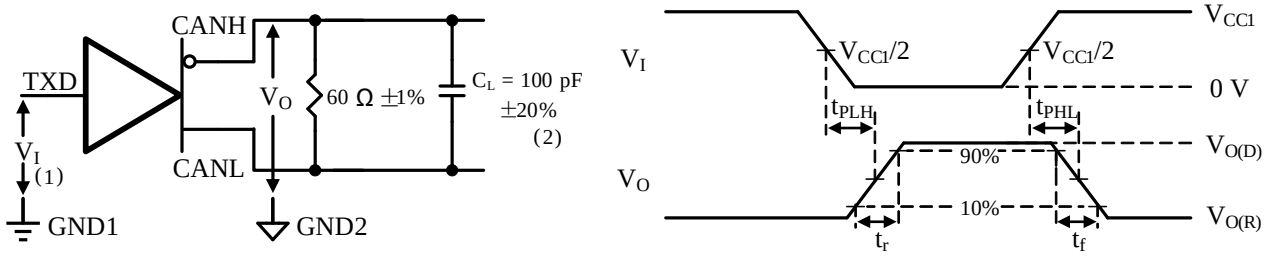


Figure. 8-3 Driver V_{OD} Common Mode Load Voltage Measuring Circuit



Notes

1. Input pulse generated by signal sources has the following requirements: pulse repetition rate PRR≤125 kHz, duty ratio of 50%, rise time t_r≤6 ns, fall time t_f≤6 ns, output impedance Z_O = 50 Ω;
2. Load capacitance C_L includes the parasitic capacitance of an instrument and a fixture.

Figure. 8-4 Driver Measuring Circuit and Voltage Waveform

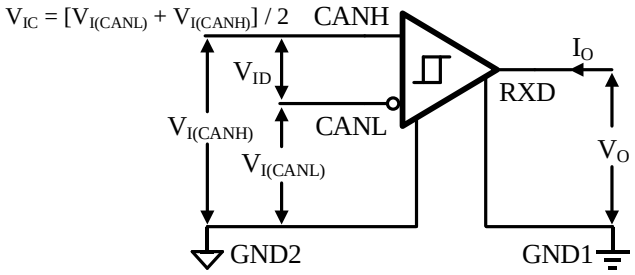
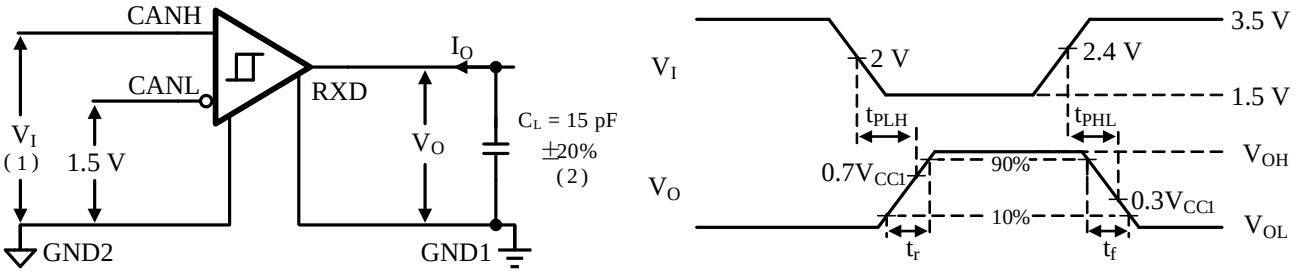


Figure. 8-5 Receiver Voltage and Current Definition



Notes:

1. Input pulse generated by signal sources has the following requirements: pulse repetition rate PRR≤125 kHz, duty ratio of 50%, rise time t_r≤6 ns, fall time t_f≤6 ns, output impedance Z_O = 50 Ω;
2. Load capacitance C_L includes the parasitic capacitance of an instrument and a fixture.

Figure. 8-6 Receiver Measuring Circuit and Voltage Waveform

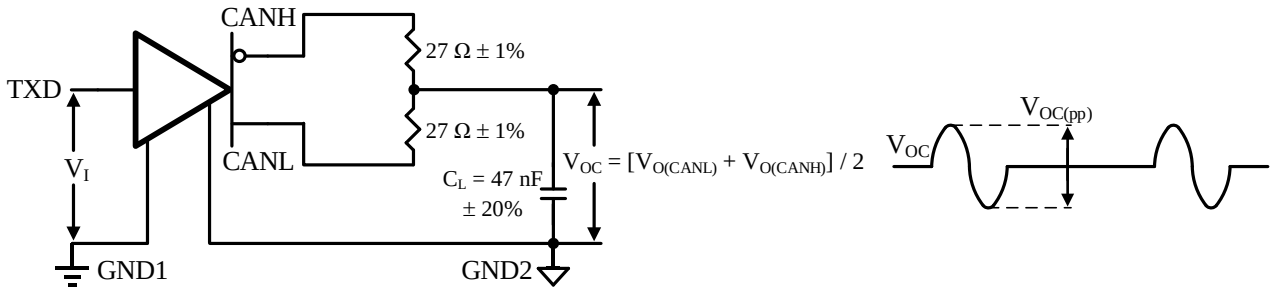


Figure. 8-7 Common Mode Output Voltage Peak Value Measuring Circuit and Waveform

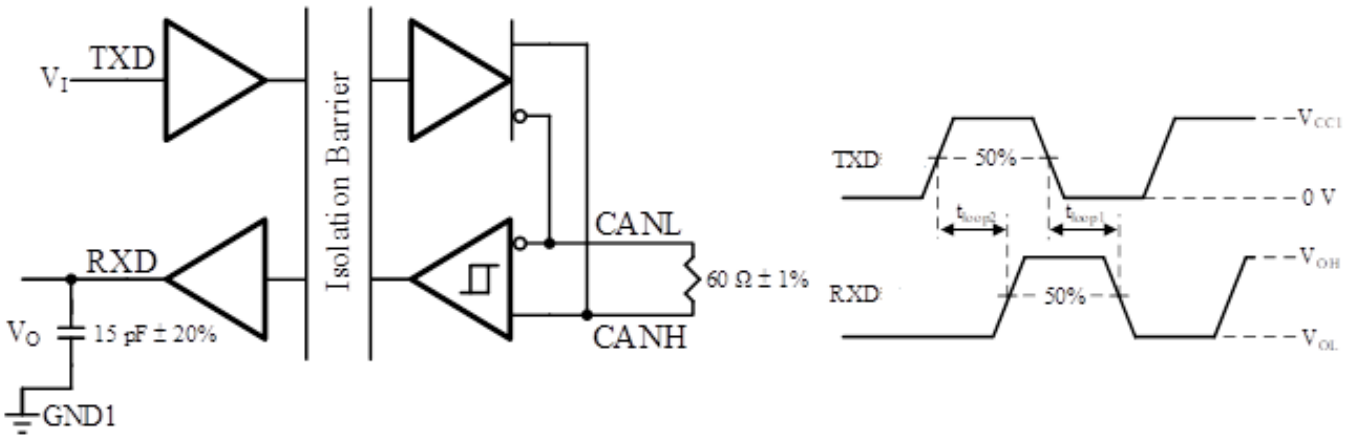
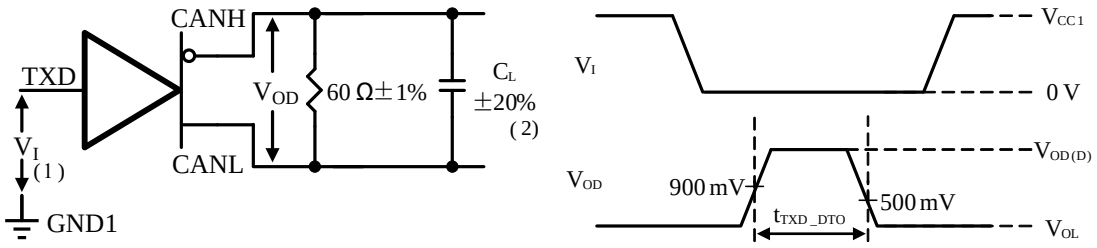


Figure. 8-8 t_{loop} Measuring Circuit and Voltage Waveform



Notes:

1. Input pulse generated by signal sources has the following requirements: rise time $t_r \leq 6$ ns, fall time $t_f \leq 6$ ns, output impedance $Z_O = 50\ \Omega$;
2. Load capacitance C_L includes the parasitic capacitance of an instrument and a fixture.

Figure. 8-9 Dominant Timeout Function Measuring Circuit and Voltage Waveform

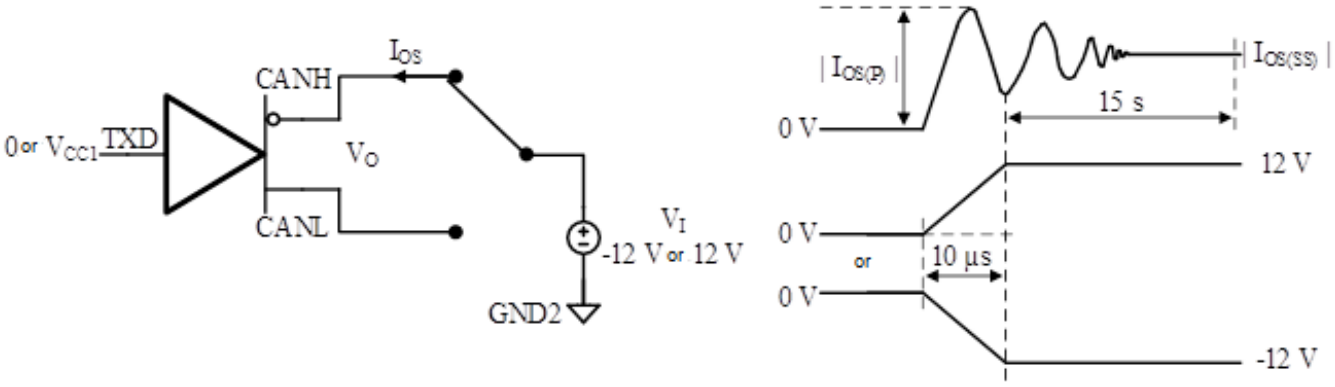


Figure. 8-10 Output Short-circuit Current Measuring Circuit and Waveform

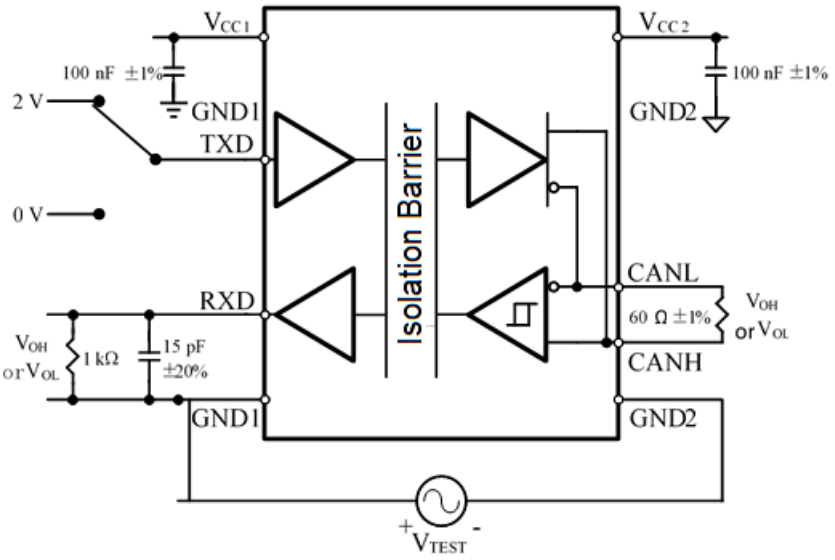


Figure. 8-11 Common Mode Transient Immunity Measuring Circuit

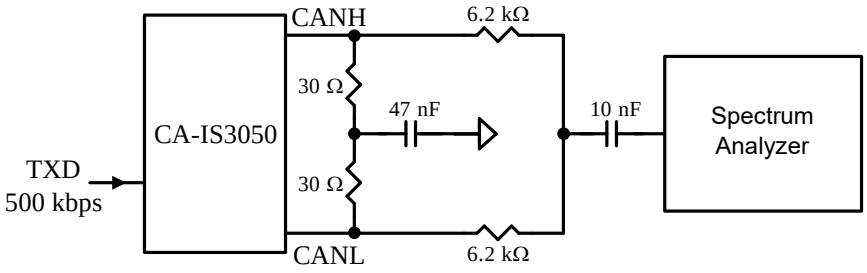


Figure. 8-12 Electromagnetic Radiation Measuring Circuit

9 Functional Description

9.1 Overview

CA-IS305x is an isolated controller area network (CAN) physical layer transceiver, supports 5 kV_{RMS} isolated withstand voltage grade and integrates the dominant timeout function and thermal shutdown protection, and common mode transient immunity is higher than 150 kV/μs. The logic side of the device can be powered by a 3.3V power supply, the bus side of the device can be powered by a 5V power supply, and the device is quite applicable to industrial control locations with harsh environments. This is because that in the industrial control locations, 3.3V power supply rails are generally used on the logic side to supply power for low-voltage equipment such as a micro-controller, so that power consumption is reduced, and 5V power supply rails are usually used on the bus side to guarantee high signal-noise ratio.

9.2 CAN Bus Status

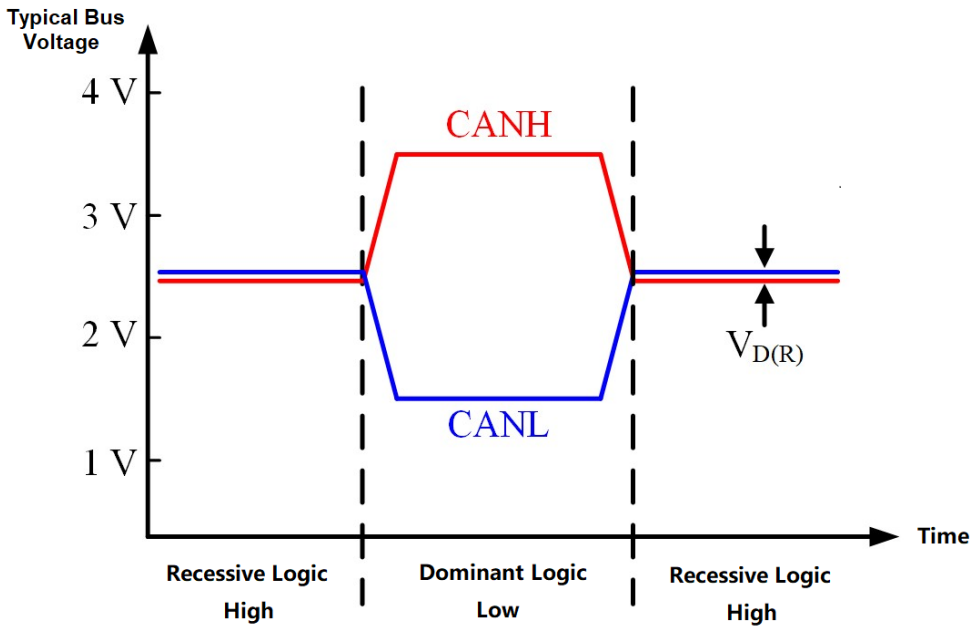


Figure. 9-1 CAN Bus Status Typical Waveform

The CAN bus has a dominant status and a recessive status: the bus is in the dominant status when the differential voltage between CANH and CANL is higher than 0.9V; the bus is in the recessive status when the differential voltage between CANH and CANL is lower than 0.5V. When the bus is in the dominant status, the pin CANH is in a high-level status, and the pin CANL is in a low-level status; when the bus is in the recessive status, both the pin CANH pin and the pin CANL are in a high-impedance status. The typical bus voltage waveform is as shown in Figure 9-1.

9.3 Protection Functions

9.3.1 Signal Isolation

Signal isolation of CA-IS305x is implemented by a digital isolator based on a capacitance isolation scheme, input signals are modulated to high frequency by the digital isolator on the logic side by means of On-Off Key (OOK), and received signals are recovered by the on-chip silicon dioxide capacitor with an isolated withstand voltage function on parts of circuits of the digital isolator on the bus side and then converted into a level meeting the standards, wherein the level is outputted to the CAN bus. Similarly, the level on the bus side is processed by circuits on the bus side, modulated to high frequency by the digital isolator, transmitted back to the logic side, then demodulated and recovered on the logic side and outputted to RXD. Grounds on the logic side and the bus side can be completely separated, the isolated withstand voltage grade up to 5kV_{RMS} is achieved by the on-chip silicon dioxide capacitor, and integrity and safety of signal transmission between the micro-controller and the high-voltage bus are guaranteed in actual use.

9.3.2 Dominant Timeout Function

Owing to the dominant timeout function of CA-IS305x, TXD is prevented from being constantly pulled to the low level due to software or hardware faults, thereby preventing the bus from constantly entering the dominant status and accordingly being locked (communication of the whole network is blocked). The dominant timeout function is triggered by a counter during occurrence of negative edges of TXD input signals, the transceiver will be turned off, and the bus is released to enter the recessive status when the duration of the low level of TXD is longer than the dominant timeout period t_{TXD_DTO}. The counter will be set during the positive edges of the TXD input signals.

9.3.3 Thermal Shutdown Protection

CA-IS305x integrates the thermal shutdown protection function and can protect internal circuits of the device under over-temperature conditions. The driver will be turned off if the junction temperature of the device exceeds thermal shutdown temperature $T_{J(shutdown)}$, so that the signal transmission path from TXD to the bus is blocked, and typical thermal shutdown temperature is 165°C. The driver will be enabled again after the junction temperature of the device is lower than the thermal shutdown temperature.

9.3.4 Current-Limiting Protection

CA-IS3050 integrates the current-limiting protection function and can prevent the bus side from having output short-circuit and causing transient over-current of the power supply or grounds, thereby preventing damage to the device. Once current limiting protection happens, high current will be generated to bring great loss.

9.4 Device Function Truth Table

Tab. 9-1 Truth Table Abbreviations

Letters	Description
H	High level
L	Low level
X	Unrelated
Z	High-impedance (off)
?	Uncertain
Open	Open circuit

Tab. 9-2 Driver Function Truth Table

Input	Output		Bus status
TXD	CANH	CANL	
L	H	L	Dominant
H or Open	Z	Z	Recessive

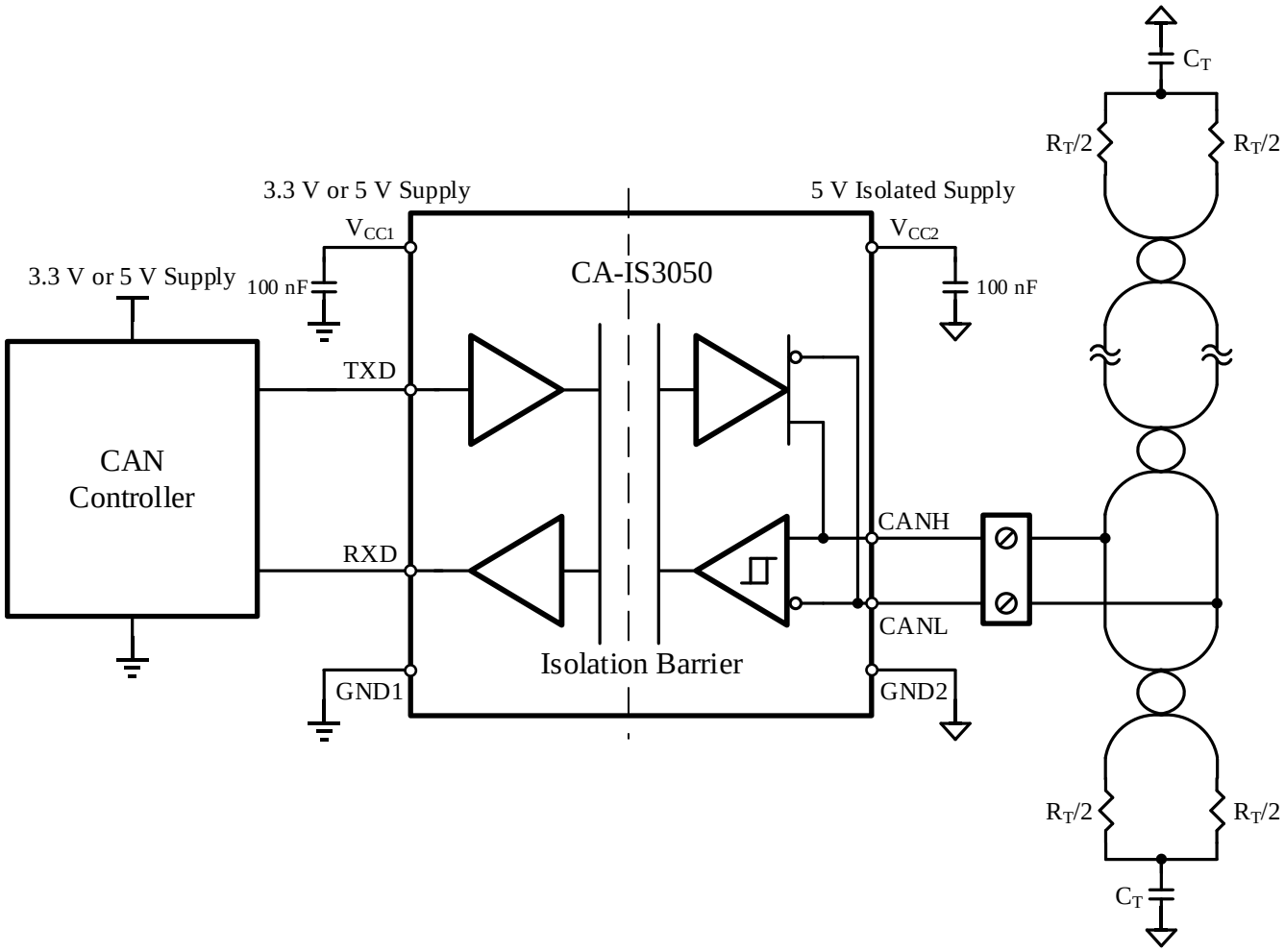
Tab. 9-3 Receiver Function Truth Table

CAN bus differential input $V_{ID} = V_{CANH} - V_{CANL}$	Bus status	RXD
$0.9\ V \le V_{ID}$	Dominant	L
$0.5\ V < V_{ID} < 0.9\ V$	?	?
$V_{ID} \le 0.5\ V$	Recessive	H
Open ($V_{ID} \approx 0\ V$)	Open	H

Tab. 9-4 Transceiver Function Truth Table

Driver				Receiver		
Input	Output		Bus status	Differential input $V_{ID} = V_{CANH} - V_{CANL}$	RXD output	Bus status
TXD	CANH	CANL				
L[1]	H	L	Dominant	$0.9\ V \le V_{ID}$	L	Dominant
H	Z	Z	Recessive	$0.5\ V < V_{ID} < 0.9\ V$	?	?
Open	Z	Z	Recessive	$V_{ID} \le 0.5\ V$	H	Recessive
X	Z	Z	Recessive	Open	H	Recessive

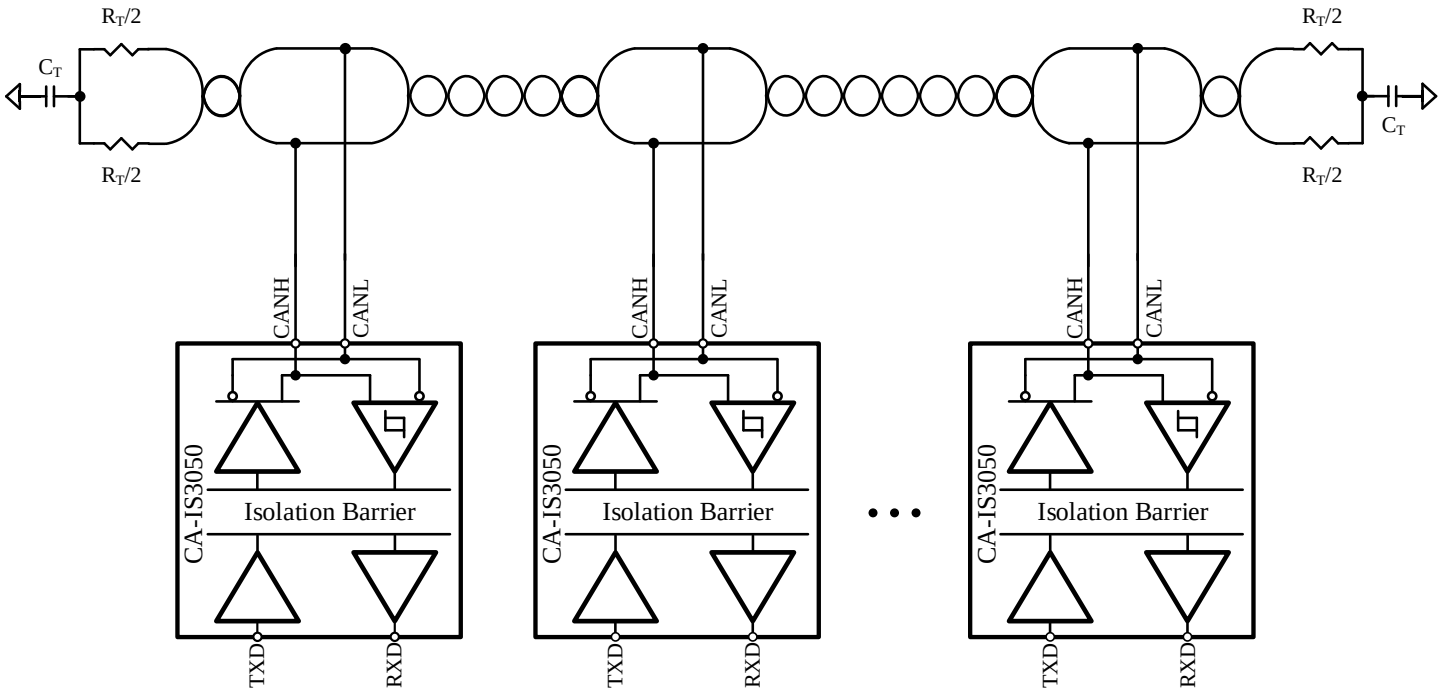
10 Application Information



Notes:

1. Terminal resistance R_T shall be equal to the characteristic impedance of the cable.

Figure. 10-1 Typical Isolated CAN Nodes Based on CA-IS305x



Notes:

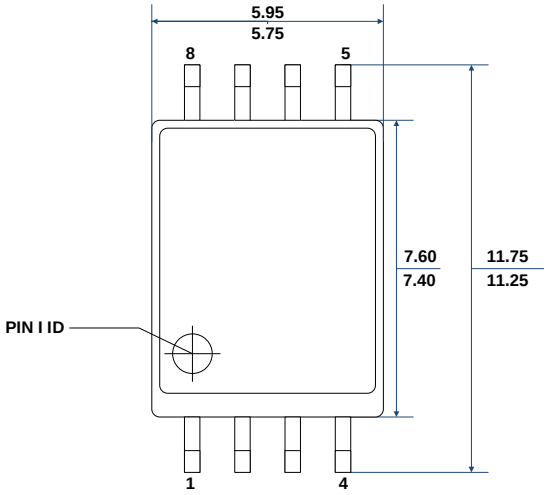
1. Terminal resistance R_T shall be equal to the characteristic impedance of the cable;
2. CA-IS305x can support at most 110 nodes.

Figure. 10-2 Typical CAN Bus Based on CA-IS305x

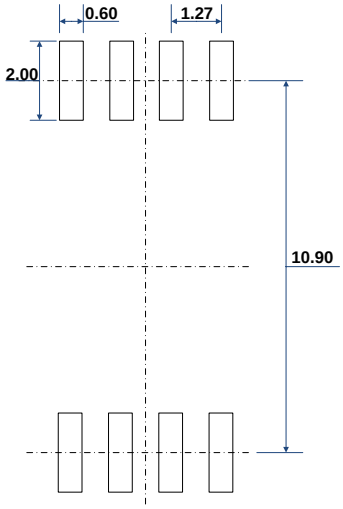
11 Package Information

11.1 SOIC8 Wide Overall Dimension

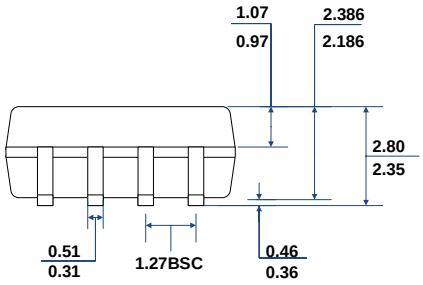
The following diagrams illustrate the dimension diagram of CA-IS305x series isolated CAN transceivers packaged in SOIC8 wide package and the suggested pad dimension diagram. Dimensions are in millimeters.



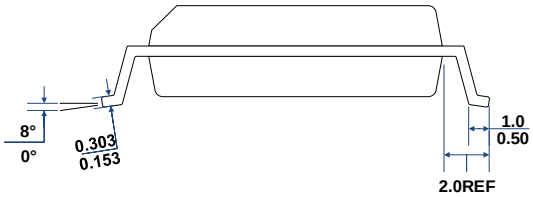
TOP VIEW



RECOMMENDED LAND PATTERN



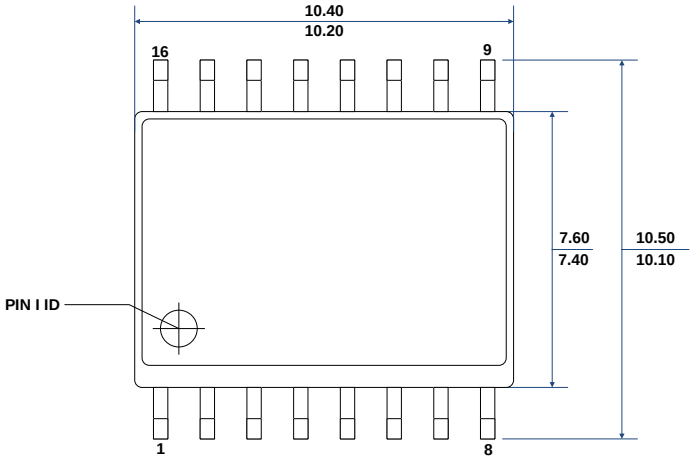
FRONT VIEW



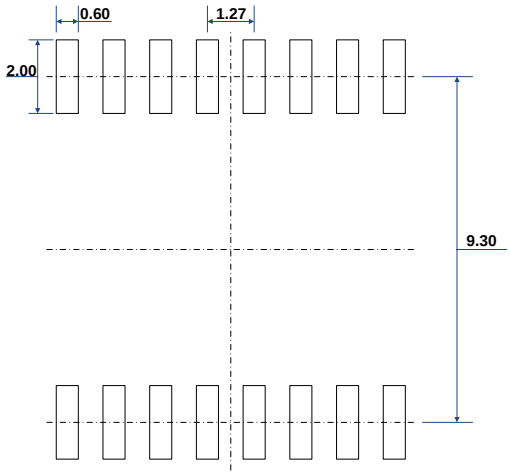
LEFT-SIDE VIEW

11.2 SOIC16 Wide Overall Dimension

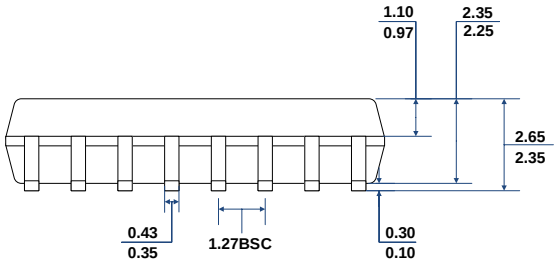
The following diagrams illustrate the dimension diagram of CA-IS305x series isolated CAN transceivers packaged in SOIC16 wide package and the suggested pad dimension diagram. Dimensions are in millimeters.



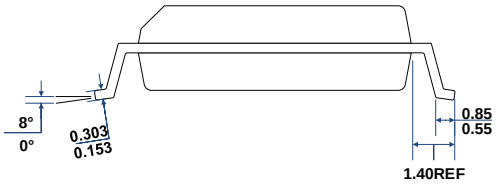
TOP VIEW



RECOMMENDED LAND PATTERN

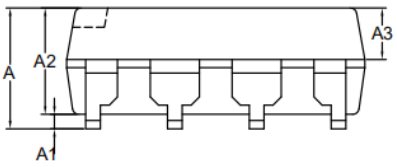


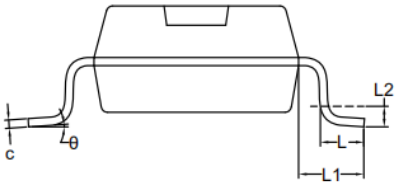
FRONT VIEW

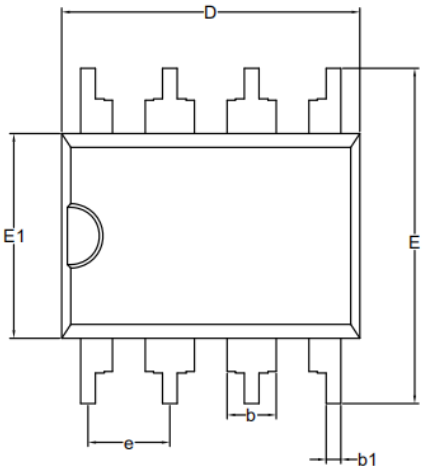


LEFT-SIDE VIEW

11.3 SOP8 Overall Dimension







SYMBOL	MIN	NOM	MAX
A	3.48	——	4.85
A_1	0.38	——	——
A_2	3.10	3.30	3.50
A_3	1.40	1.50	1.60
b	1.14	1.52	1.78
b_1	0.39	——	0.55
c	0.20	——	0.34
D	9.00	9.20	9.40
E	10.10	10.40	10.70
E1	6.15	6.35	6.55
e	2.54 BSC		
L	1.15	1.25	1.45
L1	2.03 REF		
L2	0.635 REF		
θ	0°	4°	8°

12 Welding Information

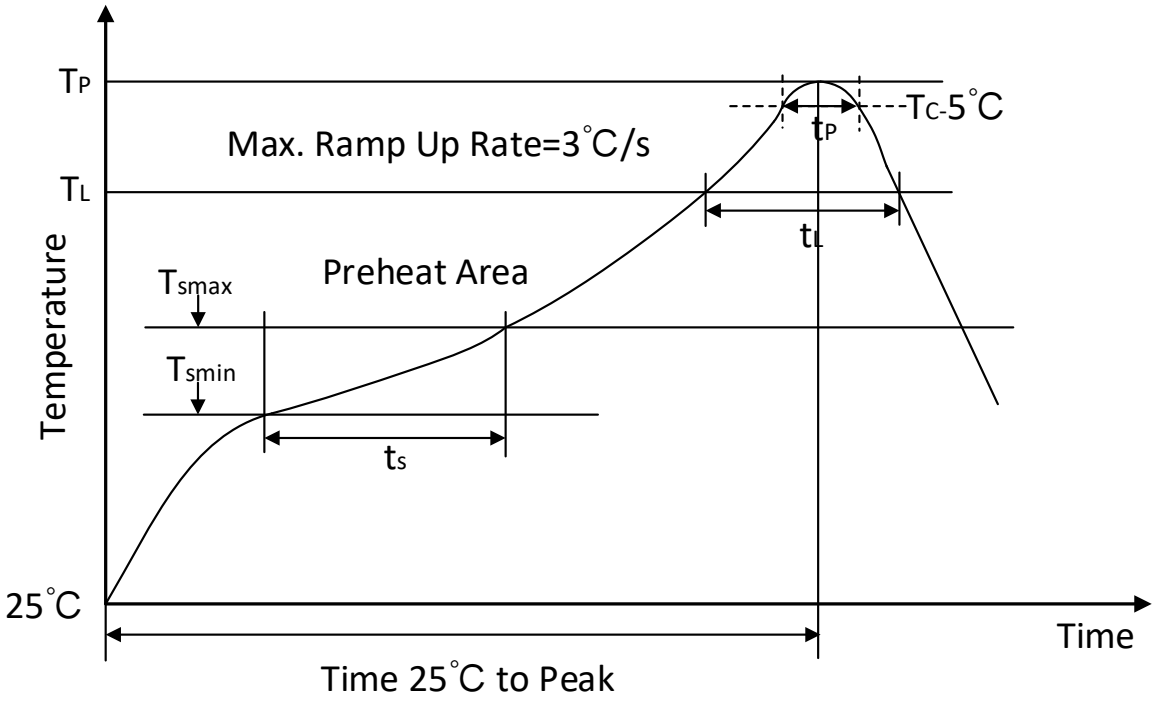


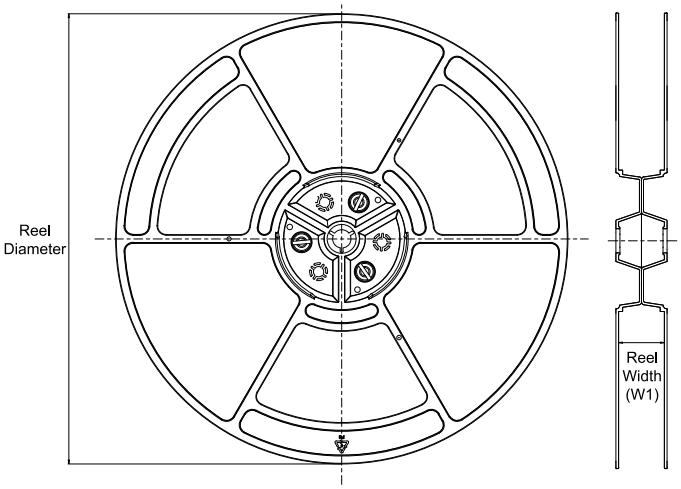
Figure. 12-1 Welding Temperature Curve

Tab. 12-1 Welding Temperature Parameters

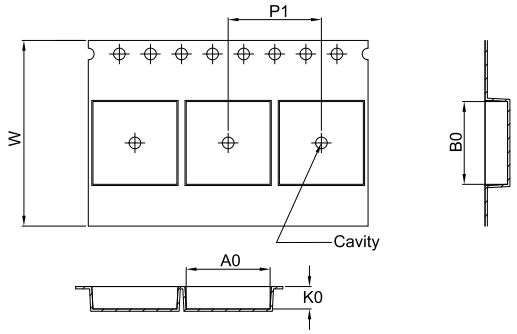
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

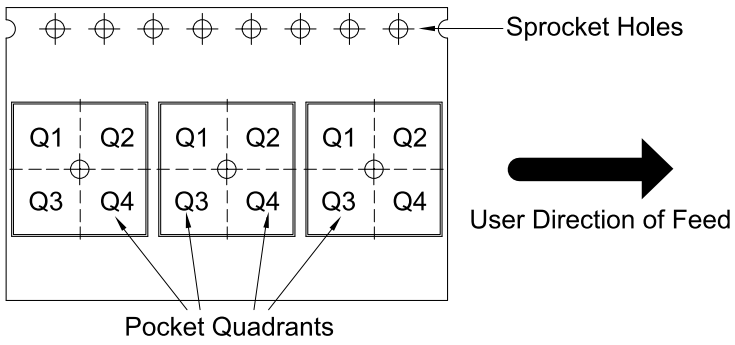


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3050W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3050G	SOIC	G	8	1000	330	16.4	12.05	6.15	3.3	16.0	16.0	Q1
CA-IS3052W	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3052G	SOIC	G	8	1000	330	16.4	12.05	6.15	3.3	16.0	16.0	Q1
CA-IS3050U	SOP	U	8	1000	330	24.4	10.9	10.01	5.85	16.0	24.0	Q1

Important Statement

The above information is for reference only and intended to help Chipanalog customers with design, research and development. Chipanalog reserves the rights to change the above information due to technological innovation without advance notice.

All Chipanalog products pass ex-factory test. As for specific practical applications, customers need to be responsible for evaluating and determining whether the products are applicable or not by themselves. Chipanalog's authorization for customers to use the resources are only limited to development of the related applications of the Chipanalog products. In addition to this, the resources cannot be copied or shown, and Chipanalog is not responsible for any claims, compensations, costs, losses, liabilities and the like arising from the use of the resources.

Trademark information

Chipanalog Inc.® and Chipanalog® are registered trademarks of Chipanalog.

http://www.chipanalog.com