Features

- AEC-Q100 qualified
- ±50mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift
  ±0.12mV (max), ±1µV/°C (max)
- Fixed gain: 41
- Low gain error and drift
  ±0.3% (max), ±30ppm/°C (max)
- Low nonlinearity and drift:
  0.03%, 1ppm/°C (typical)
- Safety-related certifications:
  7071V$_{PK}$ reinforced isolation per DIN VDE V 0884-17: 2021-10
  5.0kV$_{RMS}$ isolation for 1 minute per UL1577
- High CMTI: 150kV/µs (typical)

Applications

- Shunt-resistor-based current sensing in:
  – Motor drives
  – Frequency inverters
  – Uninterruptible power supplies

Description

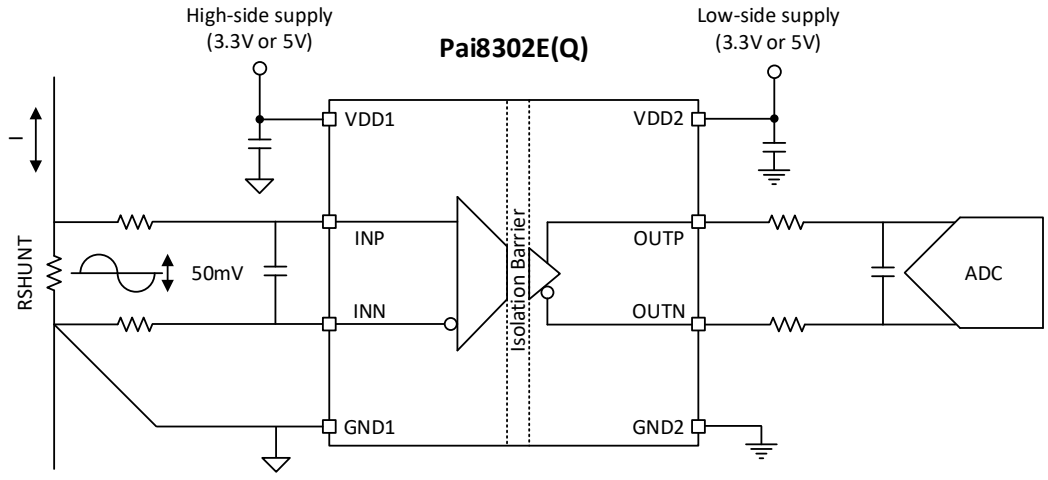
The Pai8302E(Q) is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5kV$_{RMS}$ according to VDE V 0884-17 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the Pai8302E(Q) is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings.

The Pai8302E(Q) is specified over the extended industrial temperature range of –40°C to 125°C.

PART NUMBER	PACKAGE	BODY SIZE
Pai8302E(Q)-W5R	WB SOIC-8	5.85mm*7.5mm

Simplified Schematic



1 Pin Configurations and Functions

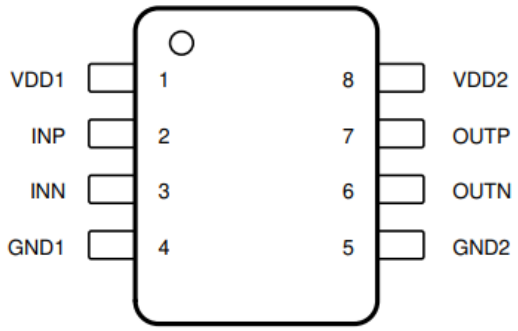


Fig1. Pin Configuration

Pin Functions

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	VDD1	High-side power	High-side power supply, 3.0V to 5.5V relative to GND1.
2	INP	Analog input	Noninverting analog input.
3	INN	Analog input	Inverting analog input.
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply, 3.0V to 5.5V.

2 Specifications

2.1 Absolute Maximum Ratings(1)

Parameter	Symbol	MIN	MAX	UNIT
Power supply	VDD1 to GND1	-0.3	6.5	V
	VDD2 to GND2	–0.3	6.5	V
Input voltage	INP, INN	GND1-6	VDD1+0.5	V
Output voltage	OUTP, OUTN	GND2-0.5	VDD2+0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Junction temperature, T_J	T_J	-40	150	°C
Storage temperature, T_{stg}	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 ESD Ratings

Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22- C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

2.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	MIN	MAX	UNIT
High side power supply	VDD1 to GND1	3.0	5.5	V
Low side power supply	VDD2 to GND2	3.0	5.5	V
Differential input voltage before clipping output	VIN = VINP – VINN	-64	64	mV
Specified linear differential input full-scale	VIN = VINP – VINN	-50	50	mV
Absolute common-mode input voltage(1)	(VINP + VINN) / 2 to GND1	-2	VDD1	V
Operating common-mode input voltage	(VINP + VINN) / 2 to GND1	-0.16	VDD1-2.1	
T_A	Ambient Temperature	-40	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the Absolute Maximum Ratings table.

2.4 Thermal Information

Symbol	Parameter	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43	°C/W

2.5 Insulation Specifications

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Test Condition	VALUE	UNIT
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
Material group		According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	

DIN V VDE V 0884-17 (VDE V 0884-17): 2021-10(2)

Parameter	Description	Test Condition	VALUE	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	1.2/50 µs waveform per IEC 62368-1 $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
$V_{pd(m)}$	Method a, after Input-Output safety test subgroup 2/3	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	2545	V_{PK}
	Method a, after Input-Output safety test subgroup 1	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	3394	V_{PK}
	Method b1, at routine test (100% production) and preconditioning (type test) (4)	Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s partial discharge ≤ 5pC	3977	V_{PK}
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4*sin(2πft), f =1MHz	~1.2	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500V at T_S =150°C	$> 10^9$	Ω
Pollution degree			2	
Climatic category			40/125/21	

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier are tied together, creating a two-pin device.

UL 1577

Parameter	Description	Test Condition	VALUE	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60 sec.(qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1 sec (100% production)	5000	V_{RMS}

2.6 Safety-Related Certifications

CQC	Certified according to GB 4943.1-2011	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate 1000 V_{RMS} maximum working voltage.	File: CQC23001405186
UL	Recognized under UL 1577 Component Recognition Program	Single protection, 5000V_{RMS}	File: E494497
VDE	Certified according to DIN V VDE V 0884-17:2021-10, and DIN EN 60950-1 (VDE 0805 Teil 1):2014-08	Reinforced Insulation Maximum Transient Isolation voltage, 7071 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121V_{PK}. Maximum Surge Isolation Voltage, 10000 V_{PK}	File: 40056491

2.7 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

Parameter	Description	Test Condition	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$=85.4°C/W, T_J=150°C, T_A =25°C, VDD1=VDD2=5.5V	-	-	266	mA
		$R_{\theta JA}$=5.4°C/W, T_J=150°C, T_A=25°C, VDD1=VDD2=3.6V	-	-	408	mA
P_S	Safety supply power(1)	$R_{\theta JA}$=85.4°C/W, T_J=150°C, T_A=25°C			1463	mW
T_S	Maximum Safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_J(max) = T_S = T_A + R_{\theta JA} \times P_S$, where $T_J(max)$ is the maximum allowed junction temperature.$P_S = I_S \times VI$, where VI is the maximum input voltage.

2.8 Electrical Characteristics

Minimum and maximum specifications of the Pai8302E(Q) apply from T_A=–40°C to +125°C, VDD1=3.0V to 5.5V, VDD2=3.0V to 5.5V, INP=–50mV to +50mV, and INN=GND1=0V; typical specifications are at T_A =25°C, VDD1=5V, and VDD2=3.3V (unless otherwise noted).

Parameter		Test Condition	MIN	TYP	MAX	UNIT
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output			±64		mV
V_{CMov}	Common-mode overvoltage detection level		VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			95		mV
V_{OS}	Input offset voltage(1)	initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1	–0.12	±0.01	0.12	mV
TCV_{OS}	Input offset drift(1)		-1	±0.1	1	µV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		-90		dB
		f_{IN} =10KHz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		-90		dB
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275kHz		25		pF
C_{IND}	Differential input capacitance	f_{IN} = 275kHz		20		pF
R_{IN}	Single-ended input resistance	INN = GND1		8		kΩ
R_{IND}	Differential input resistance			9		kΩ
I_{IB}	Input bias current	INP=INN=GND1, I_{IB}=(I_{IBP}+I_{IBN})/2	-26	-20	-14	uA
IIO	Input offset current			±20		nA

Electrical Characteristics (continued)

Minimum and maximum specifications of the Pai8302E(Q) apply from T_A=–40°C to +125°C, VDD1=3.0V to 5.5V, VDD2=3.0V to 5.5V, INP=–50mV to +50mV, and INN=GND1=0V; typical specifications are at T_A =25°C, VDD1=5V, and VDD2=3.3V (unless otherwise noted).

Parameter		Test Condition	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Normal gain			41		V/V
E_G	Gain error(1)	initial, at T_A = 25°C	–0.3%	±0.04%	0.3%	
TCE_G	Gain error drift(1)		–30	±15	30	ppm/°C
	Nonlinearity (1)		-0.03%	±0.01%	0.03 %	
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	V_{IN}=0.1V, f_{IN}=10kHz, BW=100kHz		-85		dB
	Output noise	V_{INP}=V_{INN}=GND1, BW=100kHz		260		uV_{RMS}
SNR	Signal-to-noise ratio	V_{IN}=0.1V, f_{IN}=1kHz, BW=10kHz	80	85		dB
		V_{IN}=0.1V, f_{IN}=10kHz, BW=100kHz		72		dB
PSRR	Power-supply rejection ratio(2)	PSRR vs VDD1, at DC		-100		dB
		PSRR vs VDD1, 100mV and 10kHz ripple		-100		
		PSRR vs VDD2, at DC		-110		
		PSRR vs VDD2, 100mV and 10kHz ripple		-100		
V_{CMout}	Common-mode output voltage		1.40	1.44	1.49	V
$V_{FAILSAFE}$	Failsafe differential output voltage			-2.6	-2.5	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		<0.2		Ω
	Output short-circuit current			±14		mA
CMTI	Common-mode transient immunity		100	150		kV/us
Power supply						
$VDD1_{UVLO}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	2.3	2.5	2.7	V
$VDD2_{UVLO}$	VDD2 undervoltage detection threshold voltage	VDD2 falling	2.2	2.4	2.6	V
IDD1	High-side supply current	3.0V ≤ VDD1 ≤ 3.6V		6.5	8	mA
		4.5V ≤ VDD1 ≤ 5.5V		6.5	8	
IDD2	Low-side supply current	3.0V ≤ VDD2 ≤ 3.6V		3.6	5	mA
		4.5V ≤ VDD2 ≤ 5.5V		3.6	5	

(1) The typical value includes one sigma statistical variation.
(2) This parameter is output referred.

2.9 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

Parameter		Test Condition	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN	See Fig2		0.9		us
t_f	Fall time of OUTP, OUTN	See Fig2		0.9		us
	INP, INN to OUTP, OUTN signal delay (50% – 10%)	unfiltered output, see Fig2		0.8	1.2	us
	INP, INN to OUTP, OUTN signal delay (50% – 50%)	unfiltered output, see Fig2		1.2	1.8	us
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	unfiltered output, see Fig2		1.7	2.6	us
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling		350		us

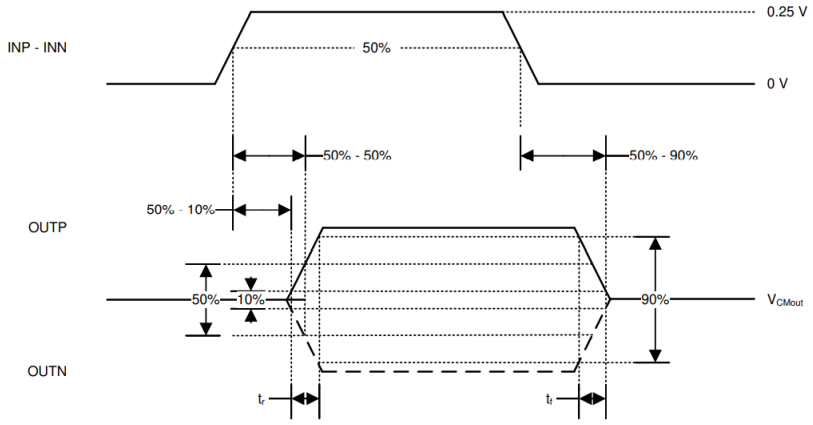


Fig2. Rise, Fall, and Delay Time Waveforms

2.10 Typical Characteristics

VDD1 = 5V, VDD2 = 3.3V, V_{INP} = –250mV to 250mV, V_{INN} = 0V, and f_{IN} = 10kHz (unless otherwise noted).

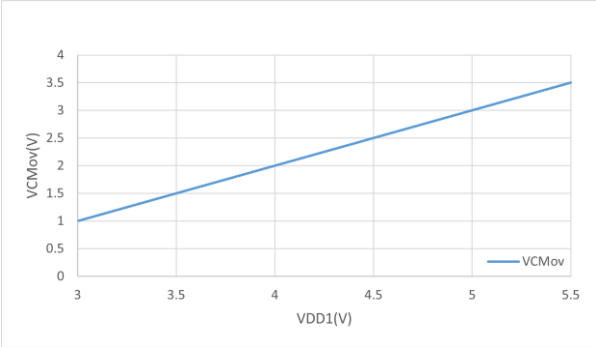


Figure 3. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

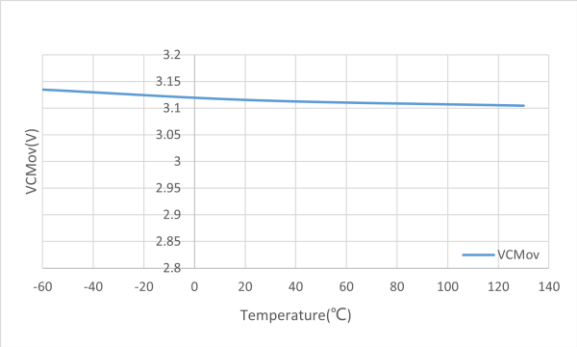


Figure 4. Common-Mode Overvoltage Detection Level vs Temperature

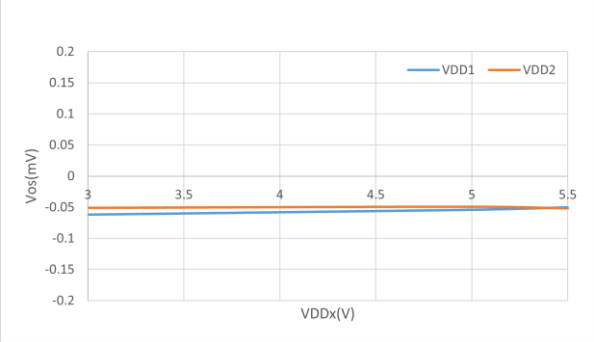


Figure 5. Input Offset Voltage vs Supply Voltage

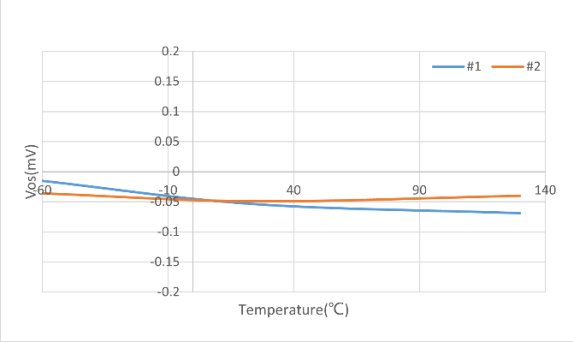


Figure 6. Input Offset Voltage vs Temperature

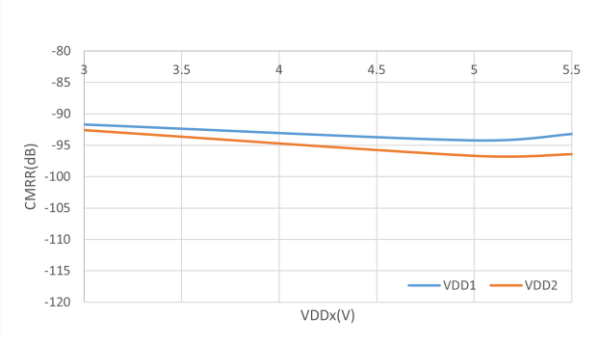


Figure 7. Common-Mode Rejection Ratio vs Supply Voltage

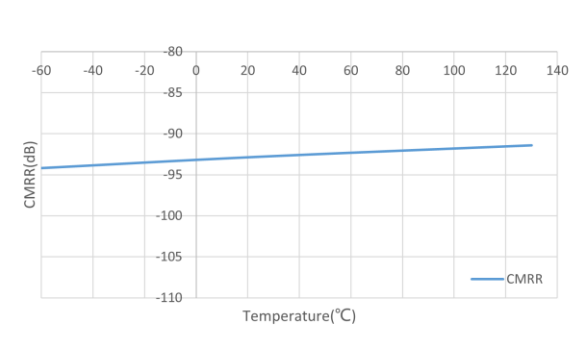


Figure 8. Common-Mode Rejection Ratio vs Temperature

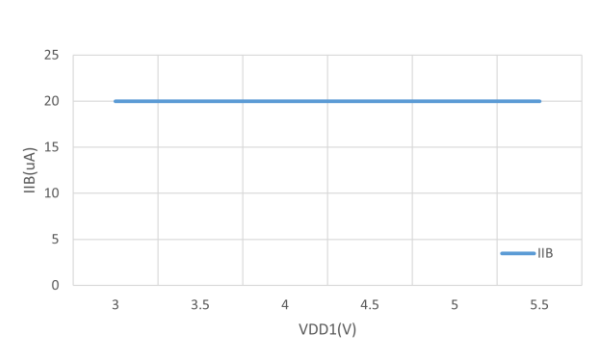


Figure 9. Input Bias Current vs High-Side Supply Voltage

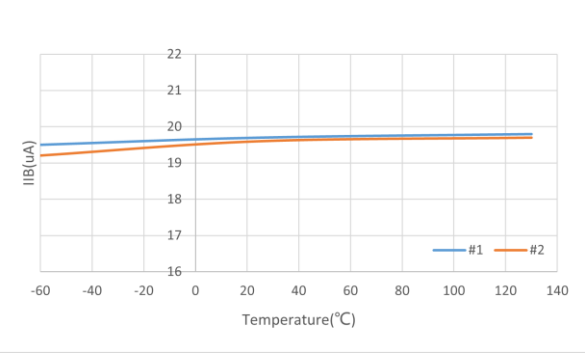


Figure 10. Input Bias Current vs Temperature

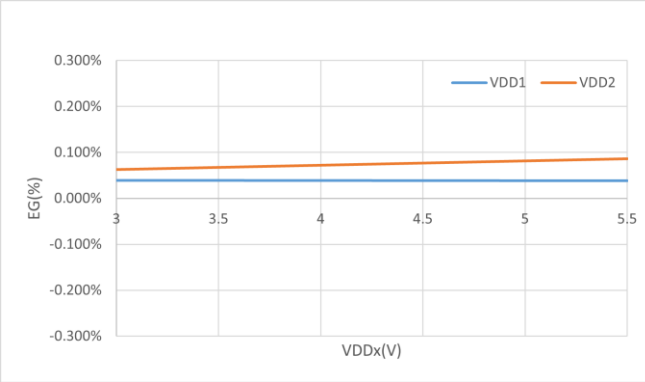


Figure 11. Gain Error vs Supply Voltage

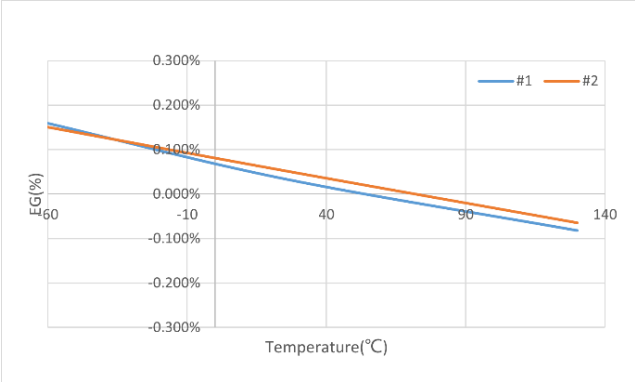


Figure 12. Gain Error vs Temperature

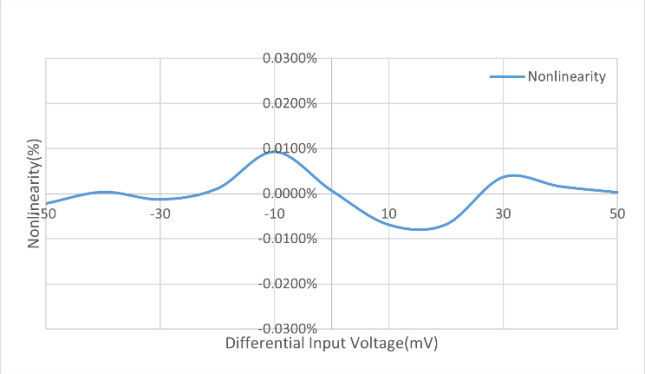


Figure 13. Nonlinearity vs Input Voltage

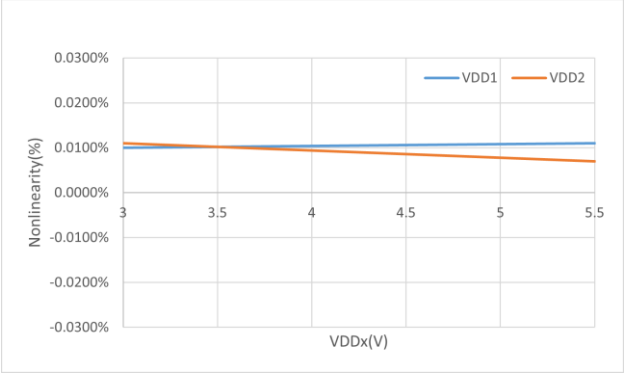


Figure 14. Nonlinearity vs Supply Voltage

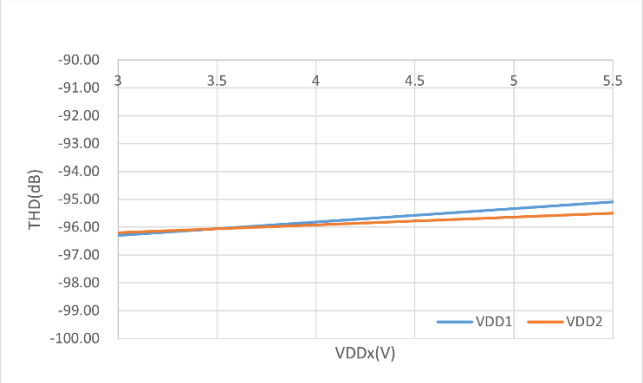


Figure 15. Total Harmonic Distortion vs Supply Voltage

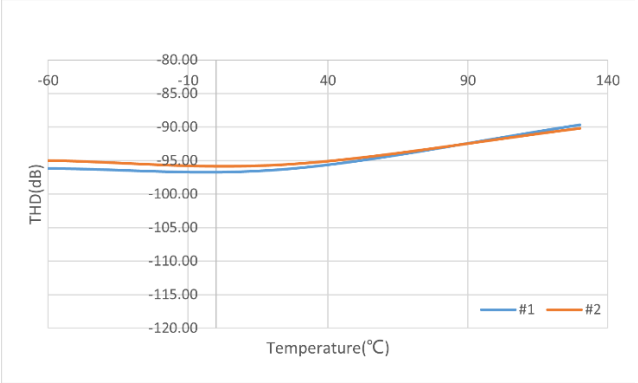


Figure 16. Total Harmonic Distortion vs Temperature

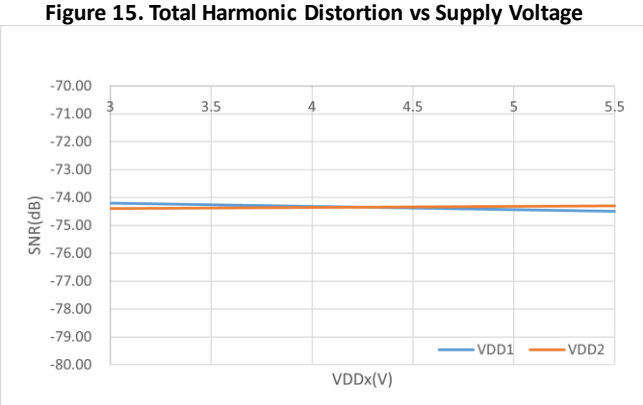


Figure 17. Signal-to-Noise Ratio (10kHz) vs Supply Voltage

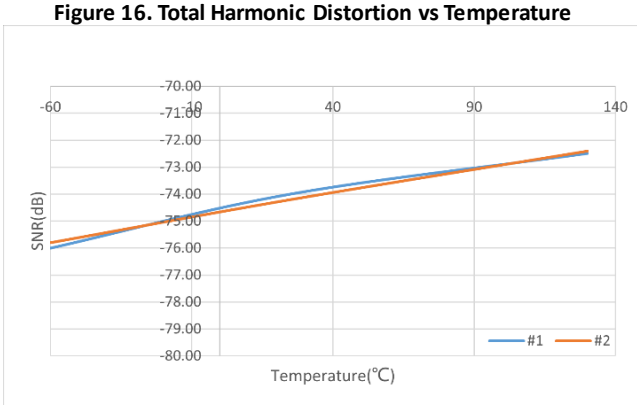


Figure 18. Signal-to-Noise Ratio (10kHz) vs Temperature

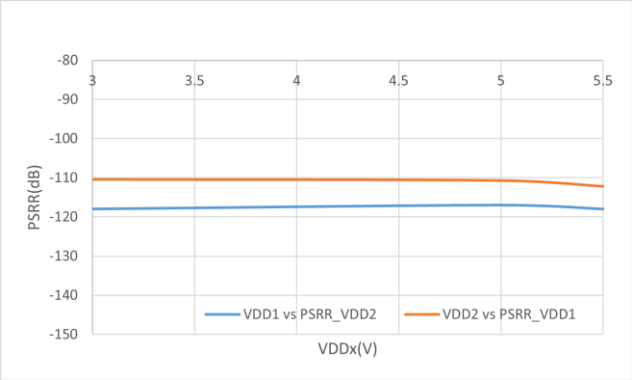


Figure 19. Power-Supply Rejection Ratio vs Supply Voltage

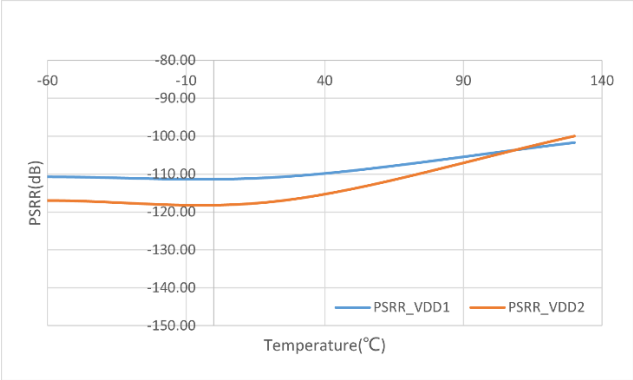


Figure 20. Power-Supply Rejection Ratio vs Temperature

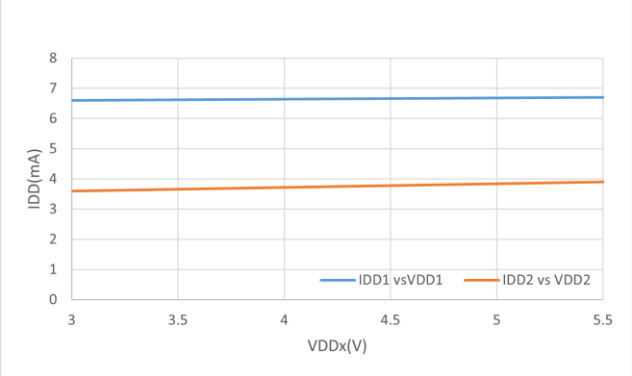


Figure 21. Supply Current vs Supply Voltage

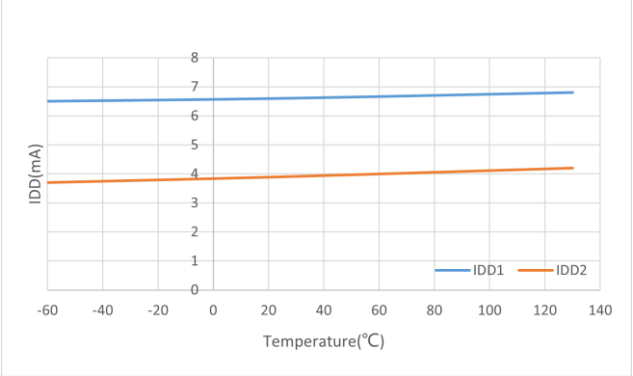


Figure 22. Supply Current vs Temperature

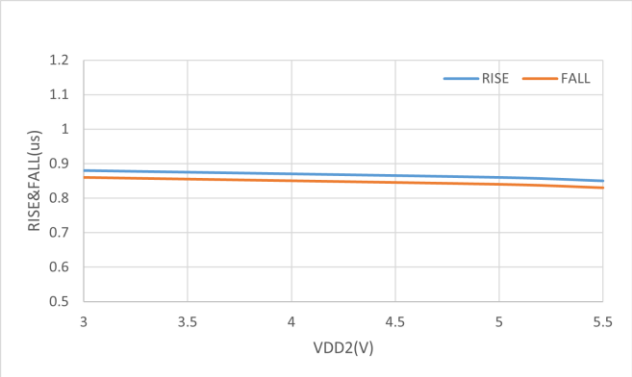


Figure 23. Output Rise and Fall Time vs Low-Side Supply

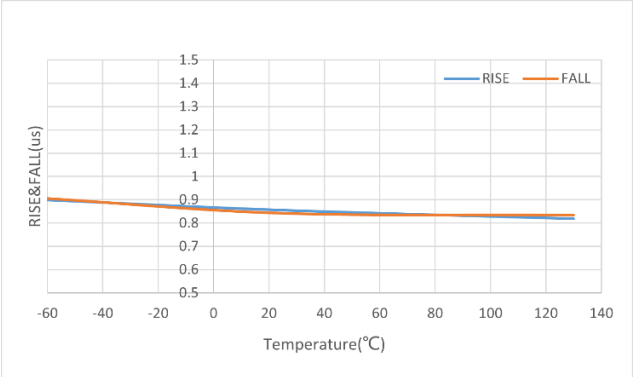


Figure 24. Output Rise and Fall Time vs Temperature

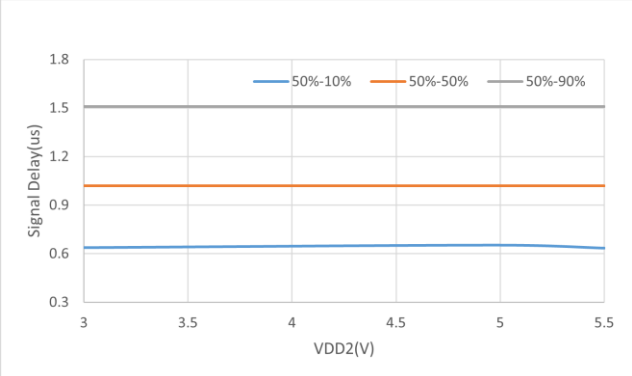


Figure 25. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

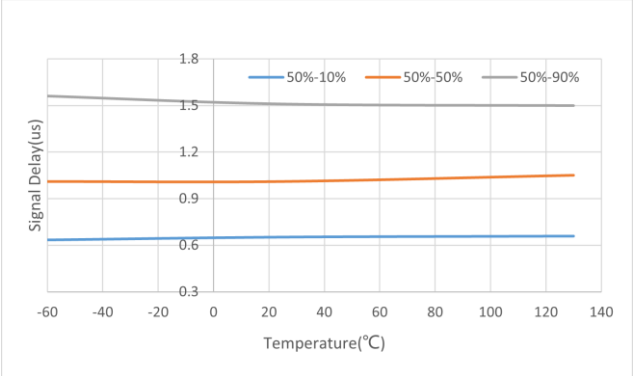


Figure 26. V_{IN} to V_{OUT} Signal Delay vs Temperature

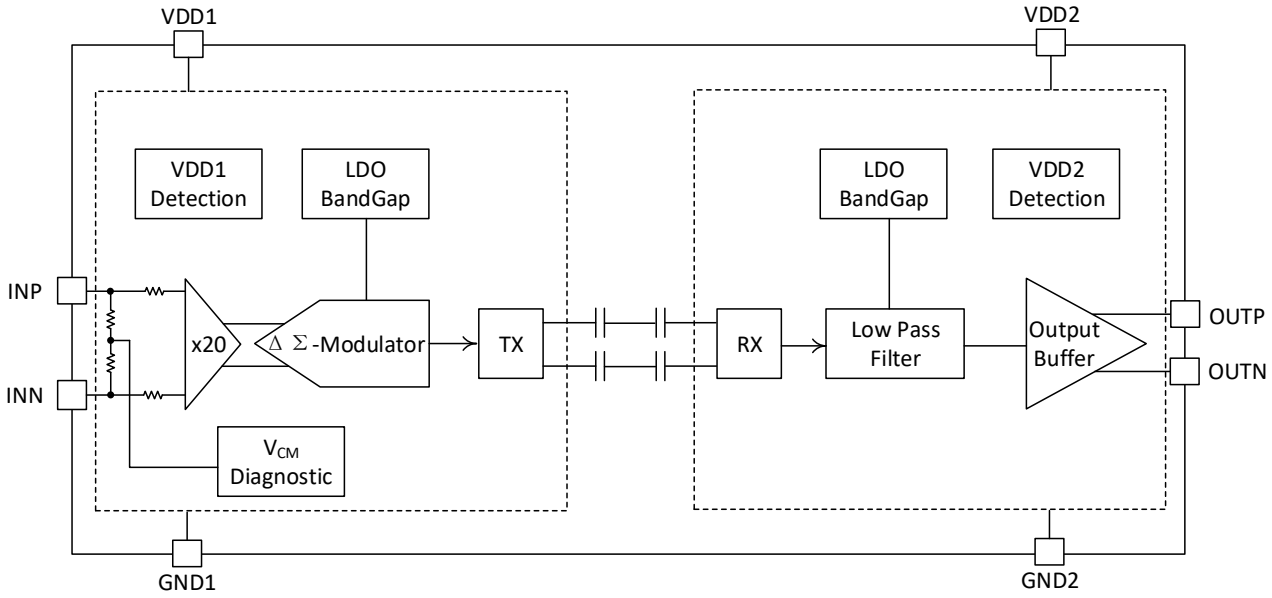
3 Detailed Description

3.1 Overview

The Pai8302E(Q) is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator generates data pulse. The drivers (called TX in the Functional Block Diagram) transfer the data pulse of the modulator across the isolation barrier. The received data pulse is synchronized and processed, as shown in the Functional Block Diagram, by a low pass filter and out buffer on the low-side and presented as a differential output of the device.

Pai8302E(Q) adopts single channel transfer architecture and saves one clock channel, compared with current other amplifiers products, Pai8302E(Q) has the lowest power consumption. Pai8302E(Q) also uses the patented I-divided Voltage technology to support a high level of magnetic field immunity.

3.2 Function block diagram



3.3 Feature Description

3.3.1 Analog Input

The differential amplifier input stage of the Pai8302E(Q) feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into data pulse that is transferred across the isolation barrier, as described in patented I-divided technology.

There are two restrictions on the analog input signals (VINP and VINN). First, if the input voltage exceeds the range GND1–6V to VDD1+0.5V, the input current must be limited to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

3.3.2 Isolation Channel Signal Transmission

The Pai8302E(Q) uses the patented I-divided (I-D) modulation scheme to transmit the modulator output data pulse across the SiO_2 -based isolation barrier. The Pai8302E(Q) also uses special circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

3.3.3 Failsafe Output

The Pai8302E(Q) offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the Pai8302E(Q) is missing, or
- When the common-mode input voltage, that is V_{CM} = (VINP + VINN)/2, exceeds the minimum common-mode overvoltage detection level V_{CMov} of VDD1–2V.

Fig27 and Fig28 show the fail-safe output of the Pai8302E(Q) as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the Electrical Characteristics table as a reference value for the fail-safe detection on a system level.

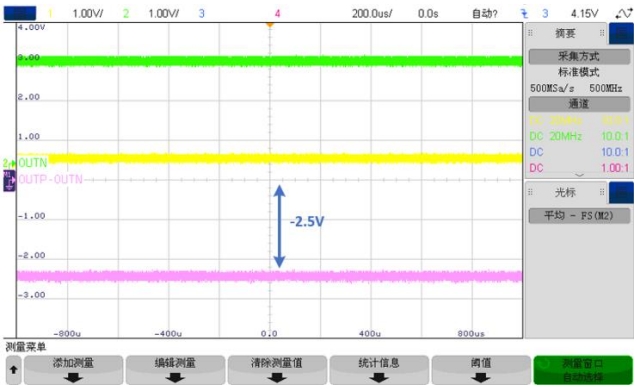


Figure 27. Typical Negative Clipping Output of Pai8302E(Q)

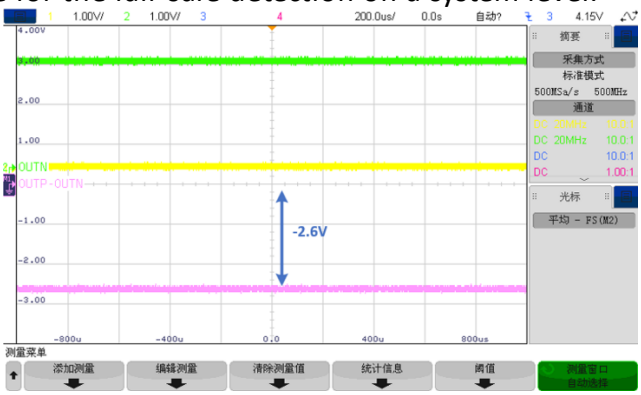


Figure 28. Typical Fail-Safe Output of Pai8302E(Q)

4 Application and Implementation

4.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the Pai8302E(Q) a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

4.2 Typical Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the Pai8302E(Q) is optimized for use with low-value shunt resistors in current sensing applications.

Figure 3 depicts a typical operation of the Pai8302E(Q) for current sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the Pai8302E(Q) ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive).

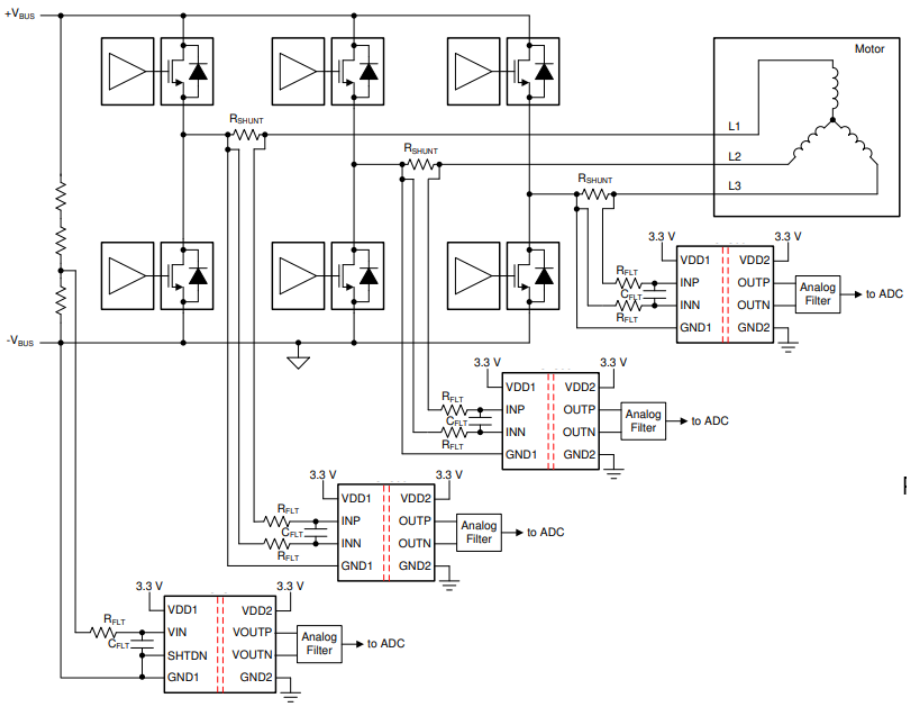


Fig29. Using the Pai8302E(Q) for Current Sensing in Frequency Inverters

4.2.1 Design Requirements

Table1 lists the parameters for this typical application.

Table1 Design Requirement

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage-drop across the shunt for a linear response	± 50mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	2μs (maximum)

4.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the Pai8302E(Q) is derived from the power supply of the upper gate driver. Further details are provided in the Power Supply Recommendations section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the Pai8302E(Q) (INN). If a four-pin shunt is used, the inputs of the Pai8302E(Q) device are connected to the inner leads and GND1 is connected to one of the outer shunts leads. Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

• The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 50mV$.
• The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

For system using single-ended input ADC, Fig30 shows an example of an amplifier-based signal conversion and filter circuit as used for recommended example. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

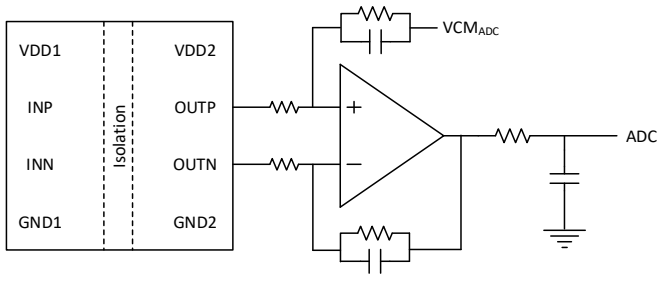


Figure 30. Connecting the Pai8302E(Q) Output to a Single-Ended Input ADC

4.3 What to Do and What Not to Do

Do not leave the inputs of the Pai8302E(Q) unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common mode of the analog frontend approximately 2V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and makes output -2.5V as described in the Fail-Safe Output section, which may lead to an undesired reaction on the system level.

4.4 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5V or 3.3V ± 10%. Alternatively, a low-cost low-dropout (LDO) regulator may be used to minimize noise on the power supply. A low-ESR decoupling capacitor of 0.1 µF to filter this power-supply path is recommended. Place this capacitor (C2 in Fig33) as close as possible to the VDD1 pin of the Pai8302E(Q) for best performance. If better filtering is required, an additional 2.2 µF capacitor may be used. To decouple the low-side power supply on the controller side, use a 0.1 µF capacitor placed as close to the VDD2 pin of the Pai8302E(Q) as possible, followed by an additional capacitor from 1 µF to 10 µF.

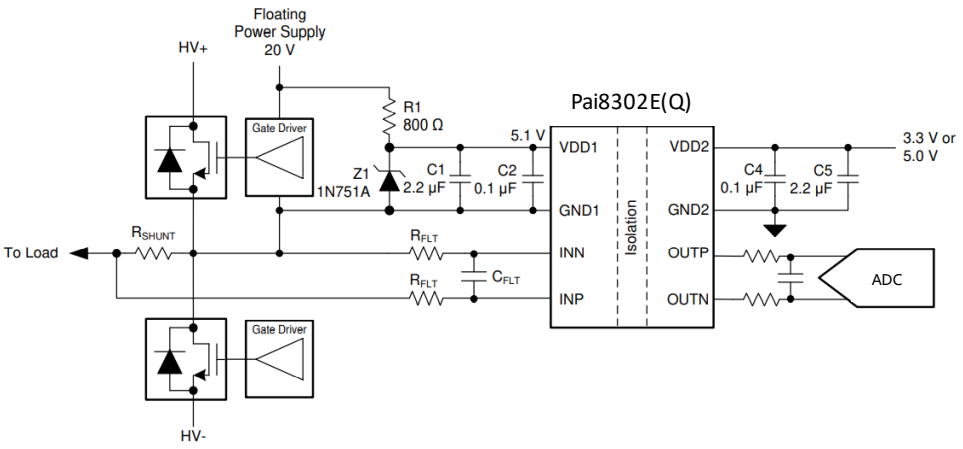


Figure 33. Zener-Diode-Based, High-Side Power Supply

4.5 Layout

Fig34 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the Pai8302E(Q) supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the Pai8302E(Q) and keep the layout of both connections symmetrical.

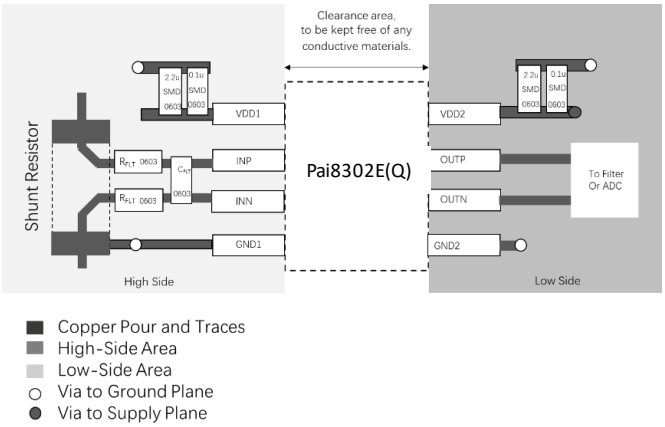
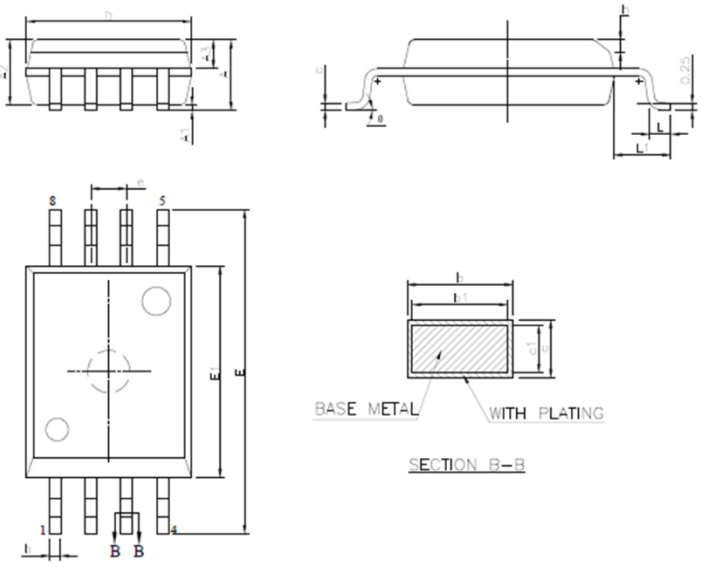


Figure 34. Recommended Layout of the Pai8302E(Q)

5 Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	1.00
L1	2.00REF		
θ	0	—	8°

Fig4. Outline Package

6 Land Patterns

The Fig5 illustrates the recommended land pattern details for the Pai8302E(Q) in an 8-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

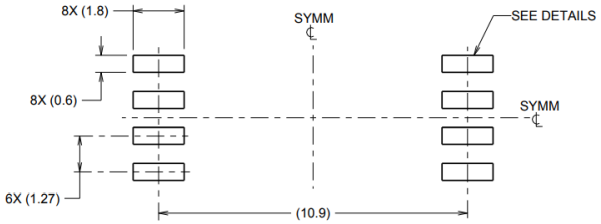


Fig5. SO8W Land Pattern

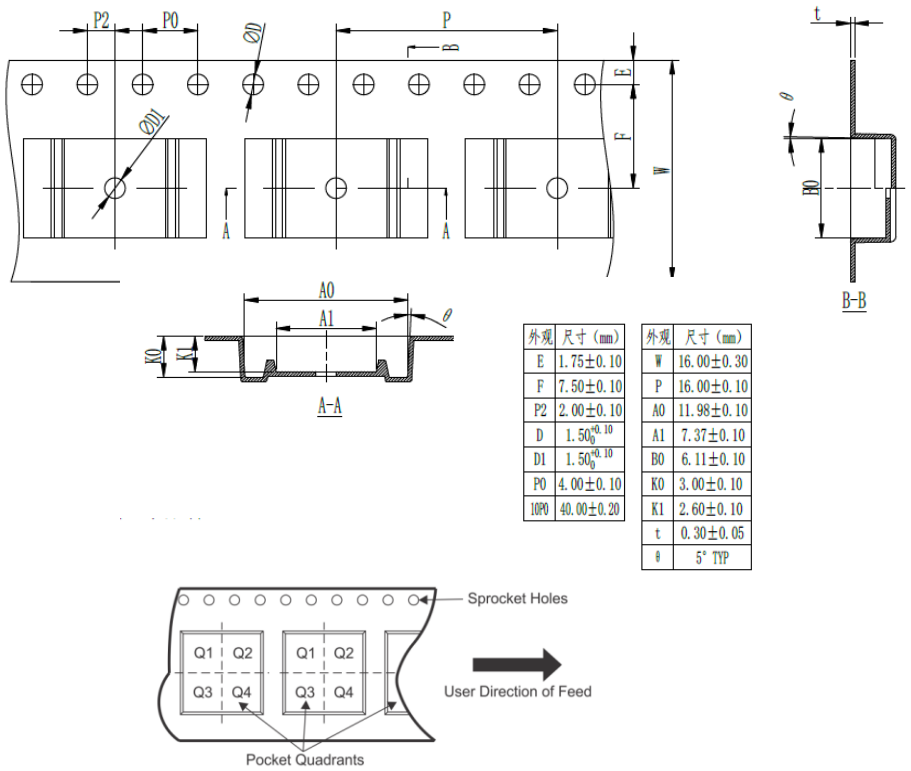
Note: All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

7 Top Marking

Fig6. Top Marking

Line 1	XXXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

8 Reel Information



外观	尺寸（mm）
E	1.75±0.10
F	7.50±0.10
P2	2.00±0.10
D	$1.50^{+0.10}_{0}$
D1	$1.50^{+0.10}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

外观	尺寸（mm）
W	16.00±0.30
P	16.00±0.10
A0	11.98±0.10
A1	7.37±0.10
B0	6.11±0.10
K0	3.00±0.10
K1	2.60±0.10
t	0.30±0.05
θ	5° TYP

Fig7. Reel Information

Note: The Pin 1of the chip is in the quadrant Q1.

9 Ordering Guide

Model Name	Temperature Range	Withstand Voltage Rating (kV_{RMS})	Package	MSL Peak Temp(1)	Quantity per reel
Pai8302E-W5R	−40~125°C	5.0	WB SOIC-8	Level-3-260C-168 HR	1000
Pai8302EQ-W5R	−40~125°C	5.0	WB SOIC-8	Level-3-260C-168 HR	1000

(1) The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

10 Important Notice and Disclaimer

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11 Revision History

Ver	Date	Page	Change Record.
0.1	2022-12-09	All	Initial version.
0.2	2024-08-15	P5	Update certifications.
0.3	2024-09-17	P6-P8	Update production data.
0.4	2025-02-07	P6	Update based on mass production data.