

CS817x20/CS817x22 Low-Power Dual-Channel Digital Isolators

1. Features

- **Ultra Low Power**
 - 90 μ A per channel at DC with 3.3V operation
 - 100 μ A per channel at 10kbps with 3.3V operation
 - 160 μ A per channel at 200kbps with 3.3V operation
- **Data Rate is up to 200kbps**
- **2.375V to 5.5V Wide Operating Supply Voltage**
- **Robust Galvanic Isolation of Digital Signals**
 - High lifetime: >40 years
 - Up to 3kV_{RMS} isolation rating
 - ± 150 kV/ μ s typical CMTI
 - Schmitt trigger inputs for high noise immunity
 - High electromagnetic immunity
- **No Start-up Initialization Required**
- **Wide operating temperature range: -40°C to 105°C**
- **Default Output High (CS817x2xHS) and Low (CS817x2xLS) Options**
- **RoHS-Compliant Package:**
 - SOIC8(S) narrow body

2. Applications

- Li+ Battery Protection
- Home Appliances
- Industrial automation systems
- Motor control
- Medical electronics
- Isolated switch mode supplies
- Power inverters
- Isolated ADC, DAC

3. General Description

The CS817x20/CS817x22 family of ultra-low-power digital isolators used Chipanalog's "Pulse-Coding" capacitive isolation technology, offering as low as 90 μ A per channel low quiescent current. These isolated CMOS compatible digital I/Os feature up to 3kV_{RMS} isolation rating and ± 150 kV/ μ s typical CMTI, provide high electromagnetic immunity and low EMI. All device versions have Schmitt

trigger inputs for high noise immunity and each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO₂) insulation barrier, only require two V_{DD} bypass capacitors to build a digital signal isolation solution.

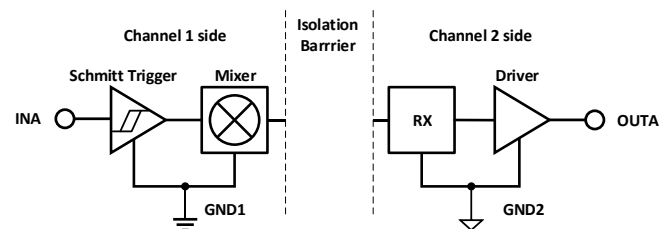
The CS817x20/CS817x22 family of devices offers all possible unidirectional channel configurations to accommodate 2-channel design digital I/O applications. The CS817x20HS and CS817x20LS feature 2 channels transferring digital signals in one direction; The CS817x22HS and CS817x22LS devices have one forward and one reverse-direction channel. All devices of this family feature default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix LS and high for devices with suffix HS, see the *Ordering Information* for suffixes associated with each option.

This family of digital isolators is based on a simple isolation architecture that provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single channel of the CS817x20 and CS817x22 is shown in the figure below. The CS817x20/CS817x22 family of devices are specified over the -40°C to +105°C operating temperature range and are available in 8-pin SOIC narrow body package.

Device information

Part number	Package	Package size (NOM)
CS817x20HS CS817x20LS CS817x22HS CS817x22LS	SOIC8-NB(S)	4.90 mm × 3.90 mm

Simplified Channel Structure



GND1 and GND2 are the isolated grounds for "1" side and "2" side respectively.

4. Ordering Information

Table. 4-1 Ordering Information

Part Number	Number of Inputs "1" Side	Number of Inputs "2" Side	Default Output	Isolation Rating (kV _{RMS})	Output Enable	Package
CS817x20LS	2	0	Low	3	N/A	SOIC8-NB
CS817x20HS	2	0	High	3	N/A	SOIC8-NB
CS817x22LS	1	1	Low	3	N/A	SOIC8-NB
CS817x22HS	1	1	High	3	N/A	SOIC8-NB

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5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	Removed "TTL logic compatible".	15
Version 1.02	Add max limit in the electrical table, as shown in chapter 7.9. Add "11 Typical Waveforms and Curve" chapter.	8,9 15

6. Pin Configuration and Description

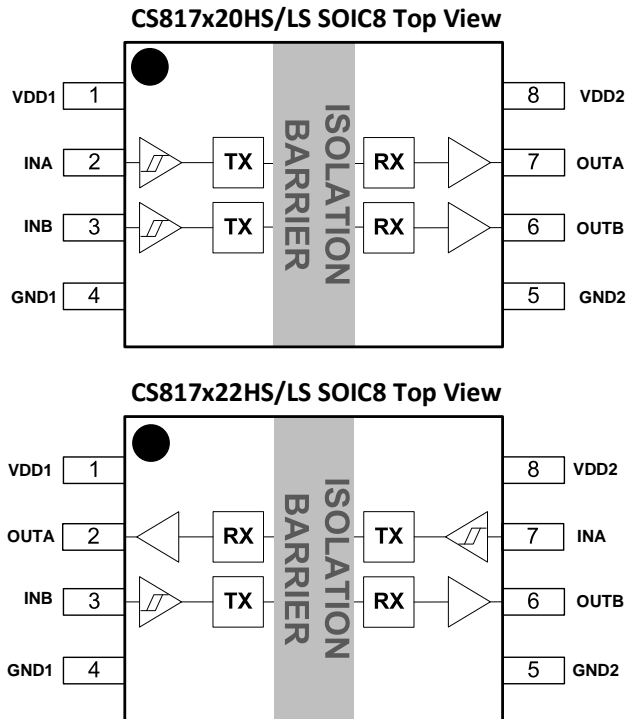


Figure 6-1 CS817x20HS/LS, CS817x22HS/LS pin configuration

Table 6-1 CS817x20/CS817x22 pin description

SOIC8 Pin #		Pin Name	Type	Description
CS817x20LS CS817x20HS	CS817x22LS CS817x22HS			
1	1	VDD1	Power	Power supply for side "1".
2	7	INA	Logic I/O	Digital input A on side "1"/"2", corresponds to logic output A on side "2"/"1".
3	3	INB	Logic I/O	Digital input B on side "1", corresponds to logic output B on side "2".
4	4	GND1	GND	Ground reference for side "1".
5	5	GND2	GND	Ground reference for side "2".
6	6	OUTB	Logic I/O	Digital output B on side "2", OUTB is the logic output for the INB input on side "1".
7	2	OUTA	Logic I/O	Digital output A on side "2"/"1", OUTA is the logic output for the INA input on side "1"/"2".
8	8	VDD2	Power	Power supply for side "2".

7. Specifications

7.1. Absolute Maximum Ratings¹

Parameters	Minimum value	Maximum value	Unit
V_{DD1}, V_{DD2}	-0.5	6.0	V
V_{in}	-0.5	$V_{DD1}+0.5^3$	V
I_o	-20	20	mA
T_j		150	°C
T_{STG}	-65	150	°C

Notes:

- The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- V_{DD1} = Input-Side Supply V_{DD} , the maximum voltage must not be exceed 6 V.

7.2. ESD Ratings

		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±5000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins ²	±2000	

Notes:

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT		
V_{DD1}, V_{DD2}	2.375	3.3/5.0	5.5	V		
I_{OH}	High-level Output Current	$V_{DDO}^1 = 5V$	4	mA		
		$V_{DDO} = 3.3V$	2			
		$V_{DDO} = 2.5V$	1			
I_{OL}	Low-level Output Current	$V_{DDO} = 5V$	-4	mA		
		$V_{DDO} = 3.3V$	-2			
		$V_{DDO} = 2.5V$	-1			
V_{IH}	High-level Input Voltage		$0.7 \times V_{DD1}^1$	V		
V_{IL}	Low-level Input Voltage		$0.3 \times V_{DD1}$	V		
DR	Data Rate		0	200	kbps	
T_A	Ambient Temperature		-40	25	125	°C

Note:

- V_{DD1} = Input-Side Supply V_{DD} ; V_{DDO} = Output Side Supply V_{DD} .

7.4. Thermal Information

Thermal Metric	CS817x2x HS/LS	UNIT	
	SOIC8-NB(S)		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W

7.5. Power Rating

PARAMETER	Test conditions	MIN	TYP	MAX	UNIT
CS817x20HS/LS					
P_D	Maximum Power Dissipation	$V_{DD1} = V_{DD2} = 5.5V, C_L = 15pF,$		5	mW
P_{D1}	Maximum Power Dissipation on Side "1"	$T_J = 150^\circ C,$ with 100kHz 50% duty cycle square wave input.		1	mW
P_{D2}	Maximum Power Dissipation on Side "2"			4	mW
CS817x22HS/LS					
P_D	Maximum Power Dissipation	$V_{DD1} = V_{DD2} = 5.5V, C_L = 15pF,$		4	mW
P_{D1}	Maximum Power Dissipation on Side "1"	$T_J = 150^\circ C,$ with 100kHz 50% duty cycle square wave input.		2	mW
P_{D2}	Maximum Power Dissipation on Side "2"			2	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value	UNIT
			S	
CLR	External Clearance ¹	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External Creepage ¹	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	Per IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 400 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
DIN V VDE V 0884-11:2017-01				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDb) test	400	V _{RMS}
		DC voltage	566	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t=60 s (certified); V _{TEST} = 1.2 × V _{IOTM} , t=1 s (100% product test)	4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ²	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (production test)	4000	V _{PK}
Q _{pd}	Apparent charge ³	Method a, after input/output safety test of the subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁴	V _{IO} = 0.4 × sin(2πft), f = 100kHz	~0.5	pF
R _{IO}	Isolation resistance ⁴	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production test)	3000	V _{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE(Pending)	CSA(Pending)	UL(Pending)	CQC(Pending)	TUV(Pending)
Certified according to DIN VDE V 0884-11:2017-01.	Certified according to IEC60950-1, IEC 62368-1 and IEC 60601-1.	Certified according to UL 1577 Component Recognition Program.	Certified according to GB 4943.1-2011.	Certified according to EN61010-1:2010 (3rd Ed) and EN 60950-1:2006 /A2:2013.

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7.8. Electrical Characteristics
 $V_{DD1} = V_{DD2} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 105°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	$I_{OH} = -4\text{mA}$; See 错误!未找到引用源。	$V_{DDO}^{1-0.4}$	4.7		V
V_{OL}	Low-level Output Voltage	$I_{OL} = 4\text{mA}$; See 错误!未找到引用源。		0.3	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				$0.7 \times V_{DD1}^1$	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{DD1}$			V
$V_{I(HYS)}$	Input Threshold Hysteresis		$0.1 \times V_{DD1}$			V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DD1}$ at INx			1	μA
I_{IL}	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-1			μA
CMTI	Common-mode Transient Immunity	$V_I = V_{DD1}^1$ or 0 V, $V_{CM} = 1500\text{ V}$; 错误!未找到引用源。	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 100\text{kHz}$, $V_{DD} = 5\text{ V}$		2		pF

Notes:

- V_{DD1} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- Measured from pin to Ground.

 $V_{DD1} = V_{DD2} = 3.3\text{ V} \pm 10\%$, $T_A = -40$ to 105°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	$I_{OH} = -4\text{mA}$; See 错误!未找到引用源。	$V_{DDO}^{1-0.4}$	3.0		V
V_{OL}	Low-level Output Voltage	$I_{OL} = 4\text{mA}$; See 错误!未找到引用源。		0.3	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				$0.7 \times V_{DD1}$	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{DD1}$			V
$V_{I(HYS)}$	Input Threshold Hysteresis		$0.1 \times V_{DD1}$			V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DD1}$ at INx			1	μA
I_{IL}	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-1			μA
CMTI	Common-mode Transient Immunity	$V_I = V_{DD1}^1$ or 0 V, $V_{CM} = 1500\text{ V}$; 错误!未找到引用源。	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 100\text{kHz}$, $V_{DD} = 3.3\text{V}$		2		pF

Notes:

- V_{DD1} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- Measured from pin to Ground.

 $V_{DD1} = V_{DD2} = 2.5\text{ V} \pm 10\%$, $T_A = -40$ to 105°C (over recommended operating conditions, unless otherwise specified)

Parameters		Test conditions	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	$I_{OH} = -4\text{mA}$; See 错误!未找到引用源。	$V_{DDO}^{1-0.5}$	2.2		V
V_{OL}	Low-level Output Voltage	$I_{OL} = 4\text{mA}$; See 错误!未找到引用源。		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				$0.7 \times V_{DD1}$	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{DD1}$			V
$V_{I(HYS)}$	Input Threshold Hysteresis		$0.1 \times V_{DD1}$			V
I_{IH}	High-Level Input Leakage Current	$V_{IH} = V_{DD1}$ at INx			1	μA
I_{IL}	Low-Level Input Leakage Current	$V_{IL} = 0\text{ V}$ at INx	-1			μA
CMTI	Common-mode Transient Immunity	$V_I = V_{DD1}^1$ or 0 V, $V_{CM} = 1500\text{ V}$; 错误!未找到引用源。	100	150		$\text{kV}/\mu\text{s}$
C_i	Input Capacitance ³	$V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 100\text{kHz}$, $V_{DD} = 2.5\text{V}$		2		pF

Notes:

- V_{DD1} = Input-side supply V_{DD} , V_{DDO} = Output-side supply V_{DD} .
- Measured from pin to Ground.

7.9. Supply Current Characteristics

$V_{DD1} = V_{DD2} = 5\text{ V} \pm 10\%$, $T_A = -40\text{ to }105^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions	Supply Current	MIN	TYP	MAX	UNIT	
CS817x20HS/LS							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CS817x20LS); $V_{IN} = V_{DD1}^1$ (CS817x20HS)	I_{DD1}		30	60	μA	
		I_{DD2}		170	340		
	$V_{IN} = V_{DD1}$ (CS817x20LS); $V_{IN} = 0\text{V}$ (CS817x20HS)	I_{DD1}		40	80		
		I_{DD2}		170	340		
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 5.0V amplitude; $C_L = 15\text{ pF}$ for each channel.	10kbps (5kHz)	I_{DD1}		45		90
			I_{DD2}		180		360
	200kbps (100kHz)	I_{DD1}		180	360		
		I_{DD2}		300	600		
CS817x22HS/LS							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CS817x22LS); $V_{IN} = V_{DD1}$ (CS817x22HS)	I_{DD1}		100	200	μA	
		I_{DD2}		105	210		
	$V_{IN} = V_{DD1}$ (CS817x22LS); $V_{IN} = 0\text{V}$ (CS817x22HS)	I_{DD1}		100	200		
		I_{DD2}		105	210		
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 5.0V amplitude; $C_L = 15\text{ pF}$ for each channel.	10kbps (5kHz)	I_{DD1}		105		210
			I_{DD2}		110		220
	200kbps (100kHz)	I_{DD1}		215	430		
		I_{DD2}		220	440		
Note:							
1. V_{DD1} = Input-side supply V_{DD} .							

$V_{DD1} = V_{DD2} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }105^\circ\text{C}$ (over recommended operating conditions, unless otherwise specified).

Parameters	Test conditions	Supply Current	MIN	TYP	MAX	UNIT	
CS817x20HS/LS							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CS817x20LS); $V_{IN} = V_{DD1}^1$ (CS817x20HS)	I_{DD1}		25	50	μA	
		I_{DD2}		155	310		
	$V_{IN} = V_{DD1}$ (CS817x20LS); $V_{IN} = 0\text{V}$ (CS817x20HS)	I_{DD1}		30	60		
		I_{DD2}		160	320		
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 3.3V amplitude; $C_L = 15\text{ pF}$ for each channel.	10kbps (5kHz)	I_{DD1}		35		70
			I_{DD2}		165		330
	200kbps (100kHz)	I_{DD1}		115	230		
		I_{DD2}		235	470		
CS817x22HS/LS							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CS817x22LS); $V_{IN} = V_{DD1}$ (CS817x22HS)	I_{DD1}		90	180	μA	
		I_{DD2}		95	190		
	$V_{IN} = V_{DD1}$ (CS817x22LS); $V_{IN} = 0\text{V}$ (CS817x22HS)	I_{DD1}		90	180		
		I_{DD2}		95	190		
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 3.3V amplitude; $C_L = 15\text{ pF}$ for each channel.	10kbps (5kHz)	I_{DD1}		95		190
			I_{DD2}		100		200
	200kbps (100kHz)	I_{DD1}		160	320		
		I_{DD2}		165	330		
Note:							
1. V_{DD1} = Input-side supply V_{DD} .							

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 $V_{DD1} = V_{DD2} = 2.5 V \pm 10\%$, $T_A = -40$ to $105^\circ C$ (over recommended operating conditions, unless otherwise specified).

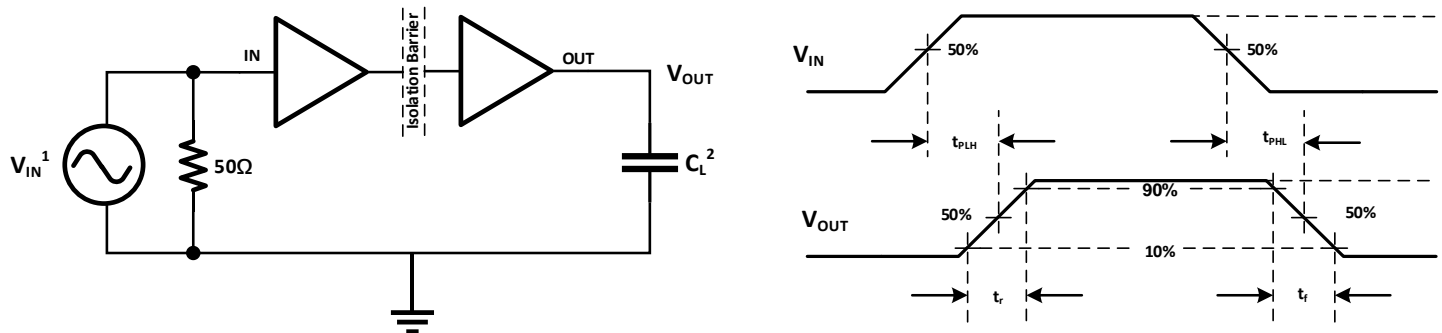
Parameters	Test conditions	Supply Current	MIN	TYP	MAX	UNIT
CS817x20HS/LS						
Supply Current – DC Signal	$V_{IN} = 0V$ (CS817x20LS); $V_{IN} = V_{DD1}^1$ (CS817x20HS)	I_{DD1}		25	50	μA
		I_{DD2}		150	300	
	$V_{IN} = V_{DD1}$ (CS817x20LS); $V_{IN} = 0V$ (CS817x20HS)	I_{DD1}		35	70	
		I_{DD2}		155	310	
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 2.5V amplitude; $C_L = 15$ pF for each channel.	10kbps (5kHz)	I_{DD1}	30	60	μA
			I_{DD2}	155	310	
	200kbps (100kHz)	I_{DD1}	40	80		
		I_{DD2}	180	360		
CS817x22HS/LS						
Supply Current – DC Signal	$V_{IN} = 0V$ (CS817x22LS); $V_{IN} = V_{DD1}$ (CS817x22HS)	I_{DD1}		90	180	μA
		I_{DD2}		95	190	
	$V_{IN} = V_{DD1}$ (CS817x22LS); $V_{IN} = 0V$ (CS817x22HS)	I_{DD1}		90	180	
		I_{DD2}		95	190	
Supply Current – AC Signal	All Channels switching with 50% duty cycle square wave and input with 2.5V amplitude; $C_L = 15$ pF for each channel.	10kbps (5kHz)	I_{DD1}	90	180	μA
			I_{DD2}	95	190	
	200kbps (100kHz)	I_{DD1}	145	290		
		I_{DD2}	150	300		
Note:						
1. V_{DD1} = Input-side supply V_{DD} .						

7.10. Timing Characteristics

 $V_{DD1} = V_{DD2} = 2.5V \sim 5.5V$, $T_A = -40$ to $105^\circ C$ (over recommended operating conditions, unless otherwise specified)

Parameters	Test conditions	MIN	TYP	MAX	UNIT
DR Data Rate			0	200	kbps
PW_{min} Minimum Pulse Width		5			μs
t_{PLH} , t_{PHL} Propagation Delay Time	See 错误!未找到引用源。		1.1	2	μs
PWD Pulse Width Distortion $ t_{PLH} - t_{PHL} $				100	ns
$t_{sk(o)}$ Channel-to-Channel Output Skew Time ¹	Same-direction channels.			100	ns
$t_{sk(pp)}$ Part-to-Part Output Skew Time ²				300	ns
t_r Output Signal Rise Time	See 错误!未找到引用源。		2.8	5.0	ns
t_f Output Signal Fall Time	See 错误!未找到引用源。		2.8	5.0	ns
t_{DO} Default Output Delay Time from Input Power Loss	See 错误!未找到引用源。		400	600	μs
t_{SU} Start-up Time			50		μs
F_R Refresh Rate			20		kbps
Notes:					
1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.					
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.					

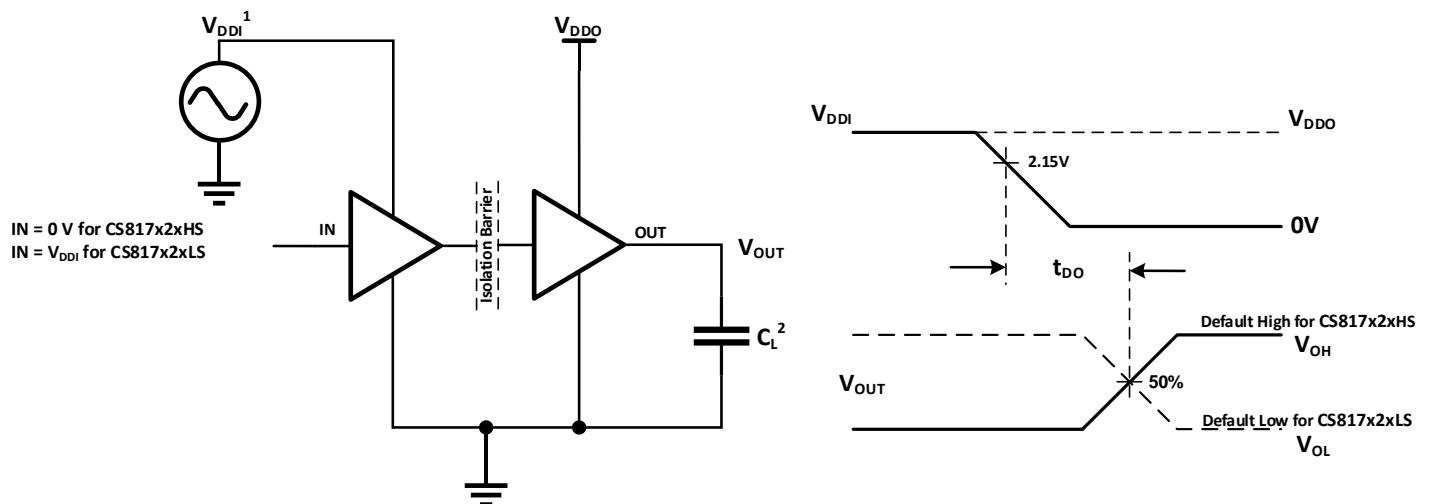
8. Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with the following characteristics: frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_{r3} \leq 3\text{ns}$, $t_{f3} \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. $C_L = 15\text{pF}$, it includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

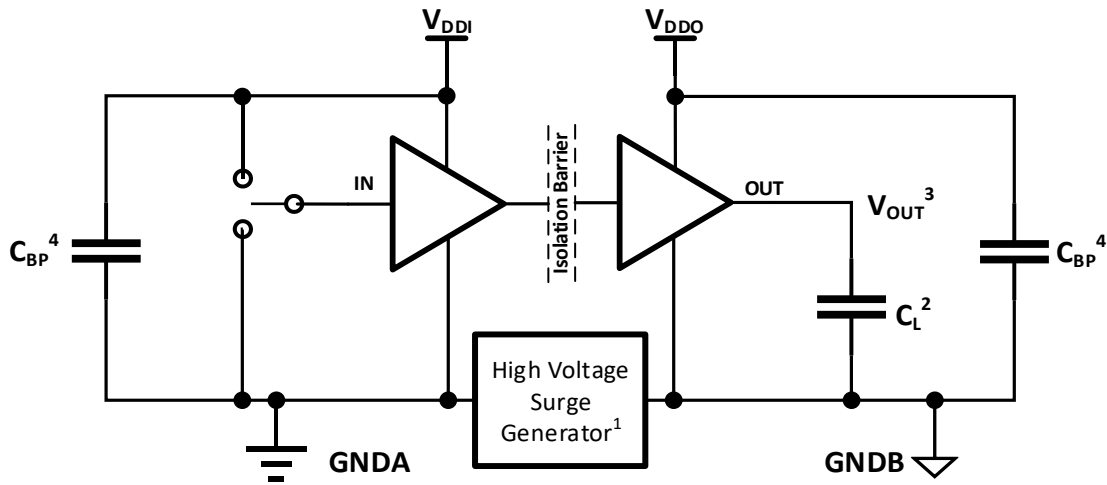
Figure. 8-1 Switching Characteristics Test Circuit and Voltage Waveforms



Notes:

1. Power Supply Ramp Rate = 10 mV/ns . V_{DDI} should ramp over 2.375V , and less than 5.5V .
2. $C_L = 15\text{pF}$, it includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure. 8-2 Default Output Delay Time Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/μs slew rate.
2. $C_L = 15\text{pF}$, it includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure. 8-3 Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CS817x20HS/LS and CS817x22HS/LS family of devices is available in a 8-pin SOIC package with 4mm creepage and clearance, with an isolation rating of $3kV_{RMS}$. These digital isolators offer low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Chipanalog's proprietary Pulse-Coding technology. The devices feature up to 200kbps data rate and can be used to isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. The CS817x20HS/LS feature all two channels transmitting digital signals in one direction and CS817x22HS/LS provide one channel transmitting digital signal in one direction and one channel transmitting in the opposite direction, which are suitable in applications such as isolated digital I/O. Both CS817x20 and CS817x22 have V_{DD1}/V_{DD2} two supply inputs that independently set the logic levels on either side of the insulation barrier. V_{DD1} and V_{DD2} are referenced to GND1 and GND2 respectively. The wide supply voltage range of V_{DD1} and V_{DD2} allows the devices to be used for level translation in addition to isolation.

The CS817x20/CS817x22 dual-channel digital galvanic isolators using full differential capacitive isolation technology build a robust data transmission path between different power domains without any special start-up initialization requirements. Also, with the advanced full differential techniques, these devices maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching, to provide best-in-class noise immunity. All devices also feature a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely. The CS817x20HS/CS817x22HS feature default-high outputs. The CS817x20LS/CS81722LS feature default-low outputs. The output assumes the default state when the input is not powered or if the input is open-circuit.

9.2. Functional Block Diagram

The CS817x20/CS817x22 digital isolation used edge based capacitive architecture, with very sensitive receiver, it can detect the edge of very small pulse. Then the receiver modulates the signal and transfer the signal across the barrier, and get back the square wave at driver output. Compared with inductive isolation, these digital isolator devices based on capacitive isolation can get low power at high frequency operation, reduces propagation delay and jitter, and provide good immunity to magnetic fields. See *Figure 9-1* the function block diagram for a single channel of the CS817x20/ CS817x22 for more details.

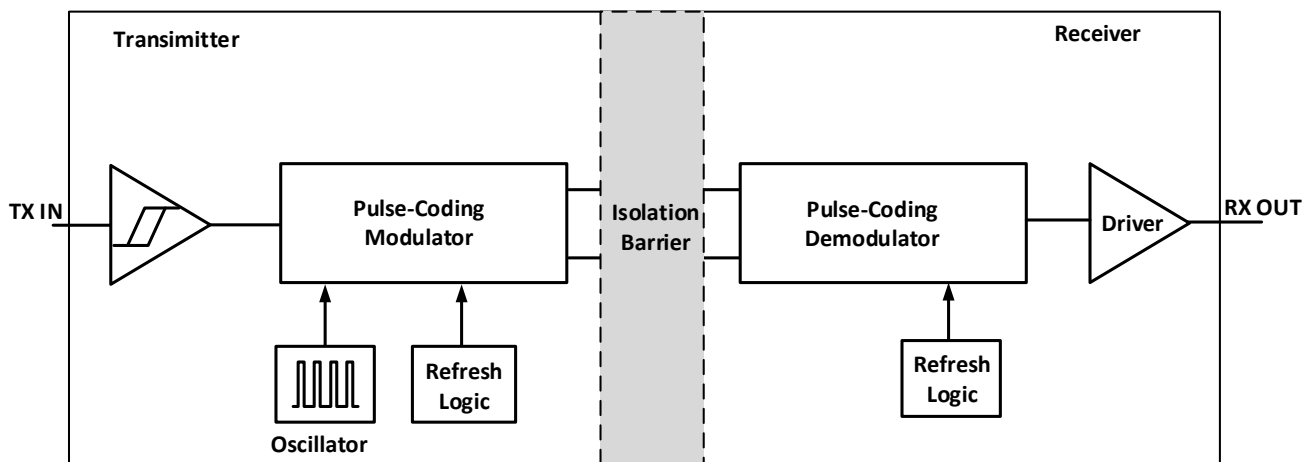


Figure. 9-1 Functional Block Diagram of a Single Channel

9.3. Refresh Rate

The CS817x2xHS/LS series low-power digital isolators incorporate Chipanalog's "pulse coding" patented technology to transmit signals across isolation barriers. These devices include a data refresh circuit to ensure that the DC output signal is consistent with the DC input signal. The internal watchdog counter monitors the input for each channel, if there is no input signal within every 50 μ s, the data will be refreshed automatically to ensure that the input and output signals are the same.

9.4. Device Operation Modes

The CS817x20/CS817x22 devices behavior during start-up, normal operation is shown in *Table 9-1*. Also, refer to the following table to determine outputs when power supply (V_{DD}) is not present.

Table 9-1 Operation Mode¹

V_{DDI}	V_{DDO}	Input (INx) ²	Output (OUTx)	Operation Mode
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input INx is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for CS817x2_HS and Low for CS817x2_LS.
PD	PU	X	Default	Default output mode: When V_{DDI} is unpowered, a channel output assumes the logic state based on its default option. Default is <i>High</i> for CS817x2_HS and Low for CS817x2_LS.
X	PD	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined.

Notes:

- V_{DDI} = Input-side supply V_{DD} ; V_{DDO} = Output-side supply V_{DD} ; PU = Powered up ($V_{DD} \geq 2.375V$); PD = Powered down ($V_{DD} < 2.375V$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
- A strong driving input signal can weakly power the floating V_{DD} through the internal protection diode and cause undetermined output.

10. Application and Implementation

The CS817x20/CS817x22 isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The CS817x20/CS817x22 devices are the high-performance, dual-channel digital isolators. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CS817x20/CS817x22 devices only require two external bypass capacitors to operate. *Figure 10-1* and *Figure 10-2* show typical operating circuit for the CS817x22 and CS817x20, respectively.

To reduce ripple and the chance of introducing data errors, bypass V_{DD1} and V_{DD2} supplies with at least 1 μ F low-ESR ceramic capacitors to GND1 and GND2 respectively. Place the bypass capacitors as close to the power supply input pins as possible. Additionally, It is recommended to keep the input/output traces as short as possible, and keep the area underneath the isolators free from ground and signal planes. Any galvanic or metallic connection between the side "1" and side "2" will defeat the isolation. The PCB designer should follow these critical recommendations to get the best performance from the design.

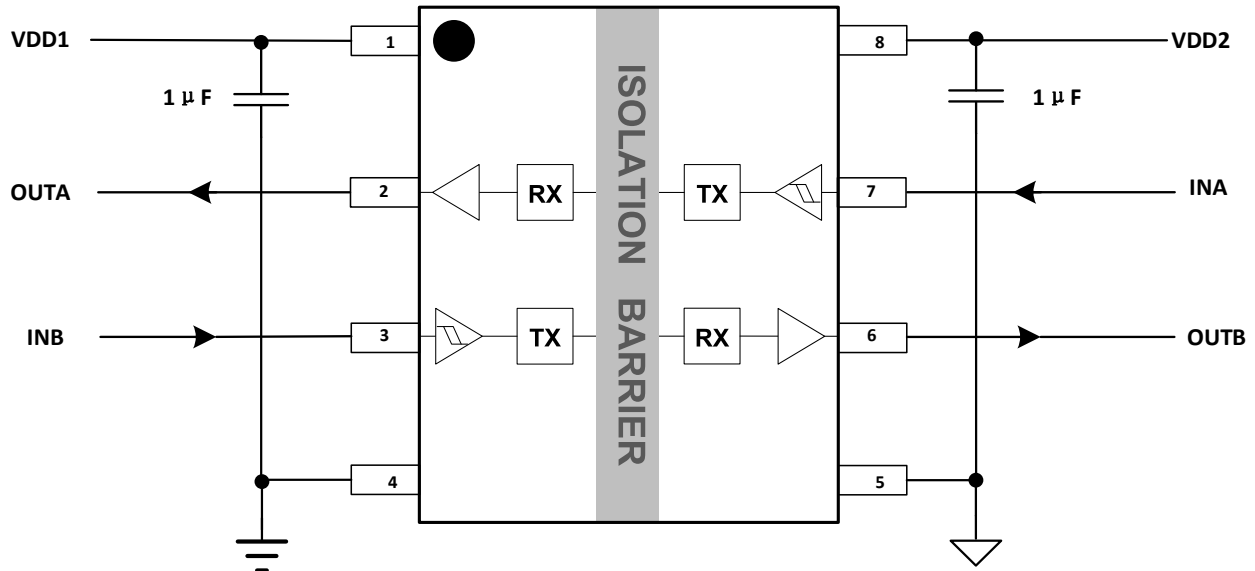


Figure10-1 CS817x22HS/LS typical operating circuit

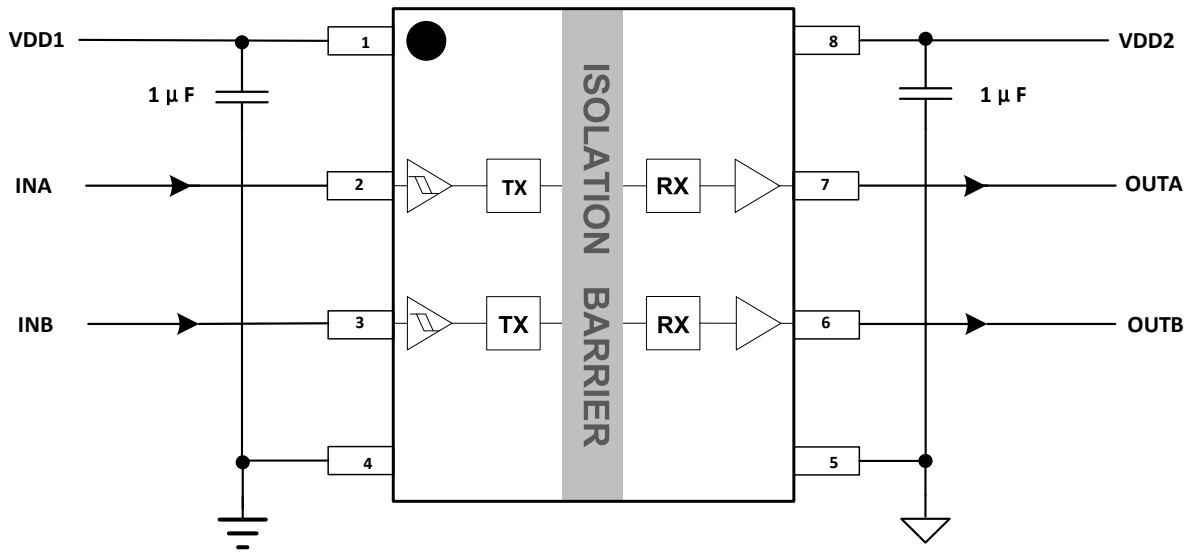
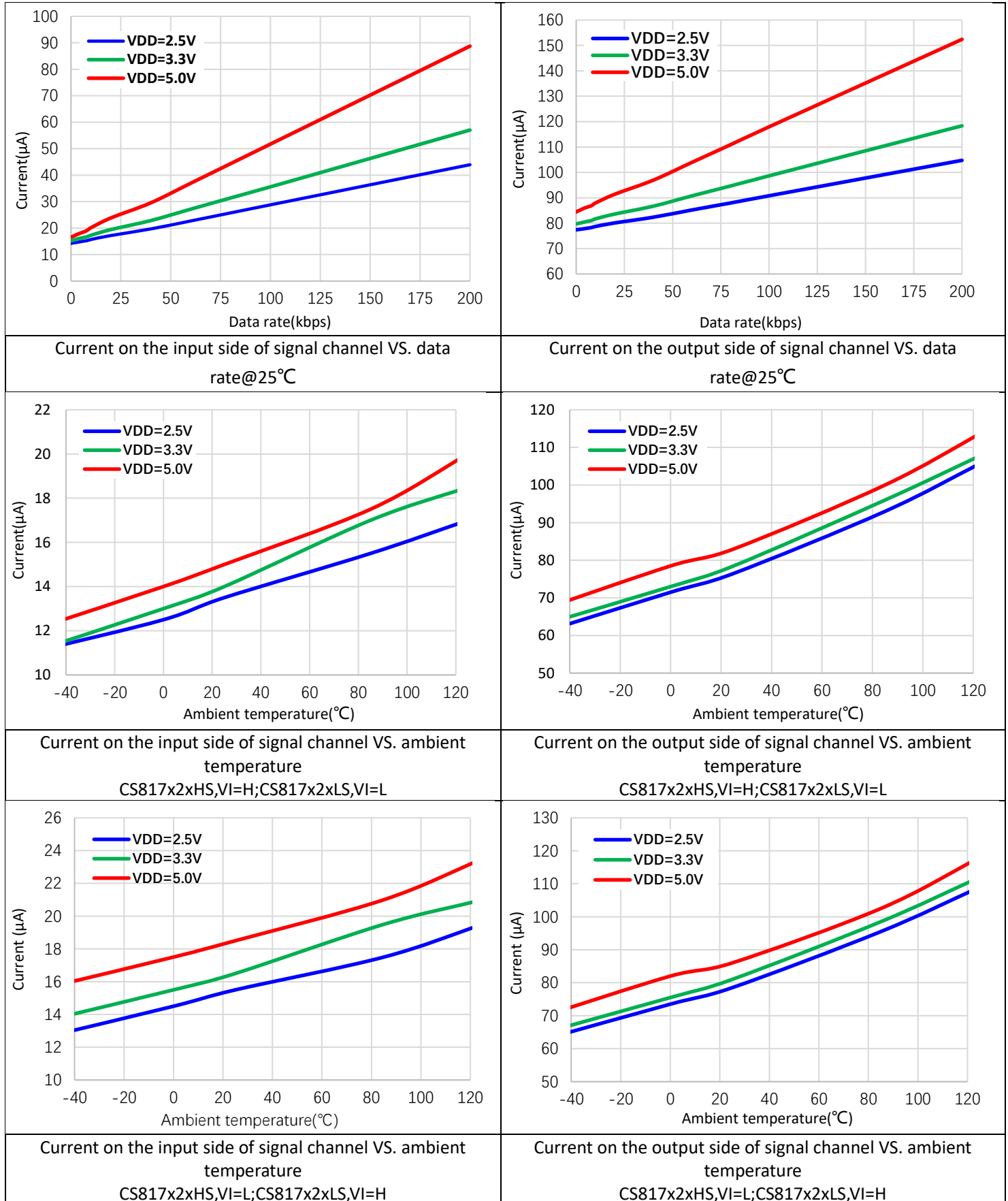
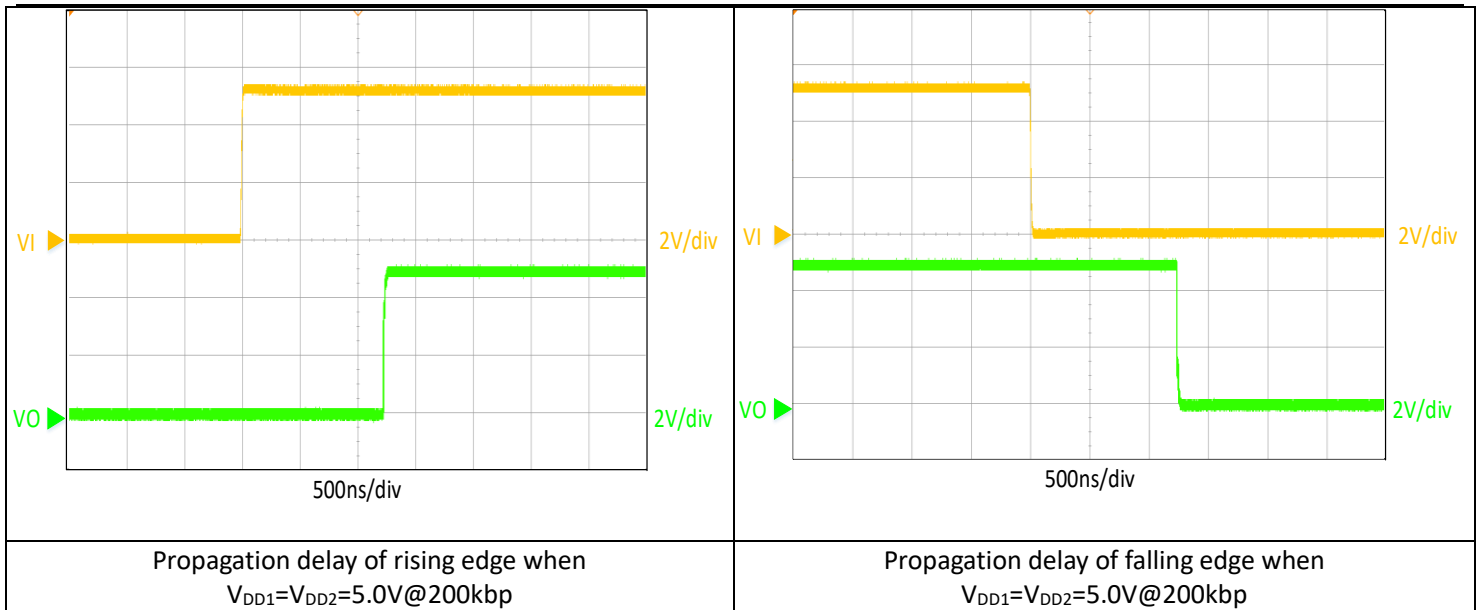


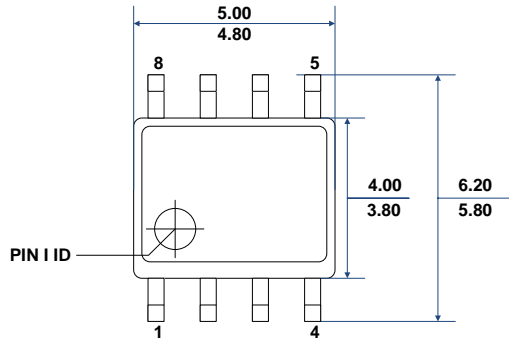
Figure10-2 CS817x20HS/LS typical operating circuit

11. Typical Waveforms and Curves


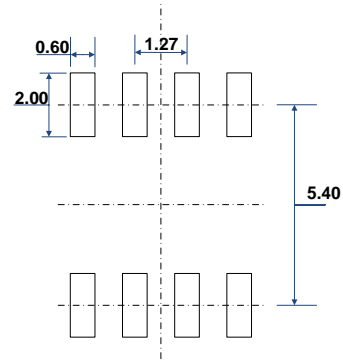


12. Package Information

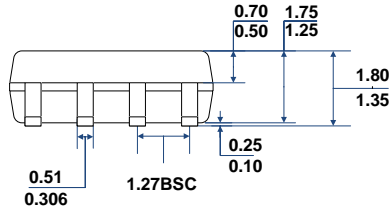
SOIC8 Narrow Body SOIC Package Outline



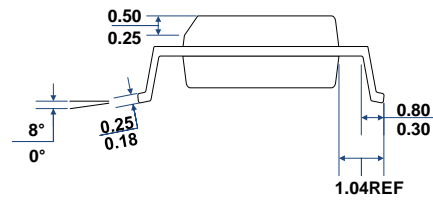
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

13. Soldering Temperature (reflow) Profile

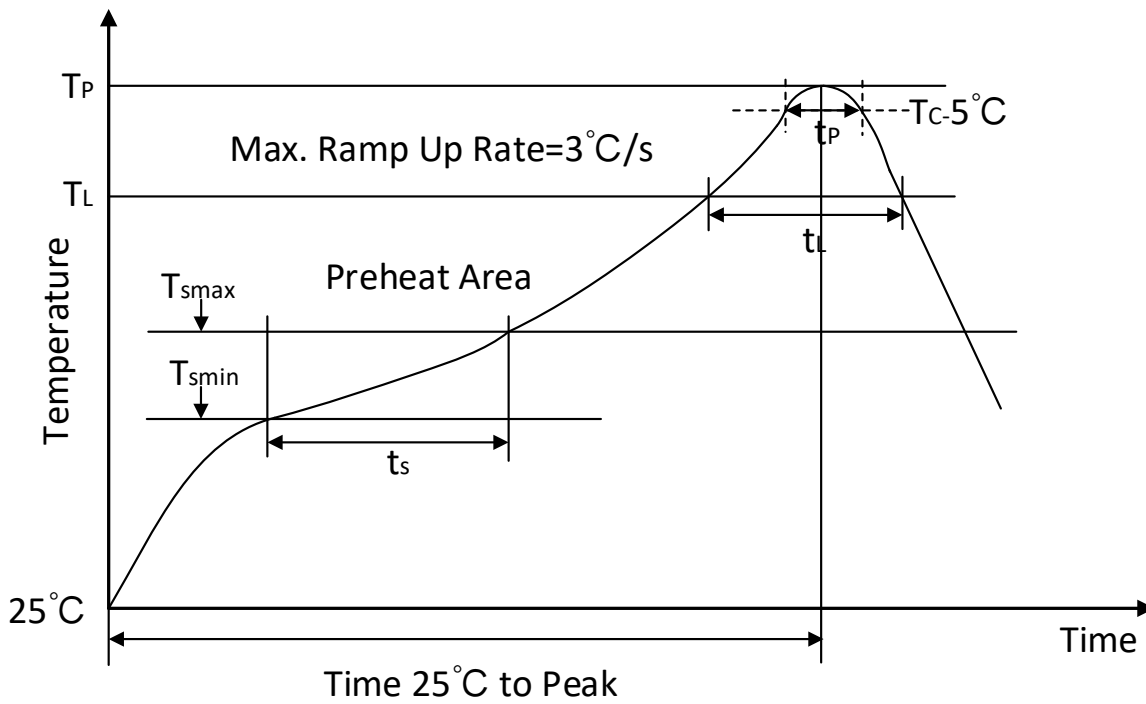
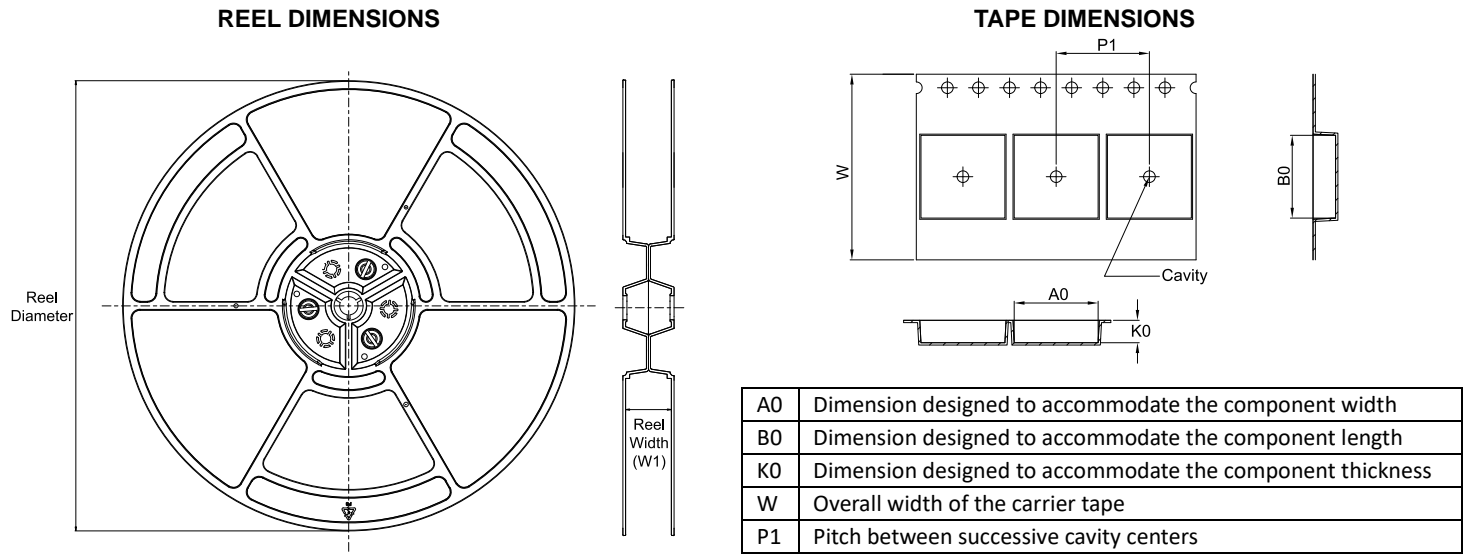


Figure 13- 1 Soldering Temperature (reflow) Profile

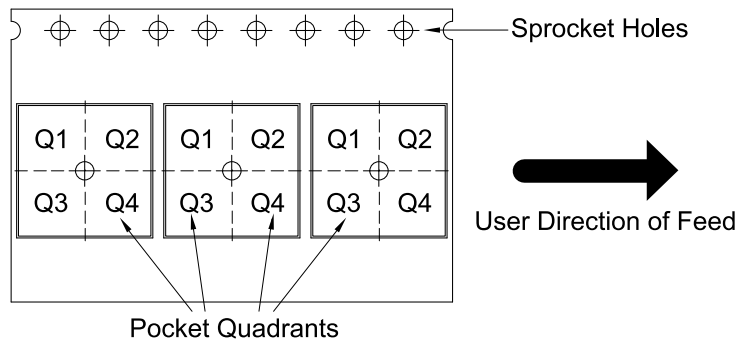
Table 13- 1 Soldering Temperature Parameter

Profile Feature	Pb-Free Assembly
Average ramp-up rate (217°C to Peak)	3°C/second max
Time of Preheat temperature (from 150°C to 200°C)	60-120 second
Time to be maintained above 217°C	60-150 second
Peak temperature	260 +5/-0°C
Time within 5°C of actual peak temp	30 second
Ramp-down rate	6°C/second max.
Time from 25°C to peak temp	8 minutes max

14. Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CS817x20HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS817x20LS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS817x22HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS817x22LS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

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