3.0V to 5.5V RS485/RS422 Transceiver with ±15kV ESD Protection

1. Features

- **High-Performance and Compliant with RS-485 EIA/ TIA-485 Standard**
  - High-Speed Data Rates: 20Mbps
  - 1/8 Unit Load Enables up to 256 Nodes on the Same Bus
- **Integrated Protection for Robust Communication**
  - ±30V Fault Protection Range on Driver Outputs/Receiver Inputs
  - ±15V Common-Mode Voltage Range
  - ±15kV Human Body Model ESD Protection
  - Hot-Swap Input Eliminates False Transitions during Power-up or Power-down
  - Short-Circuit Protection
  - Thermal Shutdown
  - True Fail-Safe Guarantees Known Receiver Output State
- **Low Power**
  - 960μA (max.) @ Receive Mode
  - Shutdown Current < 5μA
- **3.0V to 5.5V Supply Voltage Range**
- **Wide Operating Temperature Range: –40°C to 125°C**
- **14 pin SOIC Package**

2. Applications

- Motor Driver
- Industrial Automation and Control
- Power Grid Infrastructure
- Building Automation
- HVAC System
- Video Surveillance
- Process Control
- Wireless Infrastructure

3. Description

The CA-IF4220NF is low-power, full-duplex transceiver for RS-485/RS-422 communications in harsh environments. This device features ±30V fault protection for overvoltage conditions on the bus lines that ensure robust protection for the communication interface. It also has ±15V wide common-mode range (CMR), this feature was specifically designed for systems where there is a large common-mode voltage present due to either nearby electrically noisy equipment or large ground differences due to different grounds or long-distance transmission. The bus pins are protected against ±15kV electro-static discharge (ESD) shocks, eliminating the need for additional system level protection components.

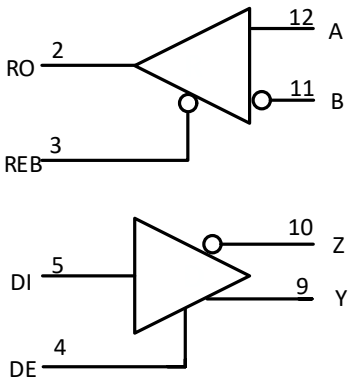
The CA-IF4220NF contains one driver (TX) and one receiver (RX), operates over the +3.0V to +5.5V supply range, making it convenient for designers to use one part with either +3.3V or +5V supply systems. The CA-IF4220NF can transmit and receive at data rate up to 20Mbps. It also includes fail-safe circuitry, guaranteeing a logic-high receiver output when the receiver inputs are shorted or open.

The CA-IF4220NF is specified over the -40°C to +125°C wide operating temperature range and is available in 14-pin SOIC package for industry drop-in compatibility.

Device Information

Part Number	Package	Package Size (Nom.)
CA-IF4220NF	SOIC14	3.9mm x 8.65mm

CA-IF4220NF Simplified Schematic Diagram



4. Ordering Information

Table 4-1. Ordering Information

Part #	Full/Half-Duplex	Data Rate (Mbps)	Number of Nodes on Bus	Package
CA-IF4220NF	Full duplex	20	256	14-pin SOIC

Contents

5. **Revision History**

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A

6. Pin Configuration and Descriptions

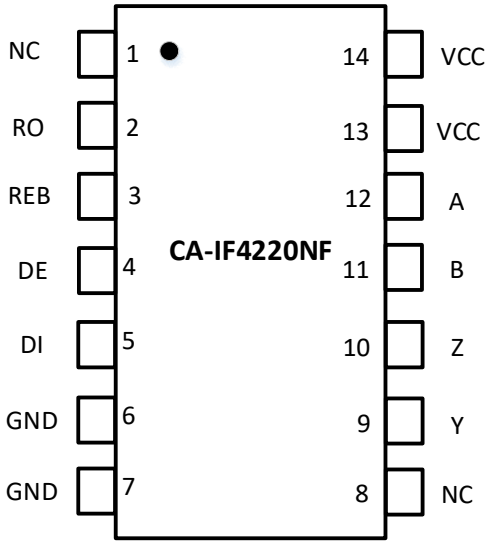


Figure 6-1. CA-IF4220NF pin configuration

Table 6-1. CA-IF4220NF pin description

Pin Name	Pin Number	Description
RO	2	Receiver data output. With REB low, RO is high when (V_A –V_B) > V_{TH+} and is low when (V_A – V_B) < V_{TH-}. RO is high impedance when REB is high.
REB	3	Receiver output enable. Drive REB low or connect to GND to enable RO. Drive REB high to disable the receiver and put RO in high impedance. Drive REB high and DE low to force the IC into low-power shutdown mode.
DE	4	Driver output enable. Drive DE high to enable the driver. Drive DE low or connect to GND to disable the driver. Drive REB high and DE low to force the IC into low-power shutdown mode.
DI	5	Driver data input. With DE high, a logic low on DI forces the noninverting output (Y) low and the inverting output (Z) high; a logic high on DI forces the noninverting output high and the inverting output low.
GND	6, 7	Ground.
Y	9	Noninverting RS-485/RS-422 driver output.
Z	10	Inverting RS-485/RS-422 driver output.
B	11	Inverting RS-485/RS-422 receiver input.
A	12	Noninverting RS-485/RS-422 receiver input.
NC	1, 8	No Connection. Not internally connected.
V_{CC}	13, 14	Power supply input. Bypass V_{CC} to GND with at least 0.1μF capacitor as close to the device as possible.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Min	Max	Unit
V_{CC}	Power supply voltage	-0.3	7.0	V
V_{IO}	Voltage at A, B, Z, Y	-30	30	V
V_{IO}	Voltage at DI, DE, REB	-0.3	7.0	V
V_{IO}	Voltage at RO	-0.3	V_{CC}+0.3	V
T_J	Operating junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

Parameters		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pin[1]	±15	kV
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, other pin[1]	±6	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2	kV

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

Parameters		Min	Typ	Max	Unit
V_{CC}	Analog power supply	3	5	5.5	V
V_{IN}	Input voltage at bus terminal	-15		15	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V
R_L	Differential load resistance	54			Ohm
$1/t_{UI}$	Data rate			20	Mbps
T_A	Ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

7.4. Thermal Information

Thermal Metric		CA-IF4220NF SOIC14	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	°C/W

7.5. Electrical Characteristics

All typical specs are at VCC = 5V, TA = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test Conditions		Min	Typ	Max	Unit
Driver							
$\|V_{OD}\|$	Differential-output voltage	R_L =60Ω, -15V≤V_{test}≤15V (See Figure 8-1)(1)		1.5	3.5		V
		R_L =60Ω, -15V≤V_{test}≤15V, 4.5V≤V_{CC}≤5.5V (See Figure 8-1)		2.1			
		R_L=100Ω (See Figure 8-2)		2	4		V
		R_L=54Ω (See Figure 8-2)		1.5	3.7		V
$\Delta\|V_{OD}\|$	Change in differential-output voltage	R_L=54Ω (See Figure 8-2)		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	-7V≤V_O≤12V		-250		250	mA
Receiver							
I_I	Bus input current	DE=0V, V_{CC}=0V or 5V	V_I=12V		75	125	uA
			V_I=-7V	-100	-43		uA
		DE=0V, V_{CC}=0V or 5V	V_I=15V		91	125	uA
			V_I=-15V	-200	-97		uA
V_{TH+}	Receiver differential threshold voltage rising	Over common mode range			-100	-20	mV
V_{TH-}	Receiver differential threshold voltage falling			-200	-130		mV
V_{HYS}	Receiver input hysteresis				30		mV
V_{OH}	High-level output voltage	I_{OH}=-4mA		V_{CC}-0.4	V_{CC}-0.2		V
V_{OL}	Low-level output voltage	I_{OL}=4mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O=0V or V_{CC}, REB at V_{CC}		-1		1	uA
Input logic							
VIH	Logic-high input	DI, V_{CC}=5.5V		2			V
VIL	Logic-low input	DI, V_{CC}=4.5V				0.8	V
I_{IN}	Logic input current	3V≤V_{CC}≤5.5V, 0V≤V_{IN}≤V_{CC}		-6.2		6.2	uA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled, REB=0V, DE = V_{CC}, no load		0.4	0.8	1.2	mA
		Driver enabled, receiver disabled, REB=V_{CC}, DE = V_{CC}, no load			0.8	1.2	mA
		Driver disabled, receiver enabled, REB=0V, DE = 0V, no load			700	960	uA
		Driver disabled, receiver disabled, REB=V_{CC}, DE = 0V, D=open, no load			2.4	5	uA
T_{SD}	Thermal shutdown temperature				180		℃

Notes:
1. $|V_{OD}|$ ≥ 1.4 V with T_A > 85°C, V_{test} < -7 V and V_{CC} < 3.135 V.
2. Under any condition, ensure that V_{TH+} is at least V_{HYS} higher than V_{TH-}.

7.6. Switching Characteristics

All typical specs are at VCC = 5V, TA = 25°C, Min/Max specs are over recommended operating conditions unless otherwise specified.

Parameters		Test Conditions	Min	Typ	Max	Unit
Driver						
t_r, t_f	Driver differential output rise/fall time	R_L=54 Ω, C_L=50pF, Figure 8-3	1	3	6	ns
t_{PHL},t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns
Receiver						
t_r, t_f	Output rise/fall time	C_L=15pF, see Figure 8-4		2	6	ns
t_{PHL},t_{PLH}	Propagation delay			25	40	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns

7.7. Typical Characteristics

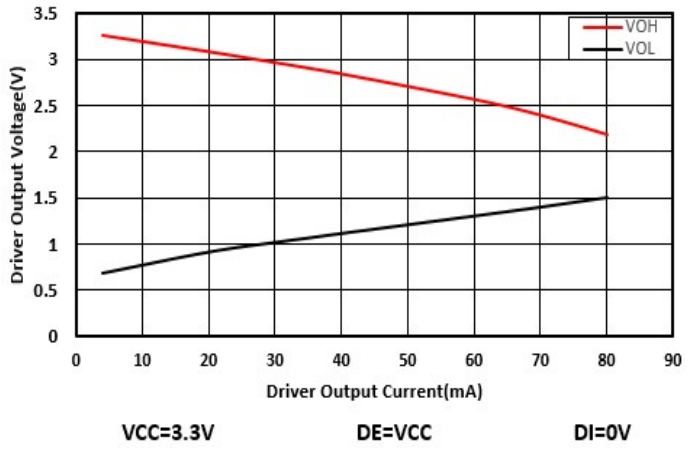


Figure 7-1. Driver Output Voltage vs Driver Output Current

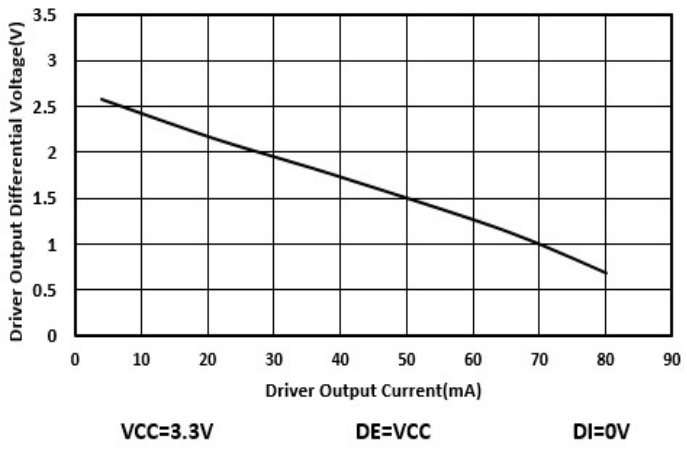


Figure 7-2. Driver Output Differential Voltage vs Driver Output Current

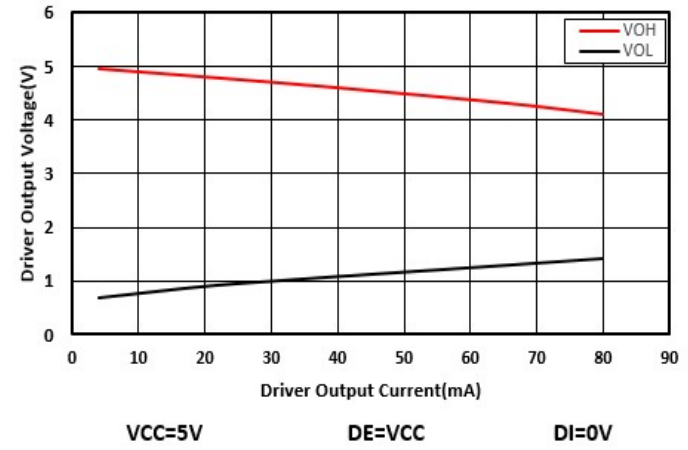


Figure 7-3. Driver Output Voltage vs Driver Output Current

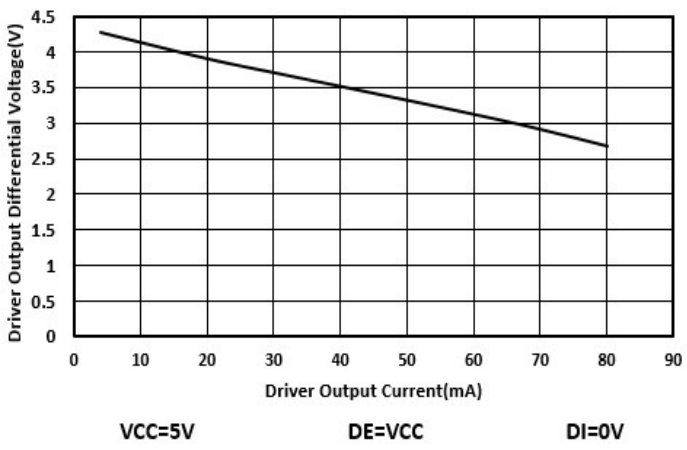


Figure 7-4. Driver Output Differential Voltage vs Driver Output Current

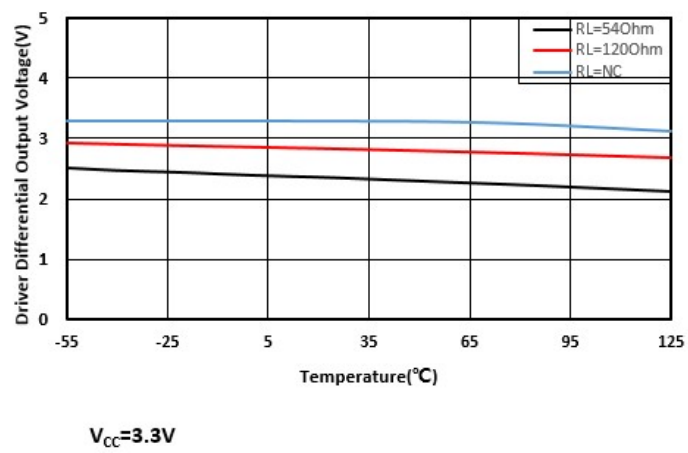


Figure 7-5. V_{OD} vs Temperature

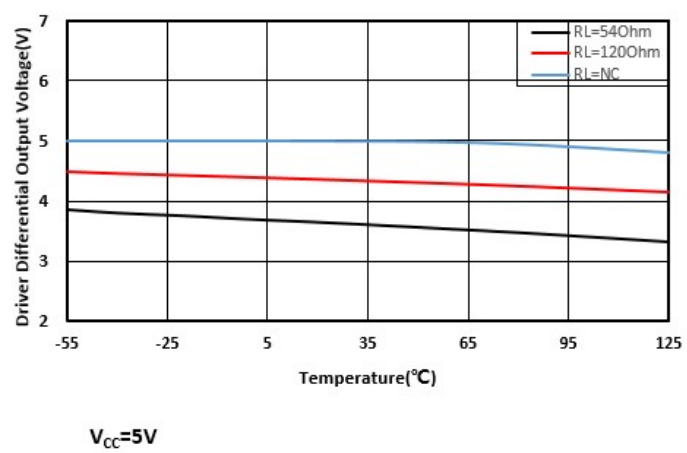


Figure 7-6. V_{OD} vs Temperature

Typical Characteristics (continued)

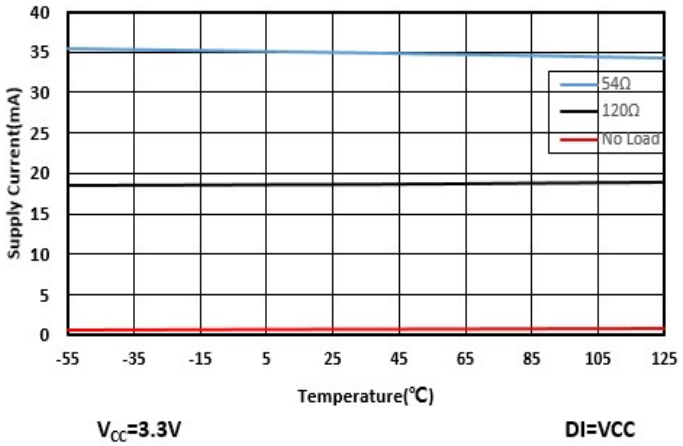


Figure 7-7. Quiescent Current vs Temperature

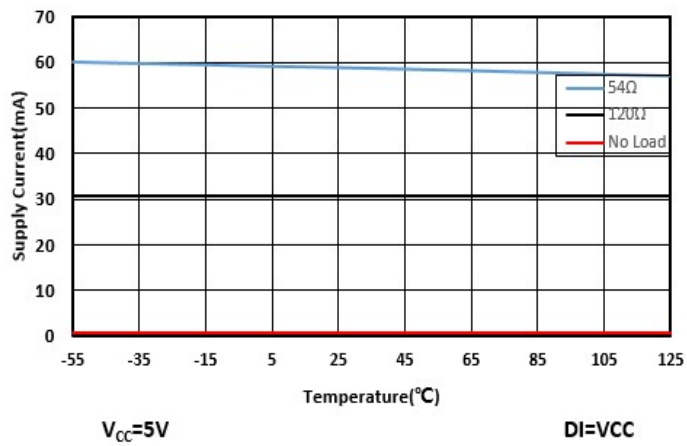


Figure 7-8. Quiescent Current vs Temperature

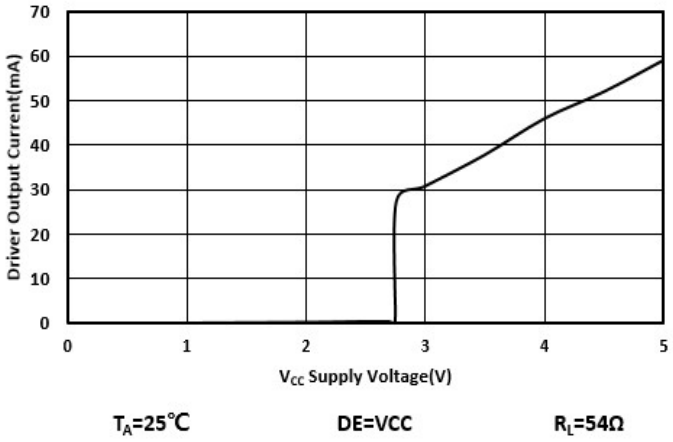
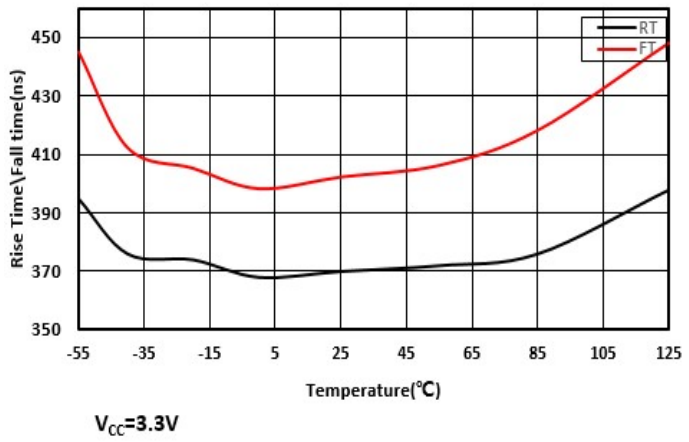


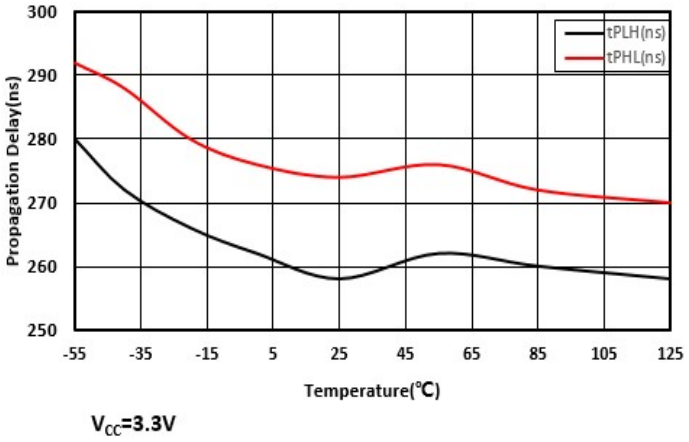
Figure 7-9. Driver Output Current vs Supply Voltage

Typical Characteristics (continued)



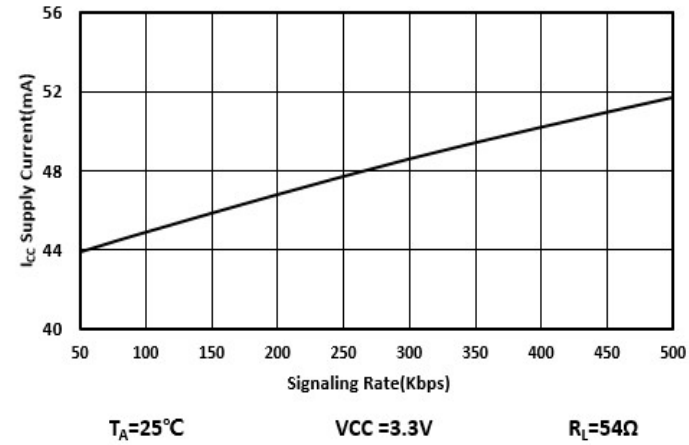
V_{CC}=3.3V

Figure 7-8. Rise Time/Fall Time vs Temperature



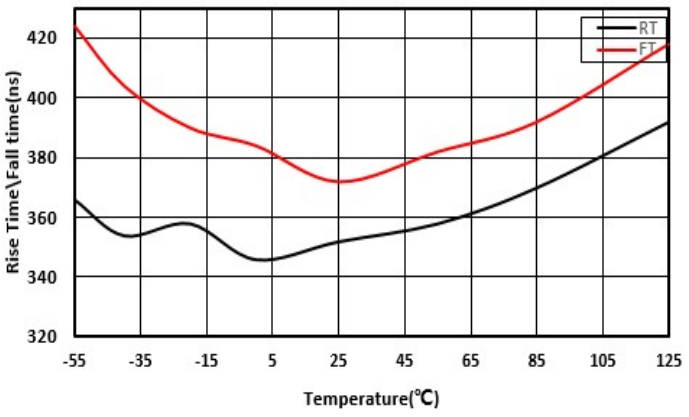
V_{CC}=3.3V

Figure 7-9. Propagation Delay vs Temperature



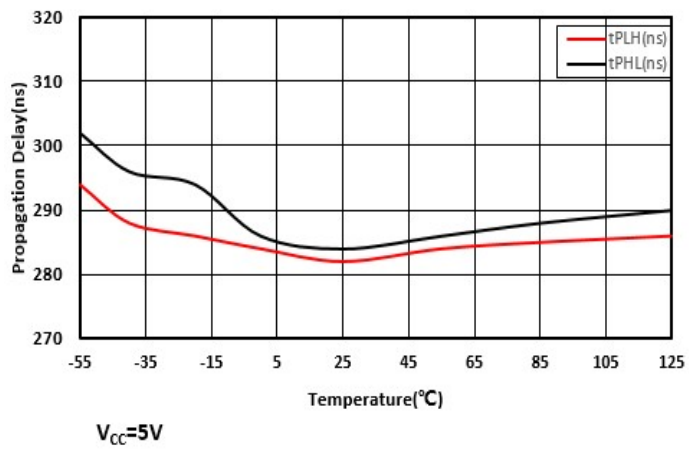
T_A=25℃ VCC =3.3V R_L=54Ω

Figure 7-10. I_{CC} Supply Current vs Signaling Rate



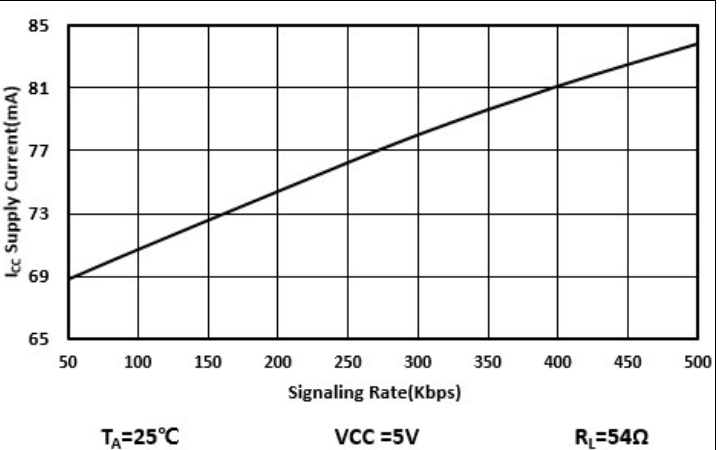
V_{CC}=5V

Figure 7-11. Rise Time/Fall Time vs Temperature



V_{CC}=5V

Figure 7-12. Propagation Delay vs Temperature



T_A=25℃ VCC =5V R_L=54Ω

Figure 7-13. I_{CC} Supply Current vs Signaling Rate

Typical Characteristics (continued)

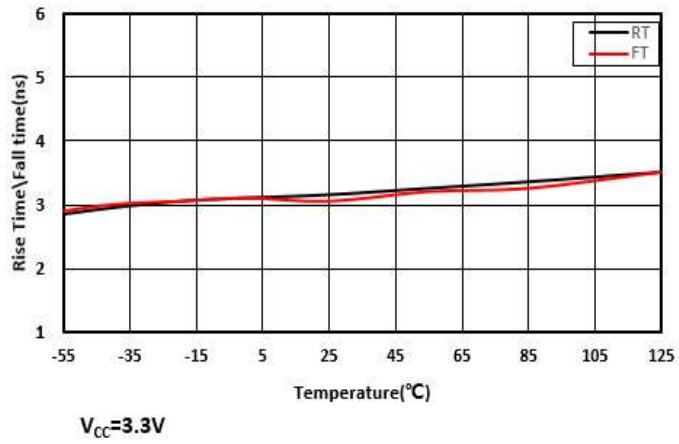


Figure 7-14. Rise Time/Fall Time vs Temperature

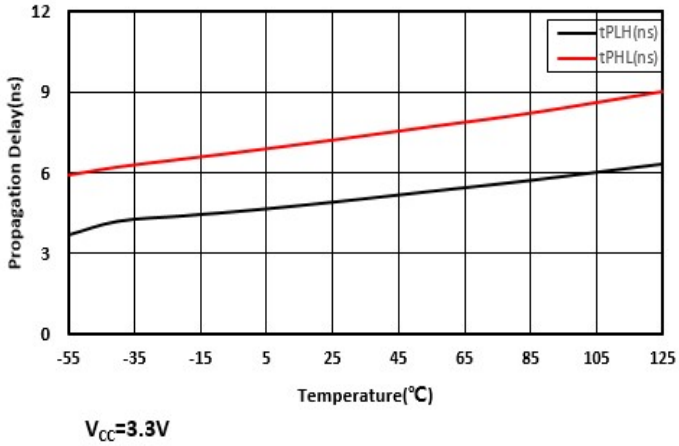


Figure 7-15. Propagation Delay vs Temperature

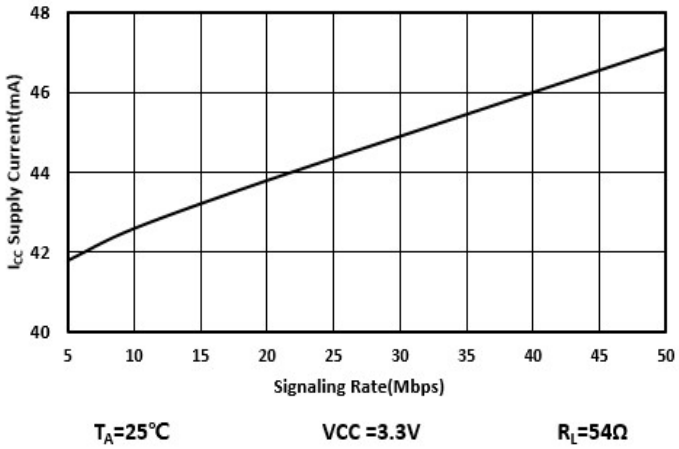


Figure 7-16. I_{CC} Supply Current vs Signaling Rate

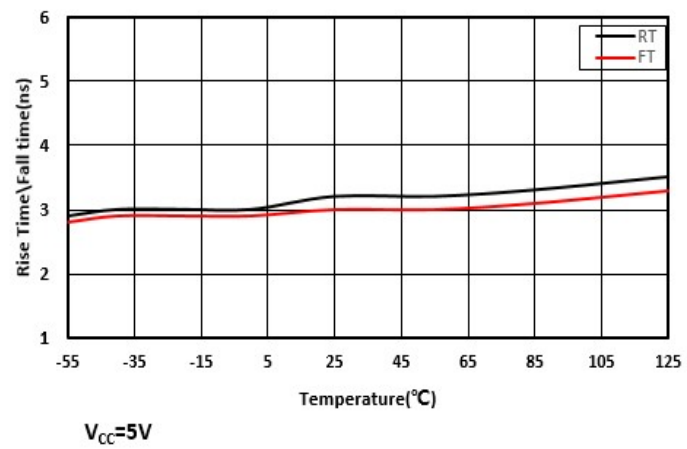


Figure 7-17. Rise Time\Fall Time vs Temperature

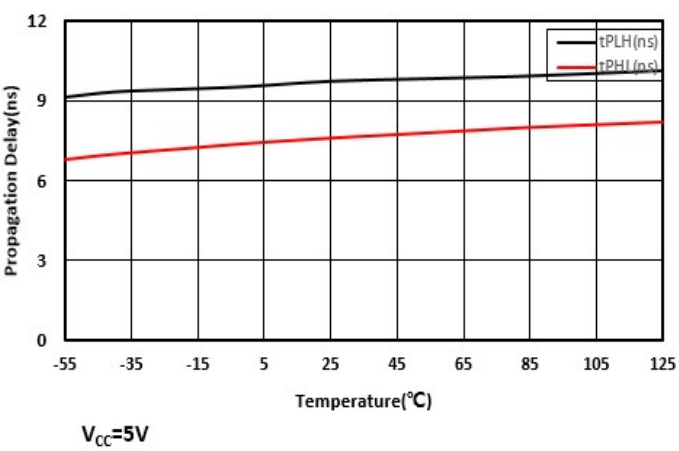


Figure 7-18. Propagation Delay vs Temperature

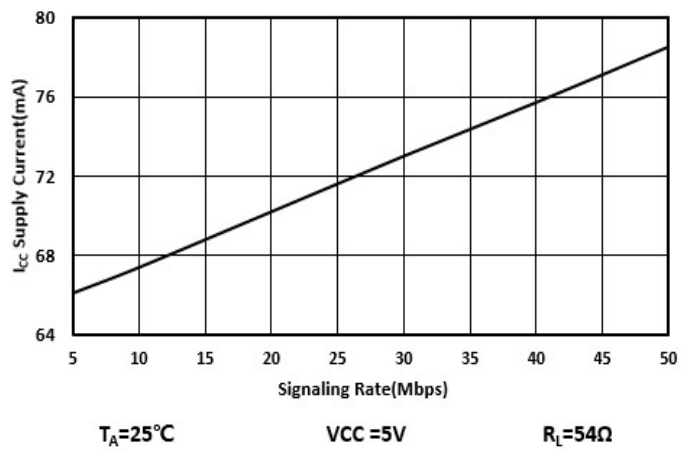


Figure 7-19. I_{CC} Supply Current vs Signaling Rate

8. Parameter Measurement Information

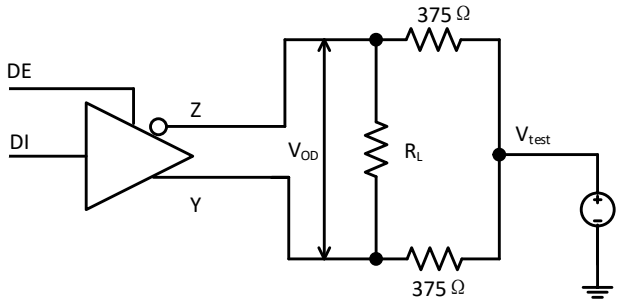


Figure 8-1. Driver Differential Output Voltage with Common-Mode Load

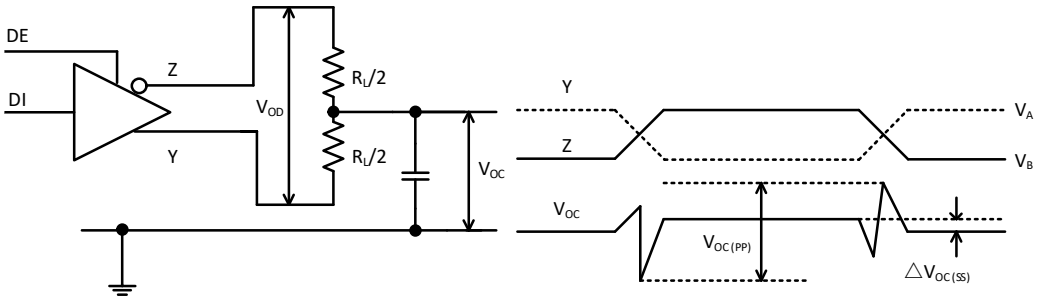


Figure 8-2. Driver Differential and Common-Mode Output with RS-485 Load

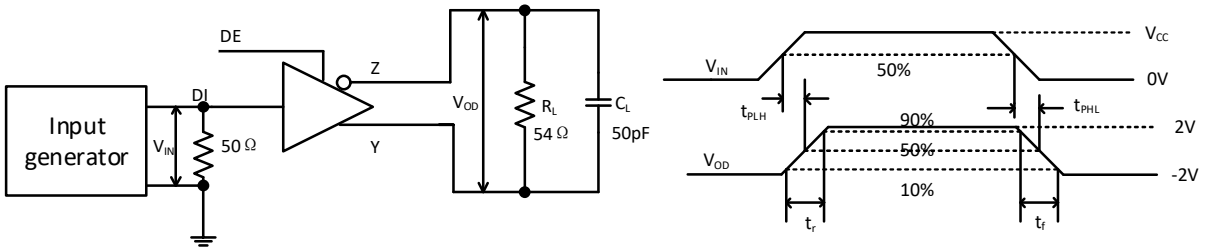


Figure 8-3. Driver Differential Output Rise and Fall Times and Propagation Delays

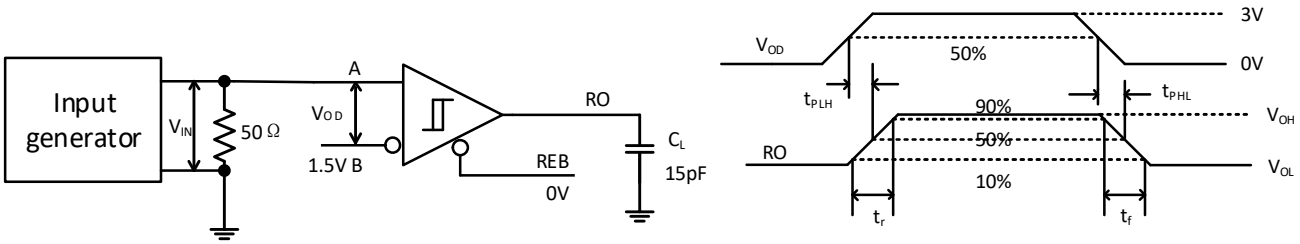


Figure 8-4. Receiver Output Rise and Fall Times and Propagation Delays

9. Detailed Description

9.1. Overview

The CA-IF4220NF device is optimized for full-duplex RS-485/RS-422 applications per the EIA/TIA-485 standard. This device contains one differential driver and one differential receiver. The receiver features a 1/8-unit load input impedance, allowing up to 256 transceivers on a single bus. Driver-enable (DE) and receiver-enable (REB) pins are included on the CA-IF4220NF transceivers. When disabled, the driver and receiver outputs are high impedance.

To reduce system complexity and the need for external protection, the driver outputs/receiver inputs of the CA-IF4220NF device are designed to withstand voltage faults of up to ±30V with respect to ground without damage, and the common-mode range exceeds the standard with ±15V for both the driver and receiver. This device also incorporates a high ESD protection circuit capable of protecting against up to ±15kV of ESD Human Body Model (HBM) for driver outputs and receiver inputs. In addition, two mechanisms against excessive power dissipation caused by faults or bus contention. The first, over-current protection on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state once the junction temperature of the device exceed the thermal shutdown threshold T_{SD} (180°C, typ.). The shutdown condition is cleared when the junction temperature drops to normal operation temperature range of the device.

9.2. Device Functional Modes

For the CA-IF4220NF full-duplex device, the driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485/RS-422 level output on the Y and Z bus lines. Set the driver enable input (DE) low to disable the driver. Y and Z are high impedance when the driver is disabled. Also, the DE pin has internal pull-down to GND, when left open, the driver is disabled as well. The DI pin has an internal pull-up resistor to V_{CC}, thus, when DI left open or a logic high at DI causes Y to turn high and Z to turn low. When DI is low, the output states reverse, Z turns high, Y becomes low. See **Table** for more details.

Table 9-1. CA-IF4220NF Driver Function Table

Input	Enable	Output		Function
DI	DE	Y	Z	
H	H	H	L	Drive bus high
L	H	L	H	Drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Drive bus high by default

Note:
L = Low level; H = High level; Z = high impedance; X = Don't care.

The receiver accepts a differential, RS-485/RS-422 level input on the A and B inputs and transfers it to a single-ended, logic-level output (RO). Drive the receiver enable input (REB) low to enable the receiver. Drive REB high to disable the receiver. RO is high impedance when REB is high. Also, the REB pin has an internal pull-up resistor to V_{CC}, thus, when left open, the receiver is disabled, and RO output is high impedance.

The CA-IF4220NF includes a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to V_{TH+} (-20mV, maximum), RO is logic high. When the input voltage (V_A - V_B) is less than the negative input threshold V_{TH-} (-200mV, minimum), the receiver output RO turns low. See Table for more details.

Table 9-2. CA-IF4220NF Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A - V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	High-level bus state
$V_{TH-} < V_{ID} < V_{TH+}$	L	Indeterminate	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Low-level bus state
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Note:
L = Low level; H = High level; Z = high impedance.

10. Application Information

The CA-IF4220NF full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires) and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. Figure 10-1**Error! Reference source not found.** shows a typical point to point application circuit for CA-IF4220NF.

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. In the multiple transceivers networking or high-speed data transmission applications, to minimize reflections, terminate the line at both ends with a termination resistor, R_T, whose value matches the characteristic impedance (Z_0) of the cable, and keep stub lengths off the main line as short as possible. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

To ensure reliable operation at all data rates and supply voltages, the supply pin should be decoupled with at least 100nF ceramic capacitor located as close to the device as possible. This helps to reduce supply voltage ripple and helps to compensate for the resistance and inductance of the PCB power planes.

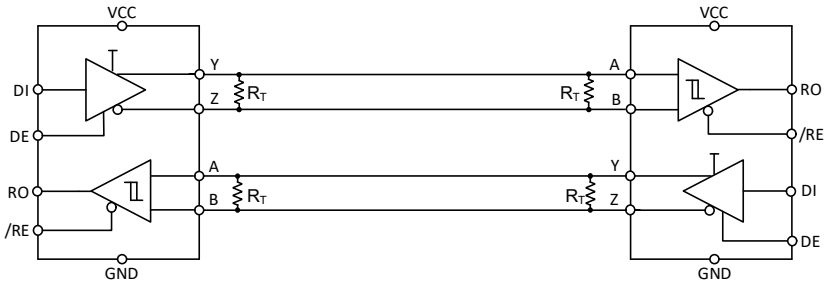
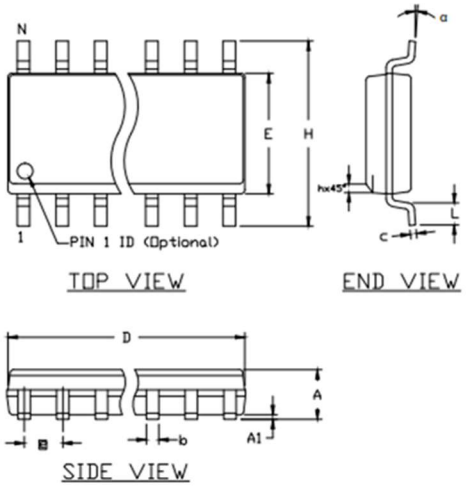


Figure 10-1. Typical RS-485/RS-422 Network With CA-IF4220NF Full-duplex Transceivers

11. Package Information

SOIC14 Package Outline



COMMON DIMENSIONS						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
A	.053	.061	.069	1.35	1.55	1.75
A1	.004	.007	.010	0.10	0.18	0.25
b	.014	.017	.019	0.35	0.42	0.49
c	.007	.009	.010	0.19	0.22	0.25
E	.150	.154	.157	3.80	3.90	4.00
e	.050 BSC			1.27 BSC		
H	.228	.236	.244	5.80	6.00	6.20
L	.016	.033	.050	0.40	0.84	1.27
α	0°	4°	8°	0°	4°	8°
h	0.01	0.015	0.019	0.25	0.38	0.5

* Typical value provided for reference only. This is not a specification.

VARIATION A						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.189	.193	.197	4.80	4.90	5.00
N	8					
MS012	AA					
PKG. CODE	S8+2, S8+2C, S8+4, S8+4C, S8+5, S8+6F, S8+7F, S8+8F, S8+10F, S8+11F, S8+16F, S8+19F, S8+20, S8+21, S8MK+1, S8M+5, S8MS+22, S8+22, S8+23, S8MS+23, S8MS+24					

VARIATION B						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.337	.341	.344	8.55	8.65	8.75
N	14					
MS012	AB					
PKG. CODE	S14+1, S14+1C, S14+4, S14+5, S14+6, S14M+4, S14M+5, S14M+6, S14M+7					

VARIATION C						
SYMBOL	INCHES			MM		
	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.
D	.386	.390	.394	9.80	9.90	10.00
N	16					
MS012	AC					
PKG. CODE	S16+1, S16+1C, S16+3, S16+5, S16+6, S16+8, S16+7F, S16+9F, S16+10F, S16M+3, S16M+6, S16M+11, S16MS+12					

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

12. Soldering Temperature (reflow) Profile

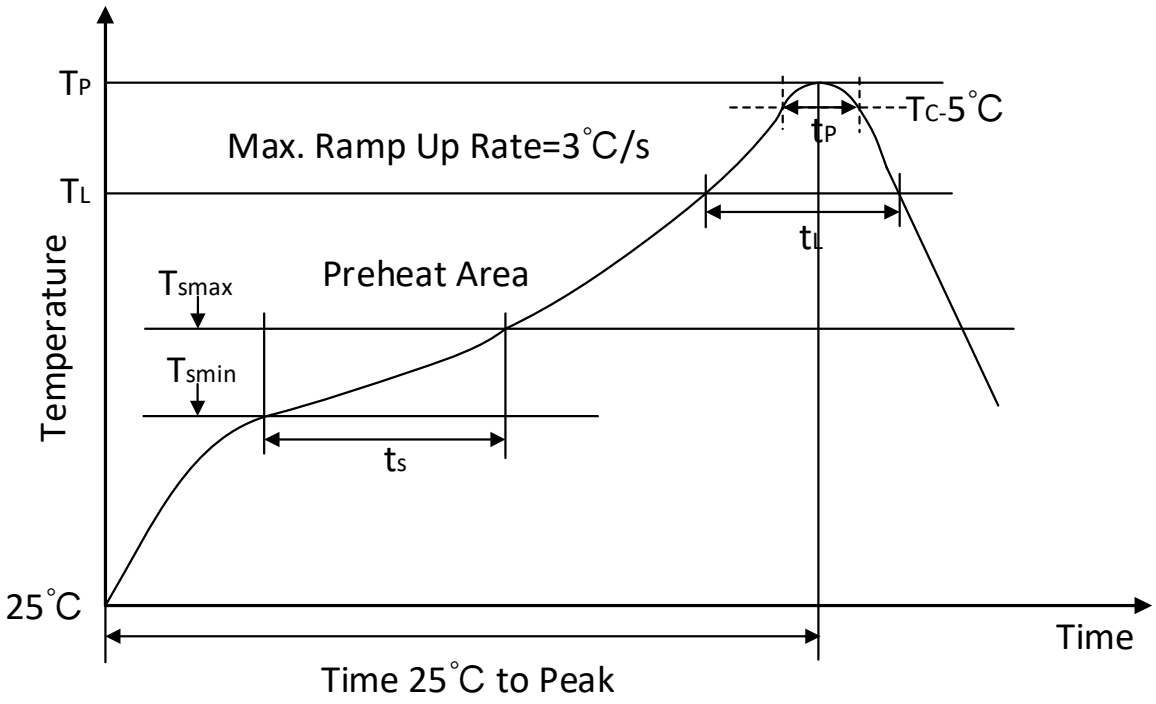


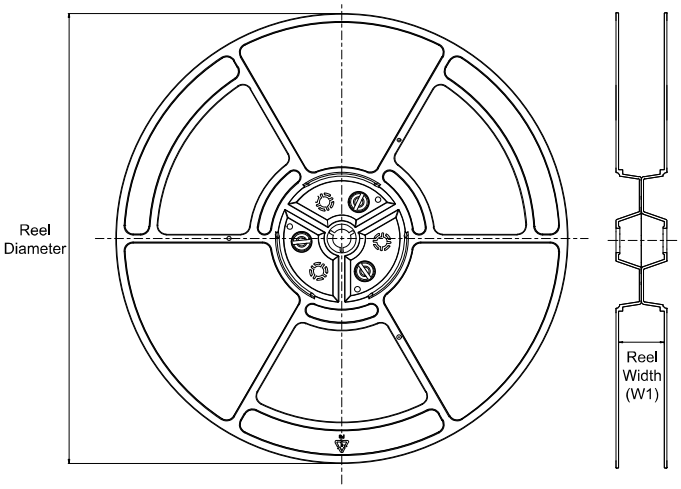
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

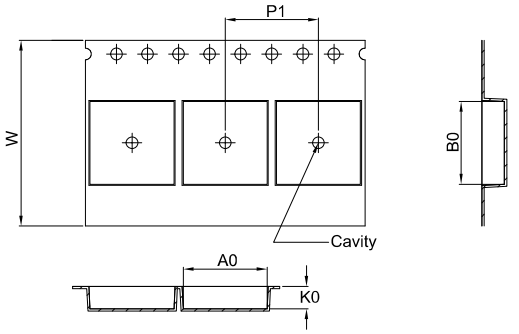
Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L=217°C to peak T_P)	3°C/s max
Time of preheat temperature, 150°C to 200°C	60-120s
Time to be maintained above 217°C	60-150s
Peak temperature	260°C
Time within 5°C of actual peak temperature	30s max
Ramp-down rate (peak T_P to T_L=217°C)	6°C/s max
Time from 25℃ to peak temperature	8min max

13. Tape and Reel Information

REEL DIMENSIONS

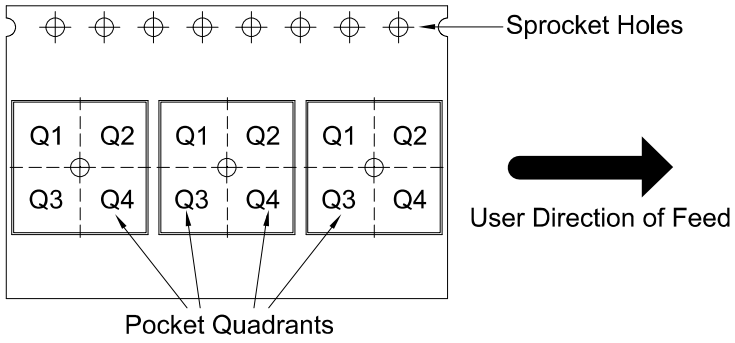


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4220NF	SOIC	NF	14	2500	330	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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