3.3V To 5V RS485/RS422 Transceivers with ±30kV ESD Protection

1. Features

- **High-Performance and Compliant with RS-485 EIA/TIA-485 Standard**
  - Low EMI 500Kbps data rate (CA-IF4805) and up to 50Mbps (CA-IF4850), 20Mbps (CA-IF4820) High-Speed Data Rates
  - 1/8 Unit Load Enables up to 256 Nodes on the Bus
  - 3V to 5.5V Supply Voltage
- **Integrated Protection for Robust Communication**
  - ±30V Fault Protection Range on Driver Outputs/Receiver Inputs
  - Common-Mode Voltage Range: ±15V
  - ±15kV Human Body Model ESD Protection for the Full-duplex Devices (CA-IF48xxF_)
  - ±30kV Human Body Model ESD Protection for the Half-duplex Devices (CA-IF48xxH_)
  - Short-Circuit Protection
  - Thermal Shutdown
  - True Fail-Safe Guarantees Known Receiver Output State
  - Wide Operating Temperature Range: –40°C to 125°C
- **Low Power**
  - 960µA (max.) @ Receive Mode
  - Shutdown Current: < 5µA
- **8 pin SOIC, 8 pin MSOP-8 and 8 pin DFN-8 Packages**

2. Applications

- Motor Drive
- Factory Automation & Control
- Grid Infrastructure
- Home and Building Automation
- Video Surveillance
- Process Control
- Telecommunication Equipment

3. General Description

CA-IF48xx family of devices are low-power transceivers for RS-485 and RS-422 communications in harsh environments. All devices have ±30V fault protection for overvoltage conditions on the communication bus lines that ensure robust protection on the bus. They also feature ±15V of common-mode range (CMR), exceeding the RS-485 standard of -7V to +12V, making them ideal for electrically noisy environments where different systems have shifting ground levels relative to each other and long distance transmission. The bus pins of these devices are protected against ±15kV (for the full-duplex parts) and ±30kV (for the half-duplex parts) electro-static discharge (ESD) shocks, eliminating the need for additional system level protection components.

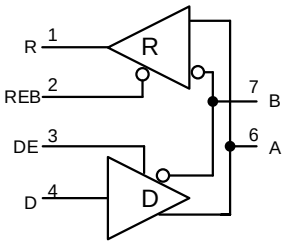
CA-IF48xx family of devices contain one driver and one receiver and operates over the +3V to +5.5V supply range, making it convenient for designers to use one part with either +3.3V or +5V supply voltages.

The CA-IS48xx family devices are specified over the -40°C to +125°C operating temperature range and are available in small 8-pin MSOP, 8-pin DFN packages for space constrained applications and 8-pin SOIC for drop-in compatibility.

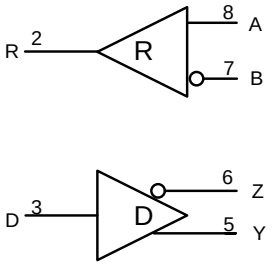
Device Information

Part number	Package	Package size (NOM)
CA-IF48xxxS	SOIC8	3.9mm*4.9mm
CA-IF48xxxM	MSOP8	3mm*3mm
CA-IF48xxxD	DFN8	3mm*3mm

CA-IF4805H Simplified Block Diagram



CA-IF4820F Simplified Block Diagram



4. Ordering Information

Table 4-1 Ordering Information

Part #	Full/Half-Duplex	Data Rate（Mbps）	Number of Nodes on Bus	Package
CA-IF4805HS	Half-Duplex	0.5	256	SOIC8
CA-IF4805FS	Full-Duplex	0.5	256	SOIC8
CA-IF4820HS	Half-Duplex	20	256	SOIC8
CA-IF4820FS	Full-Duplex	20	256	SOIC8
CA-IF4850HS	Half-Duplex	50	256	SOIC8
CA-IF4850FS	Full-Duplex	50	256	SOIC8
CA-IF4805HM	Half-Duplex	0.5	256	MSOP8
CA-IF4805FM	Full-Duplex	0.5	256	MSOP8
CA-IF4820HM	Half-Duplex	20	256	MSOP8
CA-IF4820FM	Full-Duplex	20	256	MSOP8
CA-IF4850HM	Half-Duplex	50	256	MSOP8
CA-IF4850FM	Full-Duplex	50	256	MSOP8
CA-IF4805HD	Half-Duplex	0.5	256	DFN8
CA-IF4805FD	Full-Duplex	0.5	256	DFN8
CA-IF4820HD	Half-Duplex	20	256	DFN8
CA-IF4820FD	Full-Duplex	20	256	DFN8
CA-IF4850HD	Half-Duplex	50	256	DFN8
CA-IF4850FD	Full-Duplex	50	256	DFN8

Contents

5. Pin Configuration and Functions

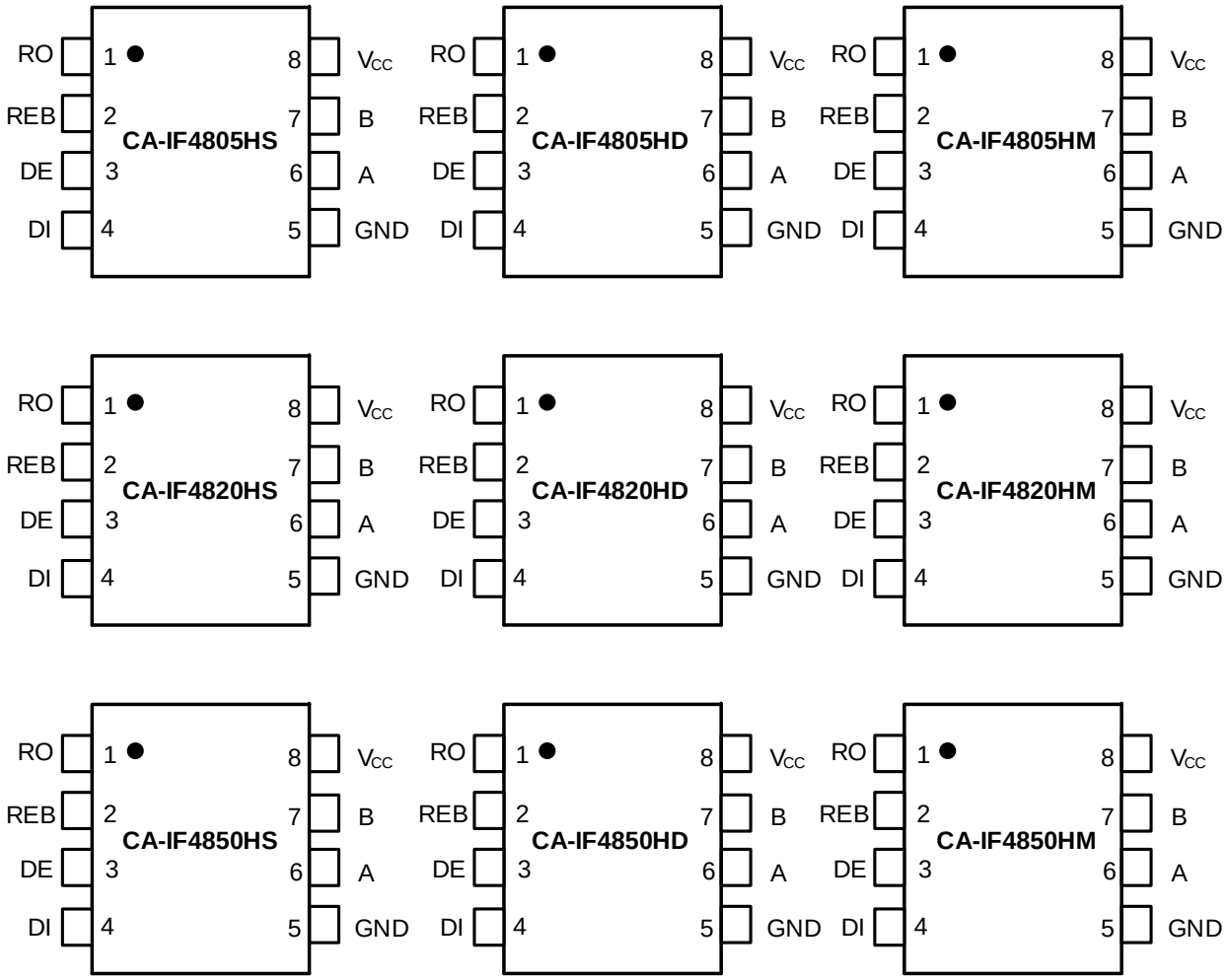


Figure 5-1 CA-IF48xxHS/ CA-IF48xxHD// CA-IF48xxHM pin configuration

Table 5-1 CA-IF48xxHS/ CA-IF48xxHD/ CA-IF48xxHM pin description and function

Pin Name	Pin Number	Description
RO	1	Receiver data output. See the *CA-IF48xxH_ Receiver Function Table* for details. RO is high impedance when REB is high.
REB	2	Receiver output enable. Drive REB low or connect to GND to enable RO. Drive REB high to disable the receiver and put RO in high impedance. Drive REB high and DE low to force the IC into low-power shutdown mode.
DE	3	Driver output enable. Drive DE high to enable the driver. Drive DE low or connect to GND to disable the driver. Drive REB high and DE low to force the IC into low-power shutdown mode.
DI	4	Driver data input. See the *CA-IF48xxH_ Driver Function Table* for details.
GND	5	Ground.
A	6	Noninverting driver output/receiver input.
B	7	Inverting driver output/receiver input.
V_{CC}	8	Power supply input.

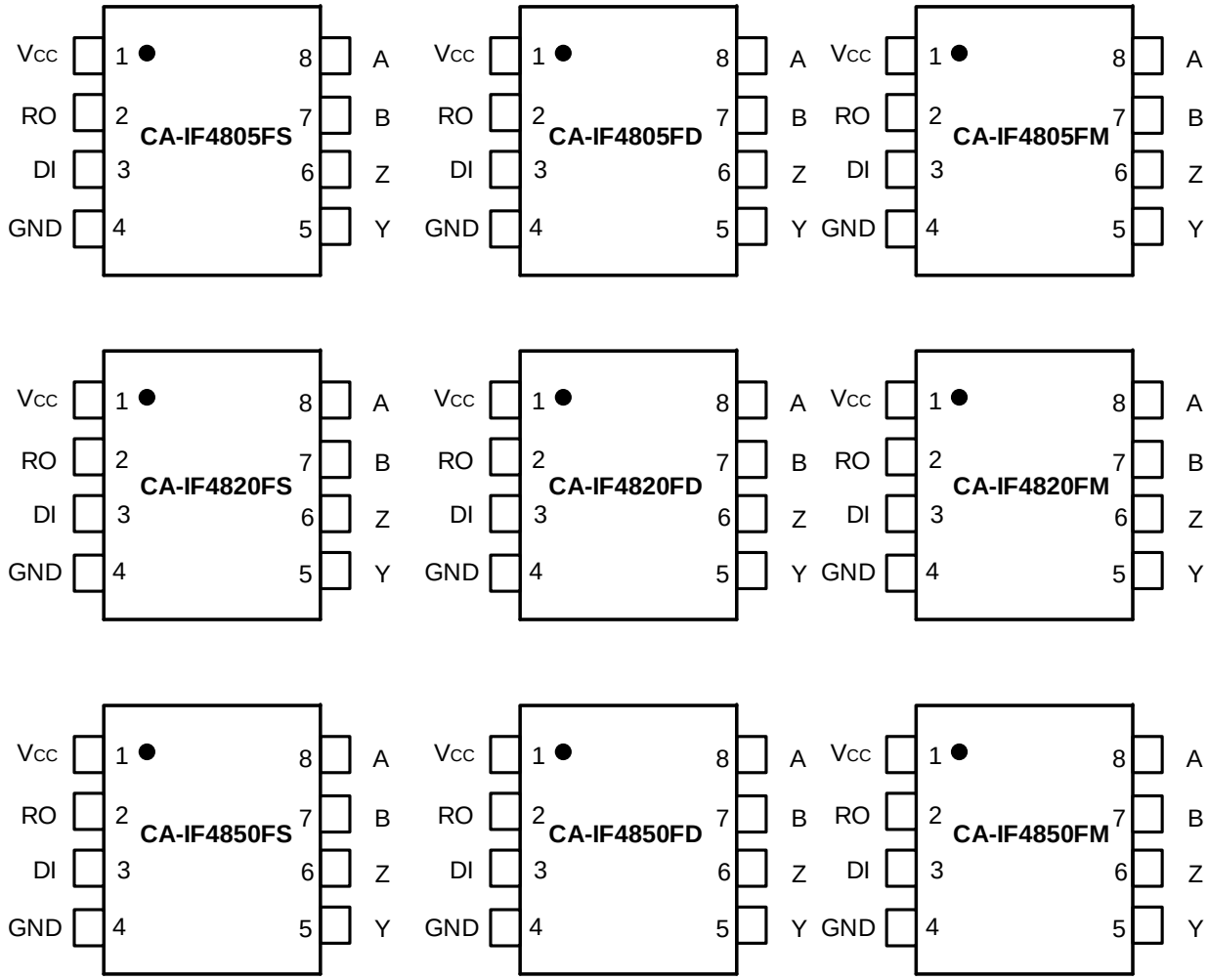


Figure 5-2 CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM pin configuration

Table 5-2 CA-IF48xxFS/CA-IF48xxFD/CA-IF48xxFM pin description and function

Pin Name	Pin Number	Description
V_{CC}	1	Power supply input.
RO	2	Receiver data output. See the *CA-IF48xxF_ Receiver Function Table* for details.
DI	3	Driver data input. See the *CA-IF48xxF_ Driver Function Table* for details.
GND	4	Ground.
Y	5	Noninverting driver output.
Z	6	Inverting driver output.
B	7	Inverting receiver input.
A	8	Noninverting receiver input.

6. Specification

6.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{CC}	Power supply voltage	-0.3	7.0	V
A, B, Y, Z	Voltage on the bus	-30	30	V
DE, DI, REB	Logic control voltage	-0.3	7.0	V
RO	Logic voltage at RO	-0.3	V_{CC}+0.3	V
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. ESD Ratings

Parameters			Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, bus pins[1]	CA-IF48xxF Full-duplexdevices	±15	kV
		CA-IF48xxH Half-duplex devices	±30	kV
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins[1]		±8	kV

Notes:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3. Recommended Operating Conditions

	Parameters	Minimum value	Typical value	Maximum value	Unit
V_{CC}	Power supply	3	5	5.5	V
V_{IN}	Input voltage at any bus terminal	-15		15	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V
R_L	Differential load resistance	54			Ohm
$1/t_{UI}$	Signaling rate：CA-IF4805			500	kbps
$1/t_{UI}$	Signaling rate：CA-IF4820			20	Mbps
$1/t_{UI}$	Signaling rate：CA-IF4850			50	Mbps
T_A	Operating ambient temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

6.4. Thermal Information

THERMAL METRIC		CA-IF48xxHS/FS SOIC8	CA- IF48xxHM/FD MSOP8	CA- IF48xxHM/FD DFN8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

6.5. Electrical Characteristics

Over operating temperature range (unless otherwise noted). All typical values are at 25℃ and supply voltage of V_{CC} = 5 V.

Parameters		Test conditions		Minimum value	Typical value	Maximum value	Unit
Driver							
$\|V_{OD}\|$	Differential output voltage	R_L =60 Ω, -15 V ≤ V_{test} ≤ 15 V (see Figure 6-22)(1)		1.5	3.5		V
		R_L =60 Ω, -15 V ≤ V_{test} ≤ 15 V , 4.5 V ≤ V_{CC} ≤ 5.5 V (see Figure 6-22)		2.1			
		R_L = 100 Ω (see Figure 6-23)		2	4		V
		R_L = 54 Ω (see Figure 6-23)		1.5	3.7		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54 Ω (see Figure 6-23)		-200		200	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			-200		200	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V		-250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5 V	V_I = 12V		75	125	μA
			V_I = -7V	-100	-43		μA
		DE = 0 V, V_{CC} = 0 V or 5V	V_I = 15V		91	125	μA
			V_I =-15V	-200	-97		μA
V_{TH+}	Receiver differential threshold voltage rising	Over common-mode range			-100	-20	mV
V_{TH-}	Receiver differential threshold voltage falling			-200	-130		mV
V_{HYS}	Receiver input hysteresis				30		mV
V_{OH}	Output high voltage	I_{OH} = -8 mA		V_{CC}-0.4	V_{CC}-0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZR}	Output high-impedance current	V_O = 0 V or V_{CC}, REB= V_{CC}		-1		1	μA
Input Logic							
I_{IN}	Logic Input current	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}		-6.2		6.2	μA
Device							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled REB=0V, DE = V_{CC}, No load		0.4	0.8	1.2	mA
		Driver enabled, receiver Disabled REB=V_{CC}, DE = V_{CC}, No load			0.8	1.2	mA
		Driver disabled, receiver enabled REB=0V, DE = 0V, No load			700	960	μA
		Driver and receiver disabled REB=V_{CC}, DE = 0V, D=open, No load			2.4	5	μA
TSD	Thermal shutdown temperature				180		℃

(1) |VOD| ≥ 1.4 V when T_A > 85 ℃, V_{test} < -7 V and V_{CC} < 3.135 V.

(2) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.

6.6. Switching Characteristics

Over operating temperature range (unless otherwise noted). All typical values are at 25℃ and supply voltage of V_{CC} = 5 V.

Parameter		Test Conditions	Minimum value	Typical value	Maximum value	Unit
Driver: CA-IF4805HS/ CA-IF4805HM/ CA-IF4805HD						
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 6-24	250	360	680	ns
t_{PHL},t_{PLH}	Propagation delay			280	500	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				10	ns
t_{PHZ},t_{PLZ}	Disable time			10	200	ns
t_{PZH},t_{PZL}	Enable time	REB = 0V, see Figure 6-25 Figure 6-26		100	600	ns
		REB = V_{CC}, see Figure 6-25 Figure 6-26		7.2	11	us
Receiver: CA-IF4805HS/ CA-IF4805HM/ CA-IF4805HD						
t_r, t_f	Output rise/fall time	C_L = 15 pF, see Figure 6-27		3.8	10	ns
t_{PHL},t_{PLH}	Propagation delay			23	110	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			7	20	ns
$t_{PZH(1)}$,$t_{PZL(1)}$, $t_{PZH(2)}$,$t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 6-28		8	20	ns
		DE = 0 V, see Figure 6-29		7	14	µs
Driver: CA-IF4820HS/ CA-IF4820HM/ CA-IF4820HD						
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 6-24	1	3	6	ns
t_{PHL},t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				3.5	ns
t_{PHZ},t_{PLZ}	Disable time			15	25	ns
t_{PZH},t_{PZL}	Enable time	REB = 0V, see Figure 6-25 Figure 6-26		20	50	ns
		REB = V_{CC}, see Figure 6-25 Figure 6-26		2.5	10	µs
Receiver: CA-IF4820HS/ CA-IF4820HM/ CA-IF4820HD						
t_r, t_f	Output rise/fall time	C_L = 15 pF, see Figure 6-27		3.8	10	ns
t_{PHL},t_{PLH}	Propagation delay			23	110	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			7	20	ns
$t_{PZH(1)}$,$t_{PZL(1)}$, $t_{PZH(2)}$,$t_{PZL(2)}$,	Enable time	DE = V_{CC}, see Figure 6-28		8	20	ns
		DE = 0 V, see Figure 6-29		7	14	µs
Driver: CA-IF4820FS/ CA-IF4820FM/ CA-IF4820FD						
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 6-24	1	3	6	ns
t_{PHL},t_{PLH}	Propagation delay		3	10	20	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				3.5	ns
Receiver: CA-IF4820FS/ CA-IF4820FM/ CA-IF4820FD						
t_r, t_f	Output rise/fall time	C_L = 15 pF, see Figure 6-27		2	6	ns
t_{PHL},t_{PLH}	Propagation delay			25	40	ns
$t_{SK(P)}$	Pulse skew $\|t_{PHL} - t_{PLH}\|$				3.5	ns

6.7. Typical Characteristics: All Devices

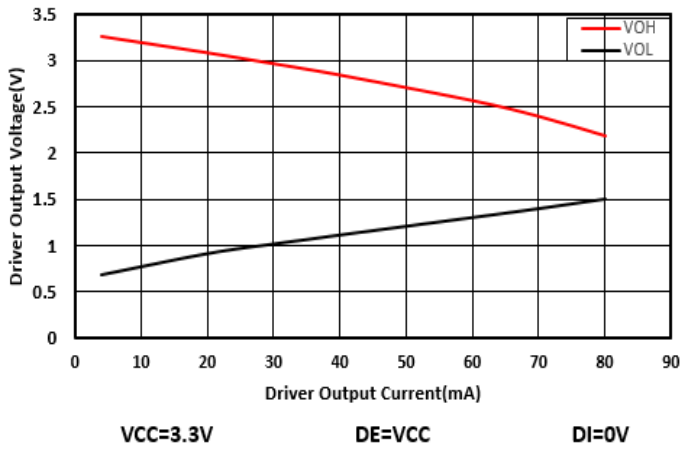


Figure 6-1 Driver Output Voltage vs Driver Output Current

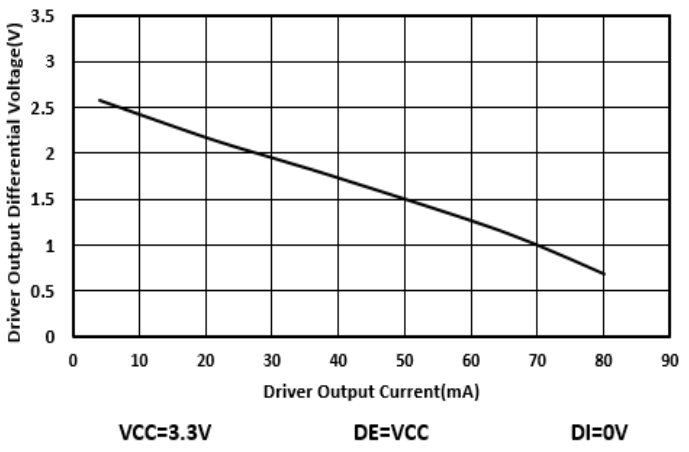


Figure 6-2 Driver Differential Output Voltage vs Driver Output Current

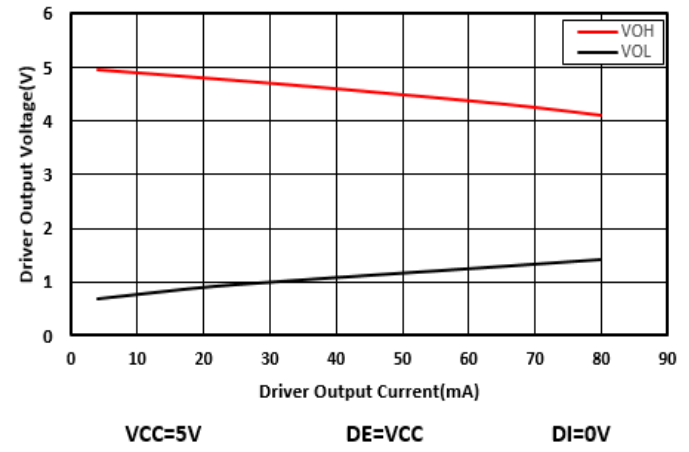


Figure 6-3 Driver Output Voltage vs. Driver Output Current

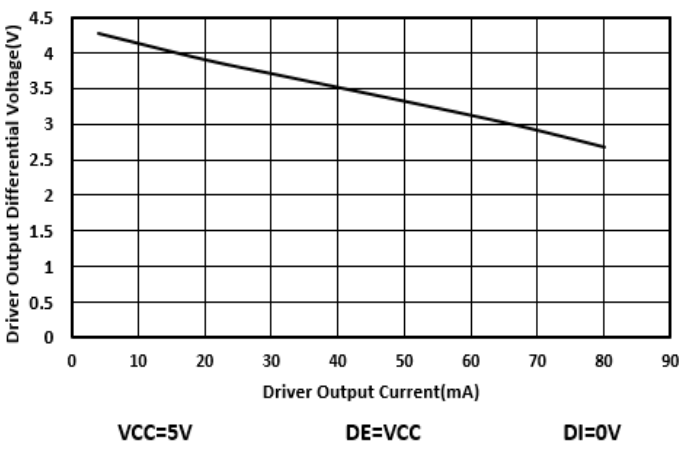


Figure 3-4 Driver Differential Output Voltage vs. Driver Output Current

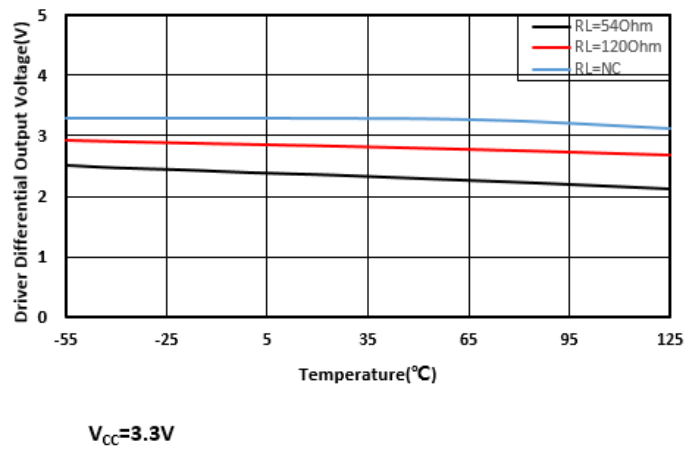


Figure 6-5 Driver Differential Output Voltage vs. Temperature

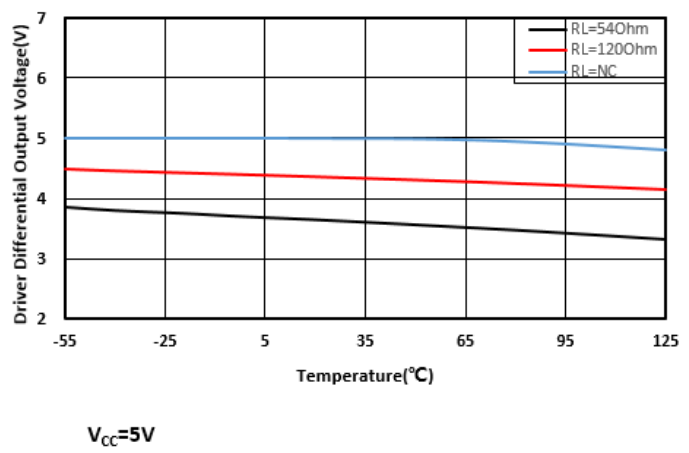


Figure 6-6 Driver Differential Output Voltage vs. Temperature

6.7 Typical Characteristics: All Devices(continued)

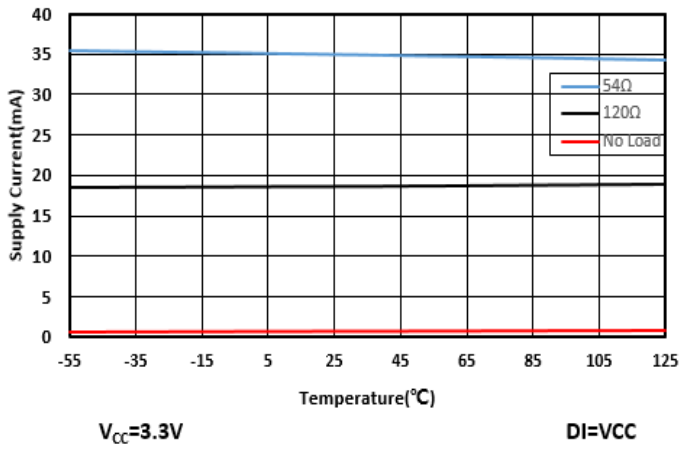


Figure 6-7 Quiescent Current vs. Temperature

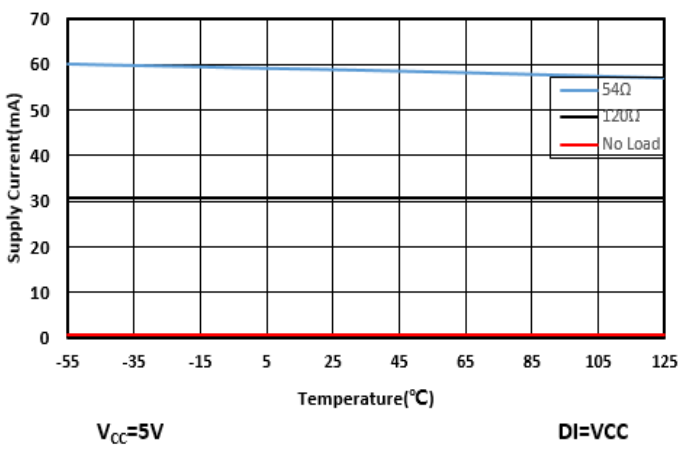


Figure 6-8 Quiescent Current vs. Temperature

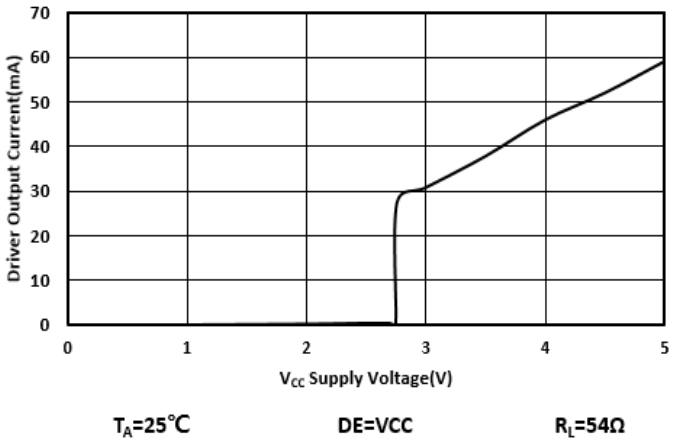
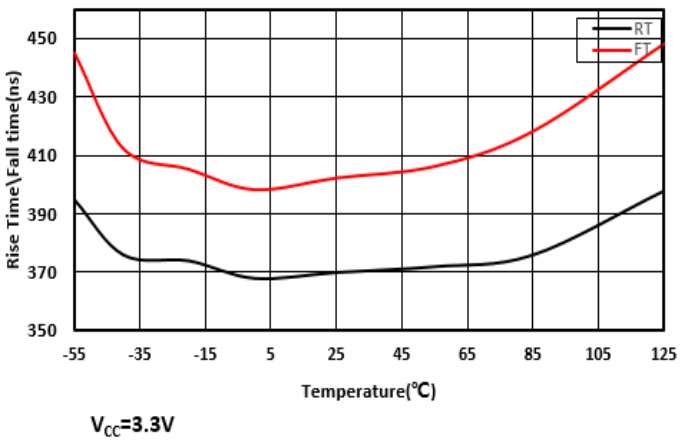


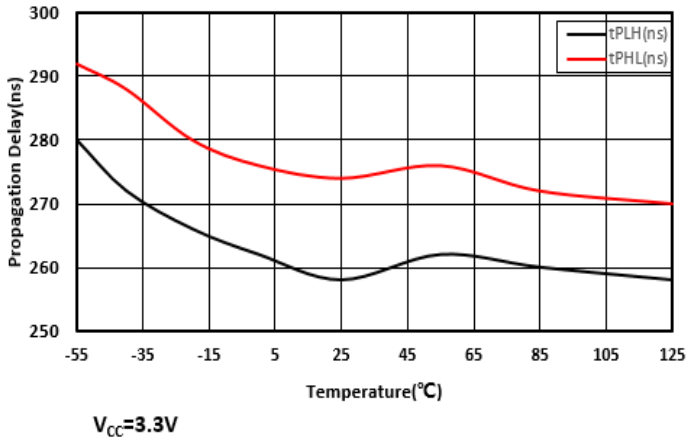
Figure 6-9 Driver Output Current vs. Supply Voltage

6.8. Typical Characteristics: CA-IF4805HS,CA-IF4805FS,CA-IF4805HM,CA-IF4805FM,CA-IF4805HD,CA-IF4805FD



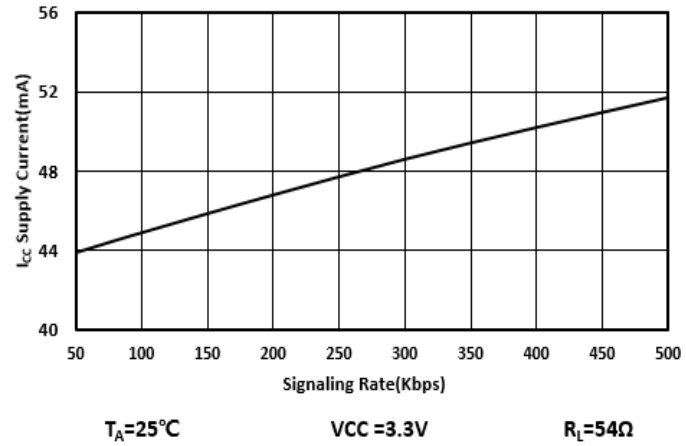
V_{CC}=3.3V

Figure 4 Driver Rise Time\Fall Time vs. Temperature



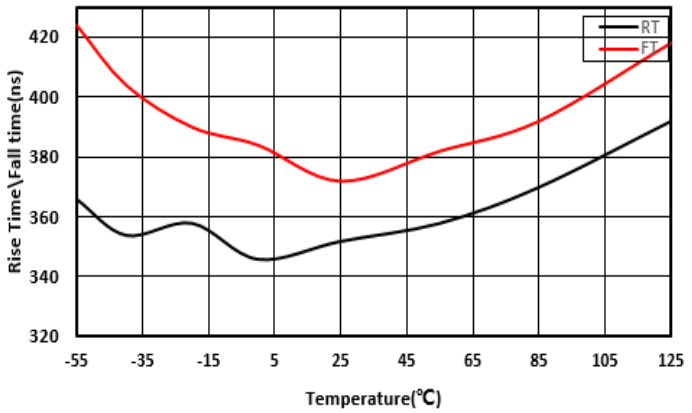
V_{CC}=3.3V

Figure 6-11 Driver Propagation Delay vs. Temperature



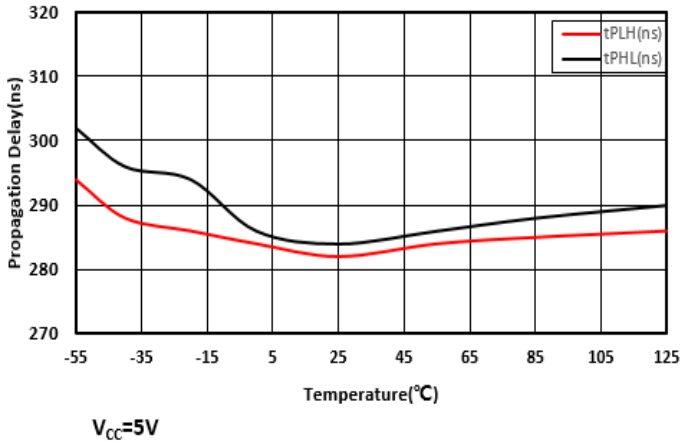
T_A=25℃ VCC =3.3V R_L=54Ω

Figure 6-12 Supply Current vs. Signal Rate



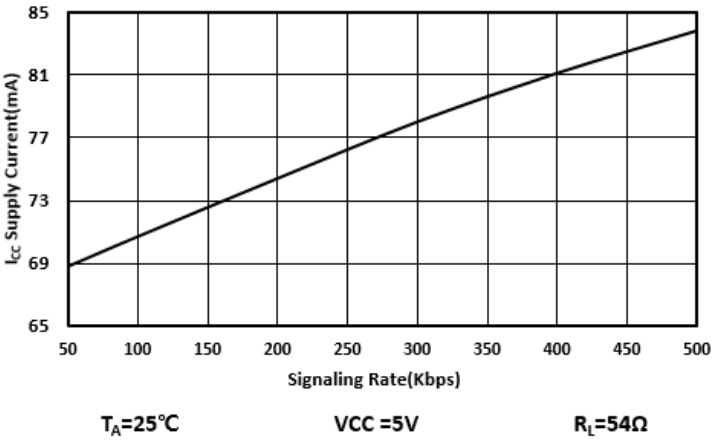
V_{CC}=5V

Figure 6-13 Driver Rise Time\Fall Time vs. Temperature



V_{CC}=5V

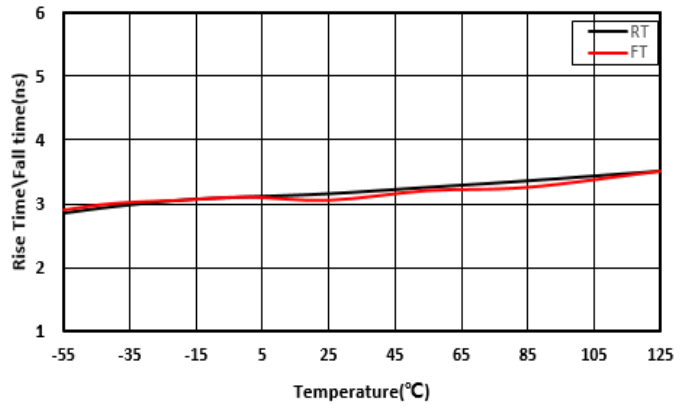
Figure 6-14 Driver Propagation Delay vs. Temperature



T_A=25℃ VCC =5V R_L=54Ω

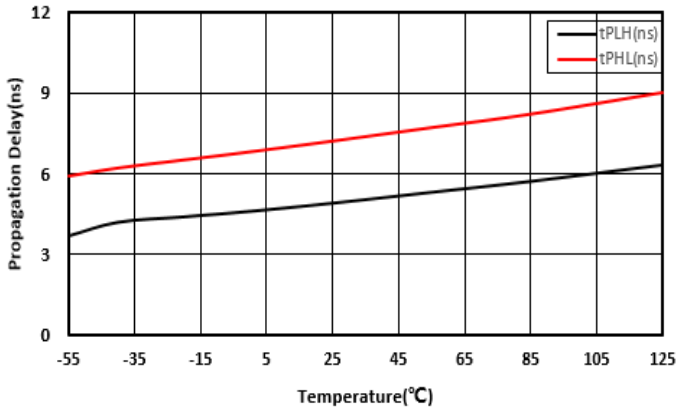
Figure 6-15 Supply Current vs. Signal Rate

6.9. Typical Characteristics: CA-IF4820HS, CA-IF4820FS, CA-IF4820HM, CA-IF4820FM, CA-IF4820HD, CA-IF4820FD



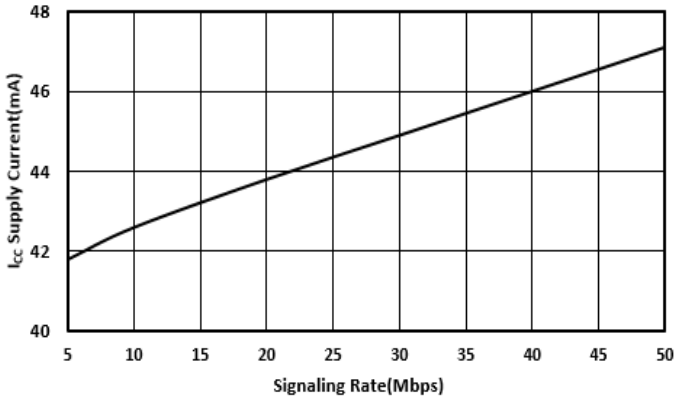
V_{CC}=3.3V

Figure 6-16 Driver Rise Time\Fall Time vs. Temperature



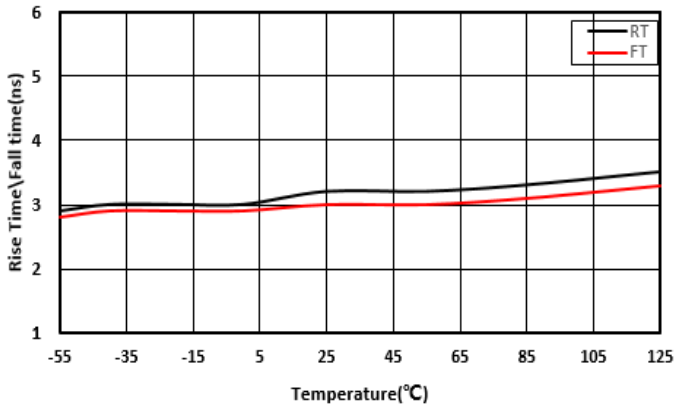
V_{CC}=3.3V

Figure 6-17 Driver Propagation Delay vs. Temperature



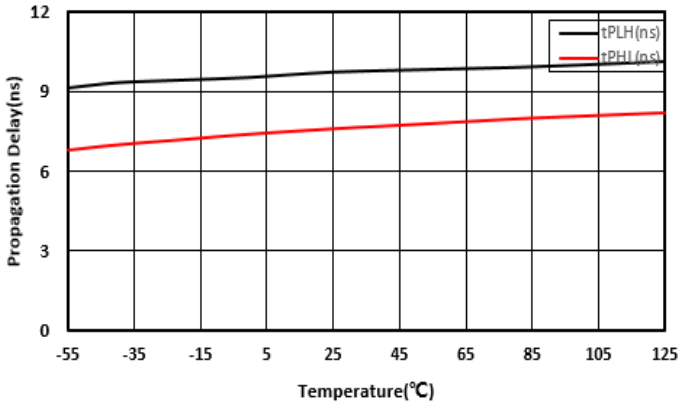
T_A=25℃ VCC =3.3V R_L=54Ω

Figure 6-18 Supply Current vs Signal Rate



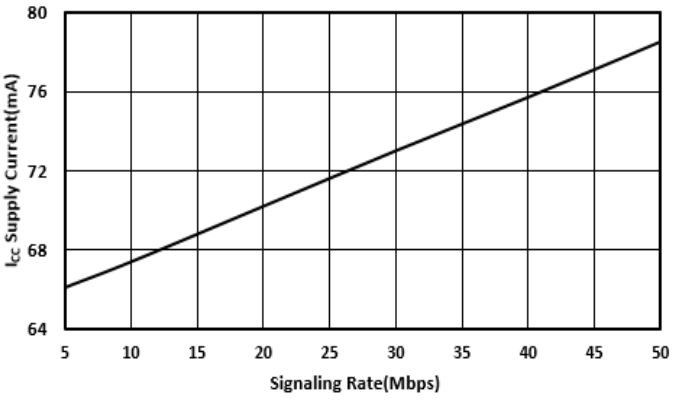
V_{CC}=5V

Figure 5 Driver Rise Time\Fall Time vs Temperature



V_{CC}=5V

Figure 6-20 Driver Propagation Delay vs. Temperature



T_A=25℃ VCC =5V R_L=54Ω

Figure 6-21 Supply Current vs. Signal Rate

7. Parameter Measurement Information

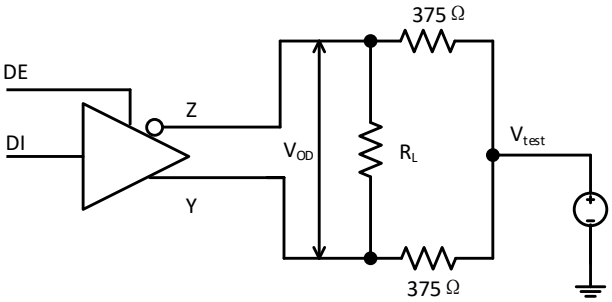


Figure 6-22 Measurement of Driver Differential Output Voltage With Common-Mode Load

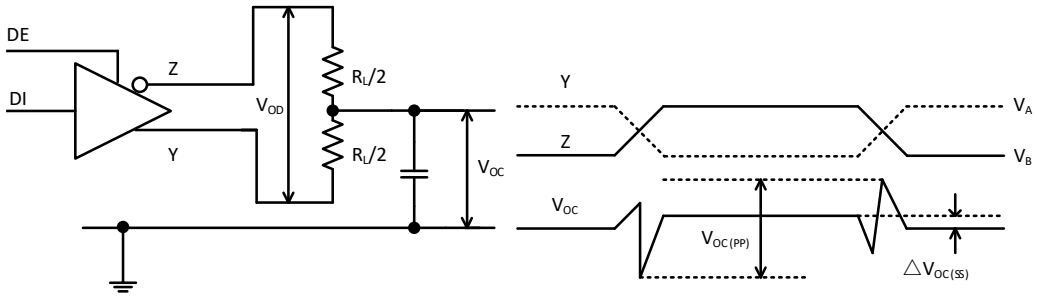


Figure 6-23 Measurement of Driver Differential and Common-Mode Output With RS-485 Load

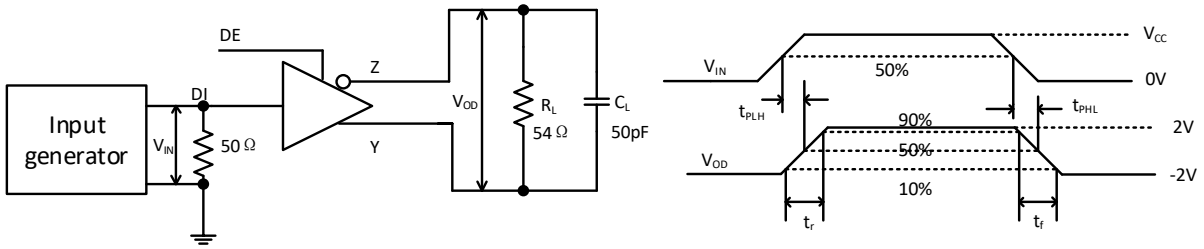


Figure 6-24 Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

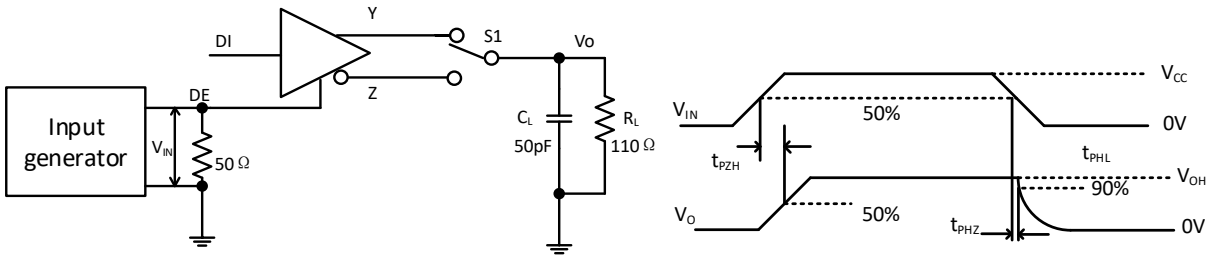


Figure 6-25 Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

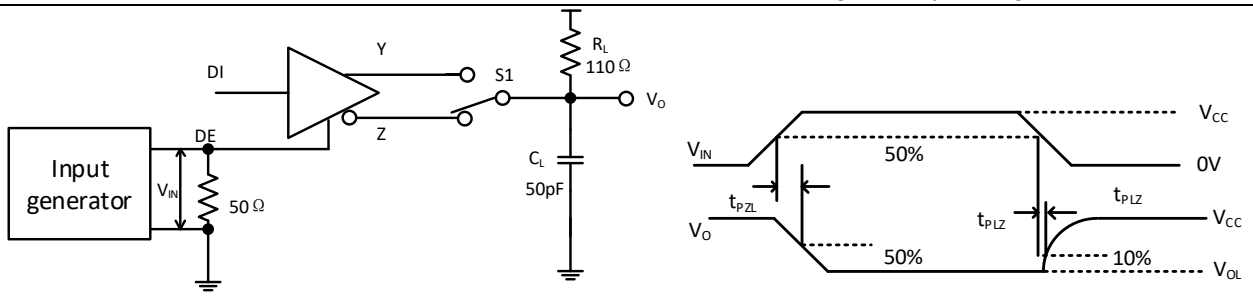


Figure 6-26 Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

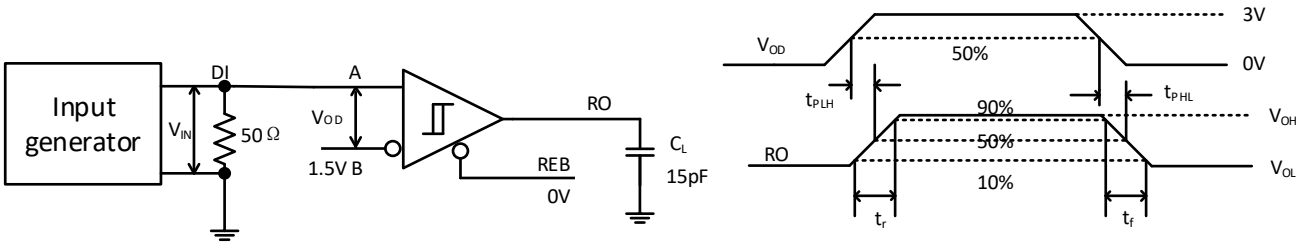


Figure 6 Measurement of Receiver Output Rise and Fall Times and Propagation Delays

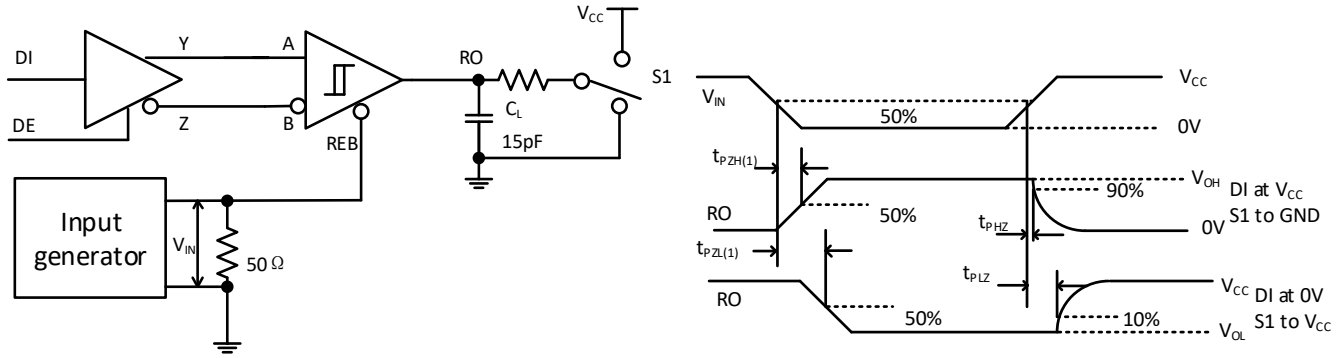


Figure 6-28 Measurement of Receiver Enable/Disable Times With Driver Enabled

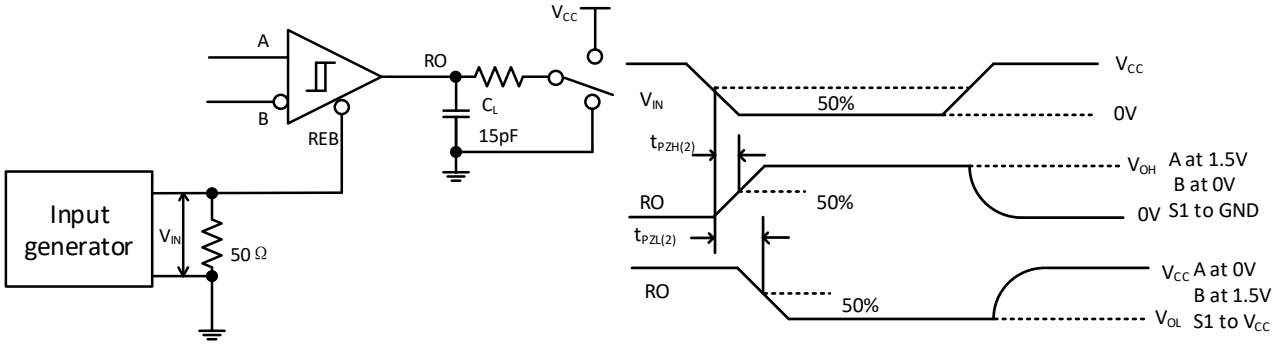


Figure 6-29 Measurement of Receiver Enable Times With Driver Disabled

8. Detailed Description

8.1. Overview

CA-IF48xx family of devices are optimized for RS-485/RS-422 applications per the EIA/TIA-485 standard. The CA-IF48xxH_serials devices are the half-duplex transceivers, and the CA-IF48xxF_ serials devices are the full-duplex transceivers. These devices contain one differential driver and one differential receiver. They feature a 1/8-unit load, allowing up to 256 transceivers on a single bus. The CA-IF4805 supports data rates up to 500kbps, the CA-IF4820 supports data rates up to 20Mbps, and the CA-IF4850 supports data rates up to 50Mbps.

The CA-IF48xx device family provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

8.2. Device Functional Modes

8.2.1 Device Function Modes for CA-IF48xxH_

The CA-IF48xxH_ driver accepts a single-ended, logic-level input (DI) and transfers it to a differential RS-485/RS-422 level output on the A and B driver outputs. Set the driver enable input (DE) low to disable the driver. A and B are high impedance when the driver is disabled. The DI pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1 CA-IF48xxH_ Driver Function Table

Input	Enable	Output		Function
DI	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

The receiver accepts a differential, RS-485/RS-422 level input on the A and B inputs and transfers it to a single-ended, logic-level output (RO). Drive the receiver enable input (REB) low to enable the receiver. Drive REB high to disable the receiver. RO is high impedance when REB is high. The CA-IF48xx devices include a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to V_{TH+} (-100mV), RO is logic high.

Table 8-2 CA-IF48xxH_ Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A – V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

8.2.2 Device Function Modes for CA-IF48xxF_

For these full-duplex devices, the driver and receiver are fully enabled, thus the differential outputs Y and Z follow the logic states at data input DI at all times. A logic high at DI causes Y to turn high and Z to turn low. When DI is low, the output states reverse: Z turns high, Y becomes low. The DI pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 8-3 CA-IF48xxF_ Driver Function Table

Input	Output		Function
DI	Y	Z	
H	H	L	Actively drive bus high
L	L	H	Actively drive bus low
OPEN	H	L	Actively drive bus high by default

When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output(RO) turns high. When V_{ID} is less than the negative input threshold, $V_{TH–}$, the receiver output(RO) turns low. The CA-IF48xx devices include a true fail-safe feature that ensures the receiver output (RO) is high when the receiver inputs are shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage V_{ID} is greater than or equal to V_{TH+} (-100mV), RO is logic high.

Table 8-4 CA-IF48xxF_ Receiver Function Table

Differential Input	Enable	Output	Function
$V_{ID} = V_A – V_B$	REB	RO	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9. Application Information

CA-IF48xx family consists of half-duplex and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For half-duplex devices, the driver and receiver enable pins allow for the configuration of different operating modes. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

9.1. Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. As seen in the following typical network application circuit, to minimize reflections, terminate the line at both ends with a termination resistor, R_T, whose value matches the characteristic impedance(Z_0) of the cable, and keep stub lengths off the main line as short as possible. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

9.2. Power Supply

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

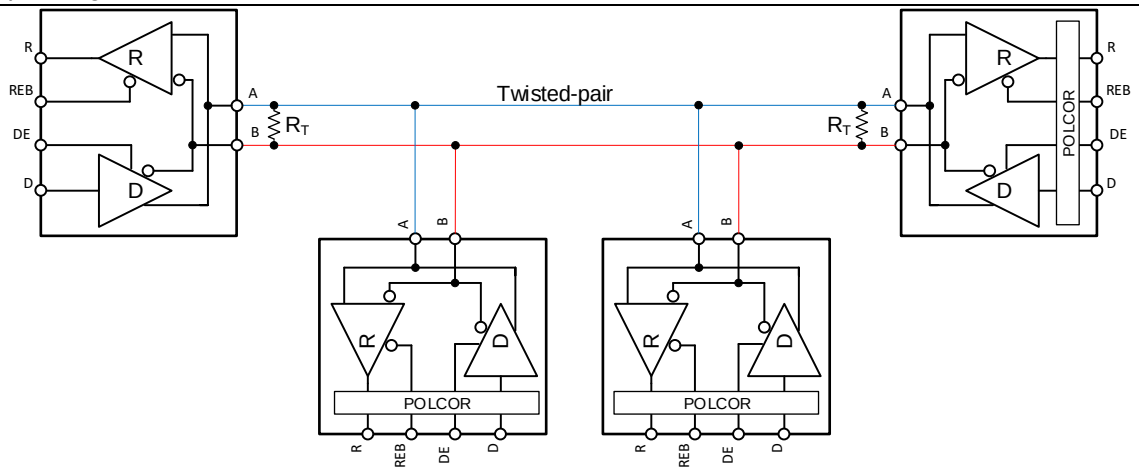


Figure 9-1 Typical RS-485 Network With Half-Duplex Transceivers

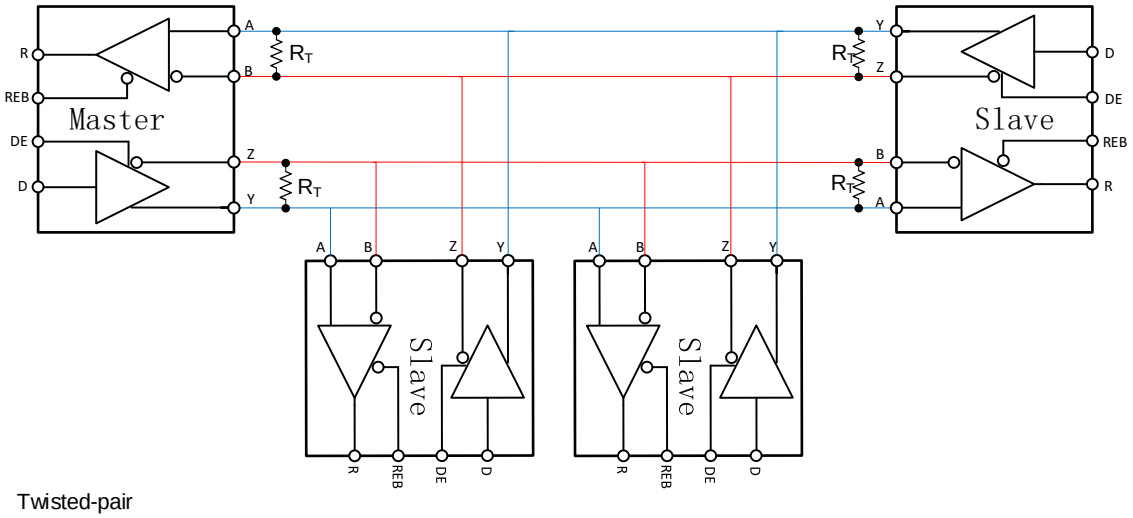
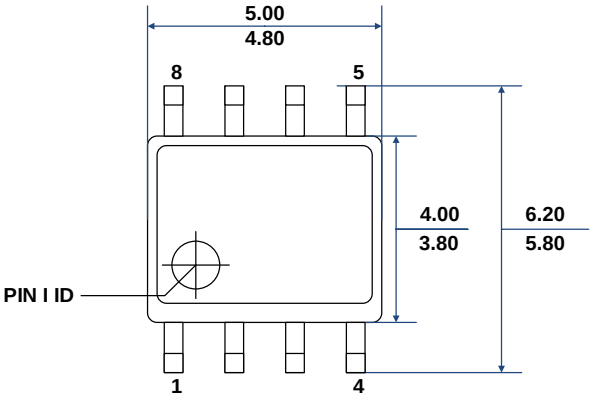


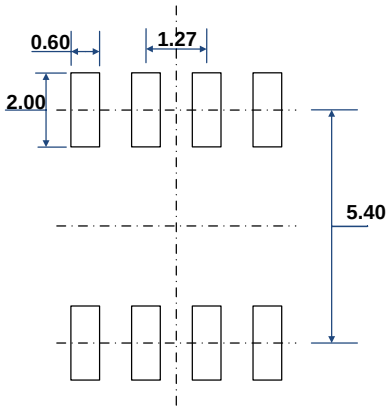
Figure 9-2 Typical RS-485 Network With Full-Duplex Transceivers

10. Package Information

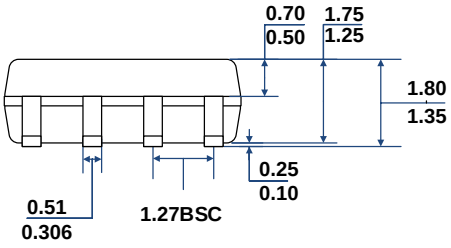
10.1. SOIC8 Package Outline



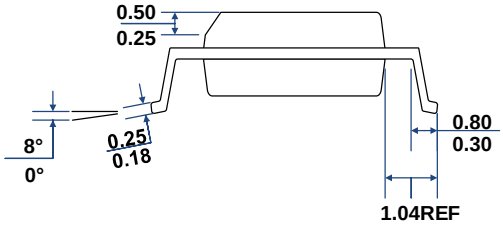
TOP VIEW



RECOMMENDED LAND PATTERN

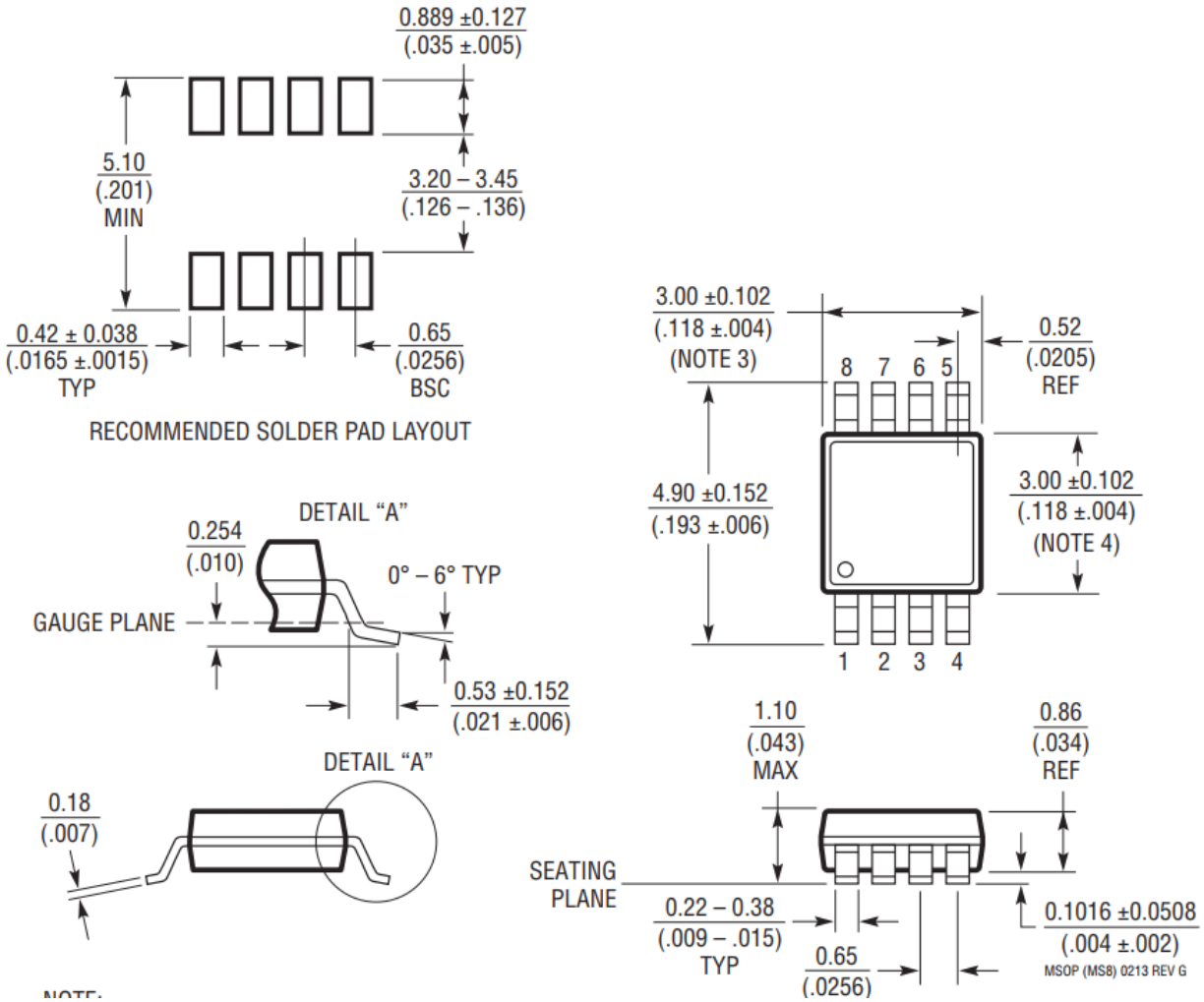


FRONT VIEW

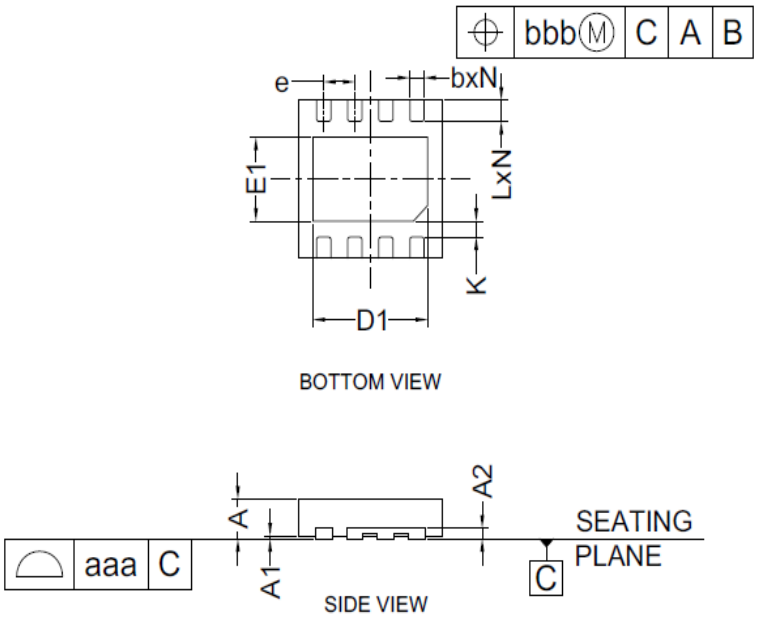


LEFT-SIDE VIEW

10.2. MSOP8 Package Outline



10.3. DFN8 Package Outline

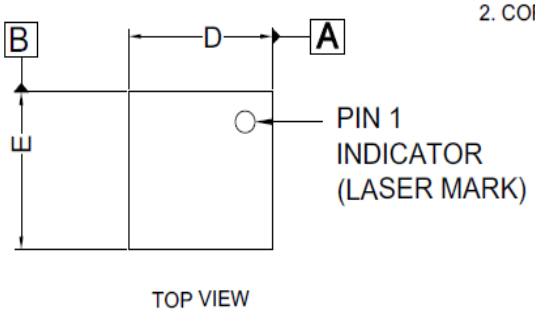


COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.30	0.35	0.40
D	2.90	3.00	3.10
D1	2.51	2.56	2.61
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
N		8	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.



11. Soldering Temperature (reflow) Profile

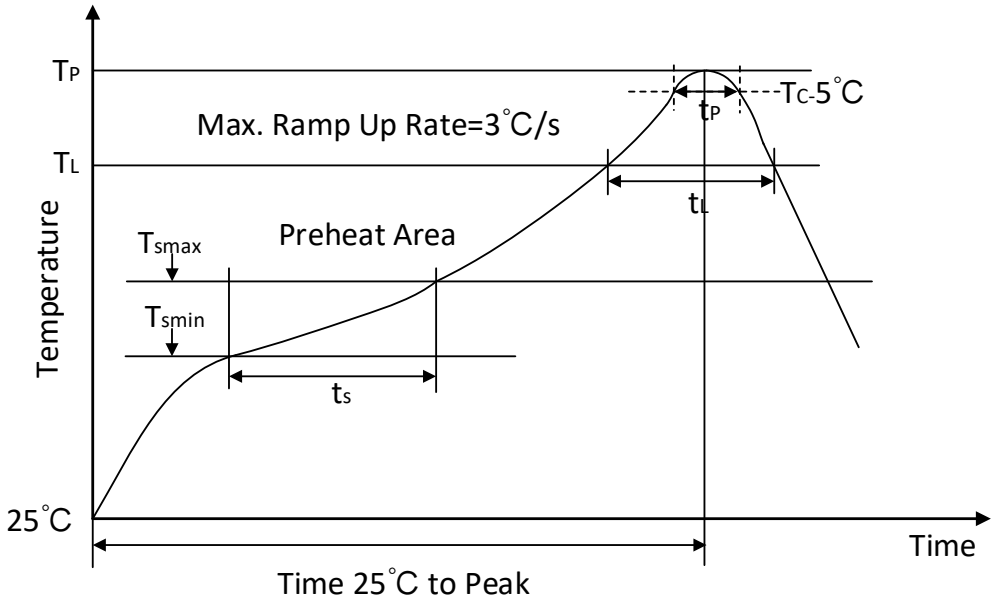


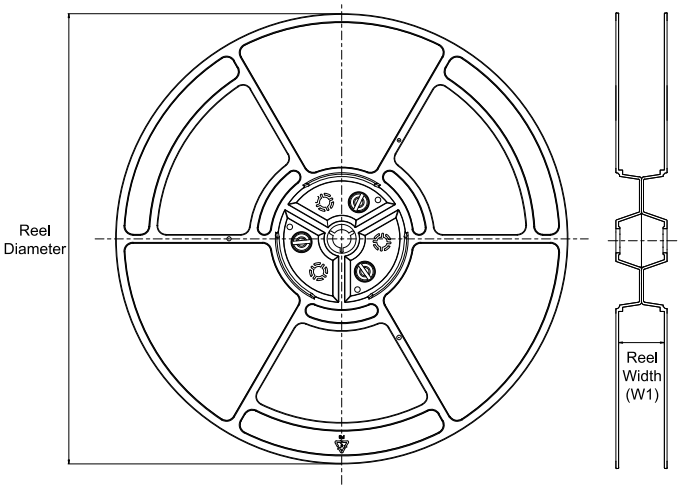
Figure 11- 1 Soldering Temperature (reflow) Profile

Table11- 1 Soldering Temperature Parameter

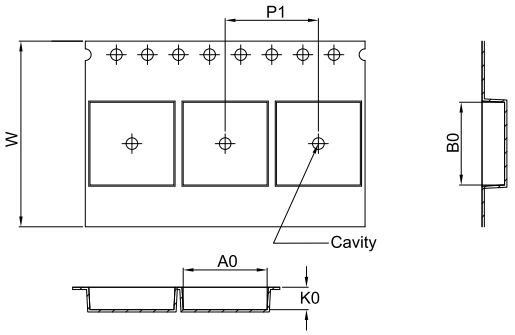
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

12. Tape and Reel Information

REEL DIMENSIONS

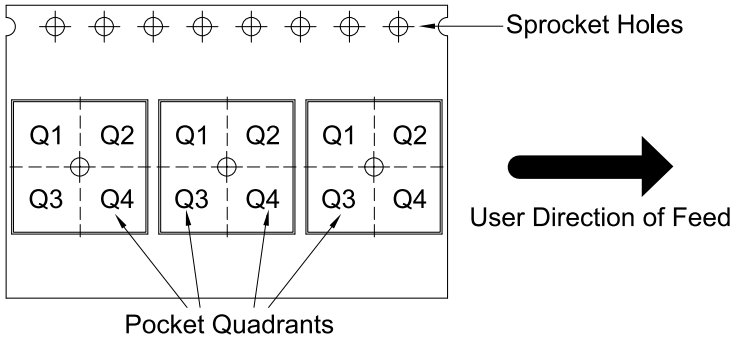


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IF4805HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4805FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4820HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4820FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4850HS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4850FS	SOIC	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CA-IF4805HM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4805FM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4820HM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4820FM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4850HM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4850FM	MSOP8	M	8	5000	330	TBD	TBD	TBD	TBD	TBD	12.0	Q1
CA-IF4805HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4805FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4820HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4820FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4850HD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CA-IF4850FD	DFN	D	8	3000	180	12.4	3.3	3.3	1.1	8.0	12.0	Q1

13. Important statement

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