CA-IS373x High-Speed Triple-Channel Digital Isolators

1. Features

- **Robust Galvanic Isolation of Digital Signals**
  - High lifetime: >40 years
  - Up to 3750 V_{RMS} isolation rating (narrow body packages) and up to 5000 V_{RMS} isolation rating (wide body packages)
  - ±150 kV/µs typical CMTI
  - Wide operating temperature range: -40°C to 125°C
  - Schmitt trigger inputs
- **Interfaces Directly with Most Micros and FPGAs**
  - Data rate: DC to 150Mbps
  - Accepts 2.5V to 5.5V supplies
  - Default output *High* (CA-IS373xH) and *Low* (CA-IS373xL) Options
- **Low Power Consumption**
  - 1.5mA per channel at 1Mbps with V_{DD} = 5.0V
  - 6.6mA per channel at 100Mbps with V_{DD} = 5.0V
- Best in class propagation delay and skew
  - 8ns typical propagation delay
  - 1ns pulse width distortion
  - 2ns propagation delay skew (chip -to-chip)
  - 5ns minimum pulse width
- **No Start-Up Initialization Required**
- **Enable Control Input with internal pull-up**
- **Package Options**
  - Narrow-body SOIC16-NB(N) package
  - Narrow-body SSOP16-NB(B)
  - Wide-body SOIC16-WB(W) package
- **Safety Regulatory Approvals**
  - VDE 0884-11 Reinforced Isolation
  - UL According to UL1577
  - IEC 62368-1, IEC 61010-1, GB 4943.1-2011 and GB 8898-2011 certifications

2. Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated SPI, RS485, CAN etc.

3. General Description

The CA-IS373x devices are high-performance triple-channel digital isolators with up to 3.75kV_{RMS} (narrow-body package) or 5kV_{RMS} (wide-body package) isolation rating and ultra-fast data rate. The CA-IS373x devices offer high electromagnetic immunity and low emissions at low power consumption, while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO2) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity.

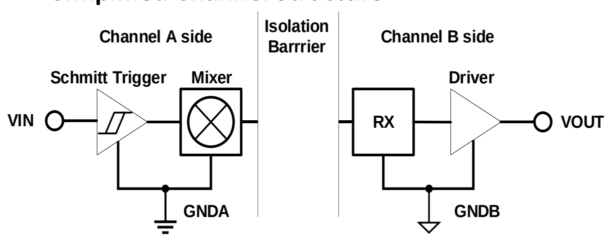
The CA-IS3730 features 3 channels transferring digital signals in one direction for applications such as isolated digital I/O. The CA-IS3731 device has 2 forward and 1 reverse-direction channels. All of the devices in the family come with enable pins which can be used to put the outputs in high impedance for multi-master driving applications to reduce power consumption. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the *Ordering Information* for suffixes associated with each option.

The CA-IS373x family devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin SOIC, narrow body package and 16-pin SOIC wide body package. The CA-IS3731 also provides 16-pin SSOP narrow body package.

Device information

Part number	Package	Package size (NOM)
CA-IS3730 CA-IS3731	SOIC16-NB (N)	9.90 mm × 3.90 mm
	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3731	SSOP16-NB(B)	4.90 mm × 3.90 mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4. Ordering Information

Tab. 4-1 Ordering Information

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3730LN	3	0	Low	3.75	Yes	SOIC16-NB
CA-IS3730LW	3	0	Low	5.0	Yes	SOIC16-WB
CA-IS3730HN	3	0	High	3.75	Yes	SOIC16-NB
CA-IS3730HW	3	0	High	5.0	Yes	SOIC16-WB
CA-IS3731LN	2	1	Low	3.75	Yes	SOIC16-NB
CA-IS3731LW	2	1	Low	5.0	Yes	SOIC16-WB
CA-IS3731HN	2	1	High	3.75	Yes	SOIC16-NB
CA-IS3731HW	2	1	High	5.0	Yes	SOIC16-WB
CA-IS3731HB	2	1	High	3.75	Yes	SSOP16-NB

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5. Revision History

Revision 0, initial version

Revision 0 to Revision A

- Updated *Description*
- Updated *Table 4-1*
  - Updated *Isolation Rating*
- Updated *Figure 6-1*
  - Revised the pin names
  - Added *EN Description*
- Updated *Insulation Specifications*
- Updated *16-Pin Wide Body SOIC Package* Outline

Revision A to Revision B

- Updated *Features* section

Revision B to Revision C

- Updated *Figure 6-1*
  - Added pin orders
- Updated the SPQ of *Tape and Reel Information*

Revision C to Revision D

- Updated *Package Information*
  - Changed Package tolerances

Revision D to Revision E

- Updated *Features* section
  - Revised CMTI spec.
- Updated *ESD Ratings*
- Updated *Table 7.8.1, Table 7.8.2, Table 7.8.3*
  - Revised CMTI spec.

Revision E to Revision F

- Updated *Electrical Characteristics*
- Updated *Table 7.8 Leakage Current*

Revision F to Revision G

- Updated *Safety-Related Certifications*
- Updated *Tape and Reel Information*
- Added *Soldering Temperature Profile*

Revision G to Revision H

- Updated *Table 7.9.1, 7.9.2, 7.9.3*
- Updated *Table 7.10.1, Table 7.10.2, Table 7.10.3*
- Changed V_{DD_AMR}, from 6V to 7V

Revision H to Revision I

- Updated Ordering Information
  - Added CA-IS3731HB part number
- Updated *Table 4.1*
- Updated *Tape and Reel Information*

6. Pin Configuration and Functions

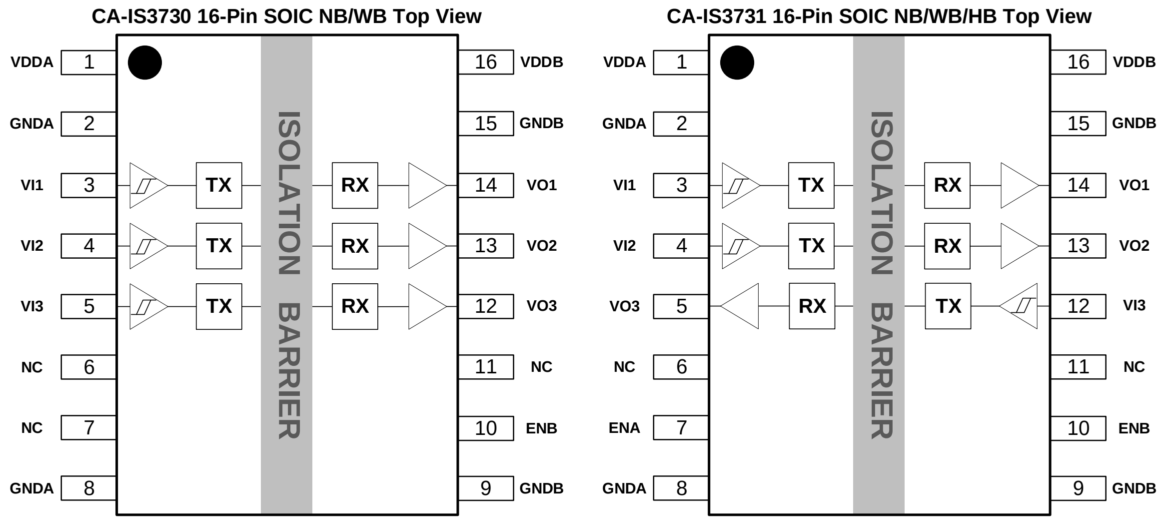


Figure. 6-1 CA-IS373x pin configuration

Tab. 6-1 CA-IS373x pin description and function

16-SOIC/16-SSOP Pin#		Name	Type	Description
CA-IS3730	CA-IS3731			
1	1	VDDA	Supply	Power supply for side A.
2, 8	2, 8	GNDA	Ground	Ground reference for side A.
3	3	VI1	Digital I/O	Digital input 1 on side A, corresponds to logic output 1 on side B.
4	4	VI2	Digital I/O	Digital input 2 on side A, corresponds to logic output 2 on side B.
5	12	VI3	Digital I/O	Digital input 3 on side A/B, corresponds to logic output 3 on side B/A.
6, 7, 11	6, 11	NC [1]	No Connect	Not internally connected.
-	7	ENA[2]	Digital I/O	Output enable A. Output pin on side A is enabled when ENA is high or floating; Output pin on side A is open and in high-impedance state when ENA is low.
9, 15	9, 15	GNDB	Ground	Ground reference for side B.
10	10	ENB[2]	Digital I/O	Output enable B. Output pin on side B is enabled when ENB is high or floating; Output pin on side B is open and in high-impedance state when ENB is low.
12	5	VO3	Digital I/O	Digital output 3 on side B/A, VO3 is the logic output for the VI3 input on side A/B.
13	13	VO2	Digital I/O	Digital output 2 on side B, VO2 is the logic output for the VI2 input on side A.
14	14	VO1	Digital I/O	Digital output 1 on side B, VO1 is the logic output for the VI1 input on side A.
16	16	VDDB	Supply	Power supply for side B.

Note:

1. No Connect. These pins are not internally connected. They can be left floating, tied to VDD_ or tied to GND.
2. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DDA}, V_{DDB}	Power supply voltage [2]	-0.5	6.0	V
V_{IN}	Voltage at VI_X, VO_X, EN_X	-0.5	V_{DD}+0.5 [3]	V
I_O	Output current	-20	20	mA
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not be exceed 7 V.

7.2. ESD Ratings

		Numerical value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±6000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. JEDEC document JEP157, 250V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

	PARAMETER		MIN	TYPE	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage on side A, B		2.375	3.30	5.50	V
$V_{DD(UVLO+)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD(UVLO-)}$	V_{DD} Undervoltage-Lockout Threshold When Supply Voltage is Falling		1.88	2.10	2.325	V
$V_{HYS(UVLO)}$	V_{DD} Undervoltage-Lockout Threshold Hysteresis		70	140	250	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			1	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

Notes:

1. V_{DDO} = Output-side supply V_{DD}.

7.4. Thermal Information

Thermal Metric		CA-IS373x			Unit
		SOIC16-NB(N)	SOIC16-WB(W)	SSOP16-NB(B)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.2	83.4	110	°C/W

7.5. Power Rating

Parameters		Test conditions	MIN	TYPE	MAX	Unit
CA-IS3730						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			252	mW
P_{DA}	Maximum Power Dissipation on Side-A				27	mW
P_{DB}	Maximum Power Dissipation on Side-B				225	mW
CA-IS3731						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave.			252	mW
P_{DA}	Maximum Power Dissipation on Side-A				92	mW
P_{DB}	Maximum Power Dissipation on Side-B				160	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value		Unit
			W	N, B	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	19	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	N/A	
VDE[1]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	566	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	400	V_{RMS}
		DC voltage	849	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	5300	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	6250	5000	V_{PK}
q_{pd}	Apparent charge	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL[2]					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	3750	V_{RMS}

Notes:
1. CA-IS3730, CA-IS3731 are certified under DIN V VDE V 0884-11:2017-01.
2. CA-IS3730, CA-IS3731 are certified under UL1577.

7.7. Safety-Related Certifications

VDE	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017
Maximum transient isolation voltage: 7070V_{pk} (SOIC16-W), 5300V_{pk} (SOIC16-N)	Single protection, SOP16-N: 3750 V_{RMS}; SOP16-W: 5000 V_{RMS}	SOP16-N: Basic insulation, 400 V_{RMS} maximum working voltage; SOP16-W: Reinforced insulation, 600 V_{RMS} maximum working voltage（Altitude ≤ 5000 m）	5000 V_{RMS}(SOP16-W) insulation and 3750 V_{RMS}(SOP16-N) insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017, working voltage is up to 600 V_{RMS}(SOP16-W) and 400 V_{RMS}(SOP16-N)
Certificate number: 40052786	Certificate number：E511334	Certificate number SOP16-N: CQC20001251750 SOP16-W: CQC20001251466	CB Certificate number: JPTUV-111116; DE 2-027880 AK Certificate number: AK 50474784 0001; AK 50474786 0001

7.8. Electrical Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See *Figure 8-2*	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See *Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See *Figure 8-4*	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

Note:

1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See *Figure 8-2*	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See *Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See *Figure 8-4*	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

Note:

1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

V_{DDA} = V_{DDB} = 2.5 V ± 10%, T_A = -40 to 125°C

Parameters		Test conditions	MIN	TYPE	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; See *Figure 8-2*	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; See *Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold		1.4	1.7	1.9	V
$V_{IT-(IN)}$	Falling input switching threshold		1.0	1.3	1.5	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at INx or ENx			20	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at INx	-20			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; See *Figure 8-4*	100	150		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

Note:

1. V_{DDI} = Input-side supply V_{DD}, V_{DDO} = Output-side supply V_{DD}.
2. The nominal output impedance of each isolator driver is 50 Ω ± 40%.
3. Measured from pin to Ground.

7.9. Supply Current Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730							
Supply Current – Outputs disabled	ENB = 0 V; V_{IN} = 0V (CA-IS3730L); V_{IN} = V_{DDA} (CA-IS3730H)		I_{DDA}		1.2	3.0	mA
			I_{DDB}		1.9	4.2	
	ENB = 0 V; V_{IN} = V_{DDA} (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		5.0	9.0	
			I_{DDB}		1.9	4.2	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730L); V_{IN} = V_{DDA} (CA-IS3730H)		I_{DDA}		1.2	3.0	
			I_{DDB}		2.1	4.4	
	ENB = V_{DDB}; V_{IN} = V_{DDA} (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		5.0	9.0	
			I_{DDB}		1.9	4.2	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		2.4	5.4	
		10Mbps (5MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		3.9	8.8	
		100Mbps (50MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		18.1	41	
CA-IS3731							
Supply Current – Outputs disabled	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI}[1] (CA-IS3731H)		I_{DDA}		1.6	3.6	mA
			I_{DDB}		2.0	4.2	
	ENA = ENB = 0 V; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.1	7.5	
			I_{DDB}		3.2	6.0	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI} (CA-IS3731H)		I_{DDA}		1.6	3.6	
			I_{DDB}		2.1	4.5	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.2	7.5	
			I_{DDB}		3.4	6.3	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.4	5.1	
			I_{DDB}		2.5	5.6	
		10Mbps (5MHz)	I_{DDA}		2.9	6.0	
			I_{DDB}		3.4	7.5	
		100Mbps (50MHz)	I_{DDA}		7.6	16.8	
			I_{DDB}		12.9	29.2	

Note:
1. V_{DDI} = Input-side V_{DD}.

$V_{DDA} = V_{DDB} = 3.3\ V \pm 10\%$, T_A = -40 to 125°C

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730							
Supply Current – Outputs disabled	ENB = 0 V; V_{IN} = 0V (CA-IS3730L); $V_{IN} = V_{DDA}$ (CA-IS3730H)		I_{DDA}		1.1	3.0	mA
			I_{DDB}		1.9	4.2	
	ENB = 0 V; $V_{IN} = V_{DDA}$ (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		5.0	9.0	
			I_{DDB}		1.9	4.2	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730L); $V_{IN} = V_{DDA}$ (CA-IS3730H)		I_{DDA}		1.1	3.0	
			I_{DDB}		2.0	4.5	
	ENB = V_{DDB}; $V_{IN} = V_{DDA}$ (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		5.0	9.0	
			I_{DDB}		2.0	4.5	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		2.4	5.4	
		10Mbps (5MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		3.5	7.5	
		100Mbps (50MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		13.6	30.1	
CA-IS3731							
Supply Current – Outputs disable	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$[1] (CA-IS3731H)		I_{DDA}		1.5	3.6	mA
			I_{DDB}		1.9	4.2	
	ENA = ENB = 0 V; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.1	7.5	
			I_{DDB}		3.2	6.0	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$ (CA-IS3731H)		I_{DDA}		1.6	3.7	
			I_{DDB}		2.0	4.5	
	ENA = ENB = V_{DDI}; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.1	7.5	
			I_{DDB}		3.4	6.3	
Supply Current – AC Signal	ENA=ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.4	5.1	
			I_{DDB}		2.5	5.6	
		10Mbps (5MHz)	I_{DDA}		2.7	6.0	
			I_{DDB}		3.2	7.2	
		100Mbps (50MHz)	I_{DDA}		6.1	14.5	
			I_{DDB}		9.9	21.5	

Note:
1. V_{DDI} = Input-side V_{DD}.

$V_{DDA} = V_{DDB} = 2.5\ V \pm 10\%$, $T_A = -40$ to 125°C

Parameters	Test conditions		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730							
Supply Current – Outputs disabled	ENB = 0 V; V_{IN} = 0V (CA-IS3730L); $V_{IN} = V_{DDA}$ (CA-IS3730H)		I_{DDA}		1.1	3	mA
			I_{DDB}		1.9	4.2	
	ENB = 0 V; $V_{IN} = V_{DDA}$ (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		4.9	9.0	
			I_{DDB}		1.9	4.2	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730L); $V_{IN} = V_{DDA}$ (CA-IS3730H)		I_{DDA}		1.1	3.0	
			I_{DDB}		2.0	4.5	
	ENB = V_{DDB}; $V_{IN} = V_{DDA}$ (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		4.9	9.0	
			I_{DDB}		2.0	4.5	
Supply Current – AC Signal	ENB = VDDB; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		2.4	5.4	
		10Mbps (5MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		3.2	7.2	
		100Mbps (50MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		10.6	24.0	
CA-IS3731							
Supply Current – Disable	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$[1] (CA-IS3731H)		I_{DDA}		1.5	3.6	mA
			I_{DDB}		1.9	4.2	
	ENA = ENB = 0 V; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.1	7.5	
			I_{DDB}		3.2	6.0	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$ (CA-IS3731H)		I_{DDA}		1.6	3.6	
			I_{DDB}		2.0	4.5	
	ENA = ENB = V_{DDI}; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		4.1	7.5	
			I_{DDB}		3.3	6.3	
Supply Current – AC Signal	ENA=ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; CL = 15 pF for Each Channel.	1Mbps (500kHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		2.4	5.4	
		10Mbps (5MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		3.2	7.2	
		100Mbps (50MHz)	I_{DDA}		2.2	4.5	
			I_{DDB}		10.6	24.0	

Note:

1. V_{DDI} = Input-side supply V_{DD}.

7.10. Timing Characteristics

V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL}\rvert$				0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time[2]				2.0	4.5	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		8	13	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				8	17	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL			10	20	ns
		CA-IS373xH			15	30	ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL			10	25	ns
		CA-IS373xH			15	30	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		0.1	0.3	µs
t_{SU}	Start-up Time				15	40	µs

Notes:
1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL}\rvert$				0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-Part Output Skew Time[2]				2.0	4.5	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		12	19	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				14	26	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL			10	20	ns
		CA-IS373xH			8	15	ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL			8	20	ns
		CA-IS373xH			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		0.1	0.3	µs
t_{SU}	Start-up Time				15	40	µs

Notes:
1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

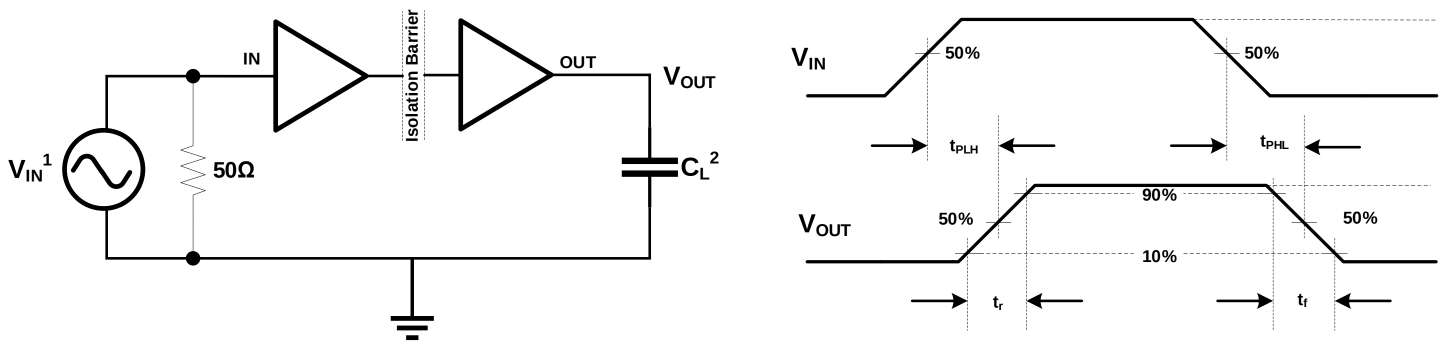
$V_{DDA} = V_{DDB} = 2.5\ V \pm 10\%$, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	12.0	15.0	ns
PWD	Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$				0.2	4.5	ns
$t_{sk(o)}$	Channel-to-Channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to Part Output Skew Time[2]				2.0	5.0	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		16	26	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				16	26	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL			10	20	ns
		CA-IS373xH			10	20	ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL			10	18	ns
		CA-IS373xH			10	20	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		0.1	0.3	µs
t_{SU}	Start-up Time				15	40	µs

Notes:

1. tsk(o) is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. tsk(pp) is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

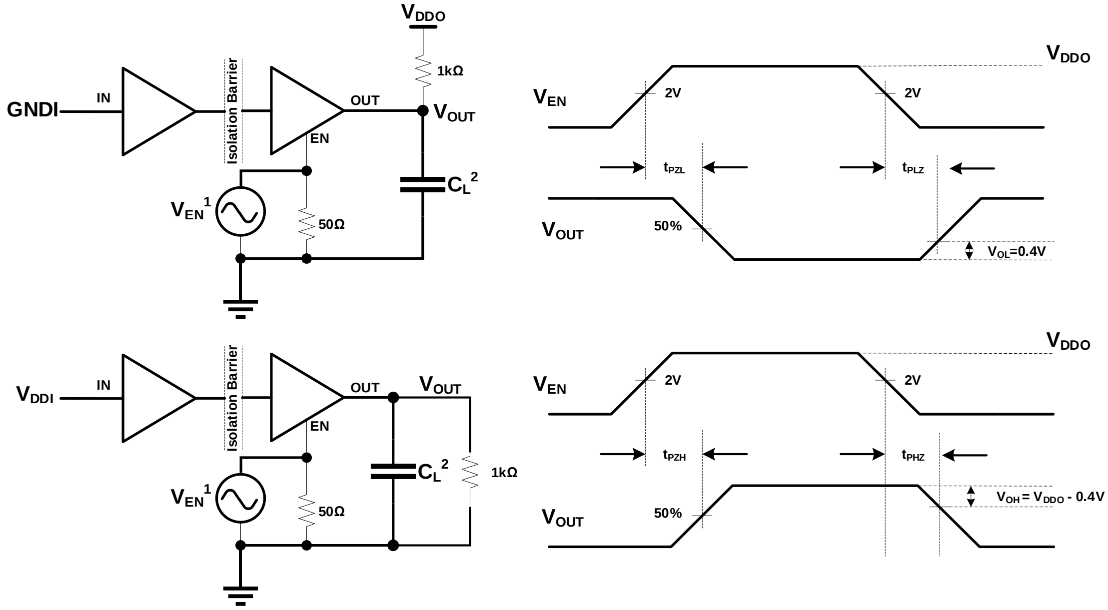
8. Parameter Measurement Information



Note:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency ≤100kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

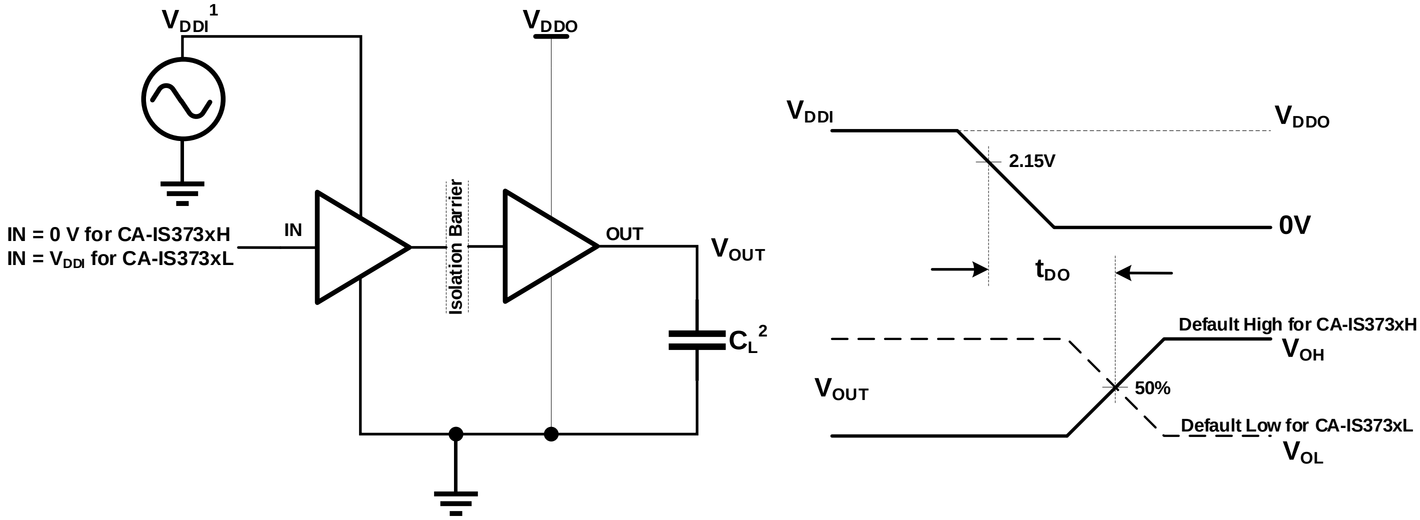
Figure. 8-1 Switching Characteristics Test Circuit and Voltage Waveforms



Note:

1. A square wave generator provide V_{IN} input signal with characteristics: frequency ≤10kHz, 50% duty cycle, t_r≤3ns, t_f≤3ns, Z_{out} = 50Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

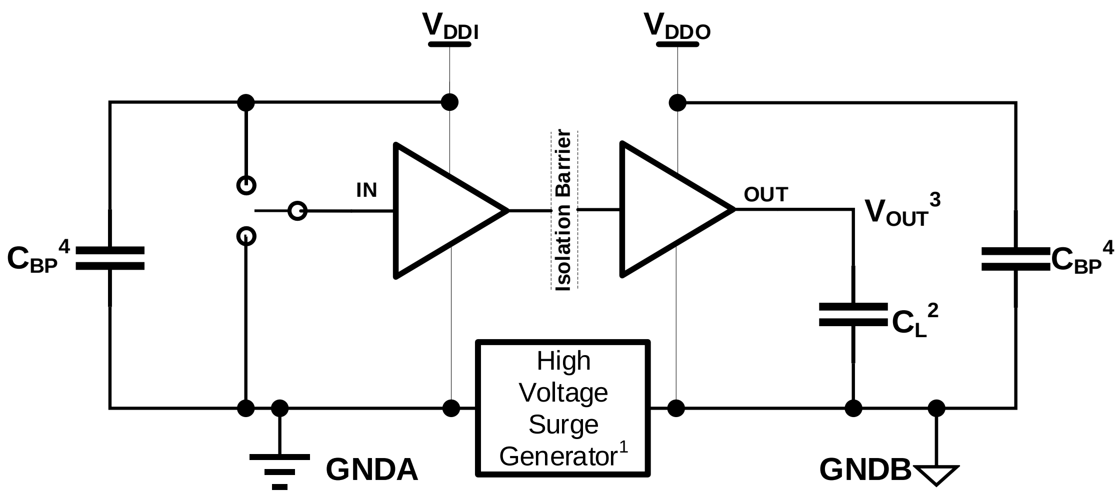
Figure. 8-2 Enable/Disable Propagation Delay Time Test Circuit and Waveform



NOTE:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.375V, and less than 5.5V.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure. 8-3 Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude, rise time <10ns and fall time <10ns, to reach common-mode transient noise with > 150kV/µs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} (0.1 ~ 1uF) is bypass capacitance.

Figure. 8-4 Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS373x are a family of three-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS373x family of devices build a robust data transmission path between different power domains, without any special start-up initialization requirements. If the ENx pin is low then the output goes to high impedance. These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching.

9.2. Functional Block Diagram

The conceptual block diagram of a digital capacitive isolator, Figure 9-1, shows a functional block diagram of a typical channel; Figure 9-2 shows the operating waveform of a typical channel. Each channel of the CA-IS374x is unidirectional, only passes data in one direction, as indicated in the functional diagram. Each device of this family features three unidirectional channels that operate independently with guaranteed data rates from DC up to 150Mbps

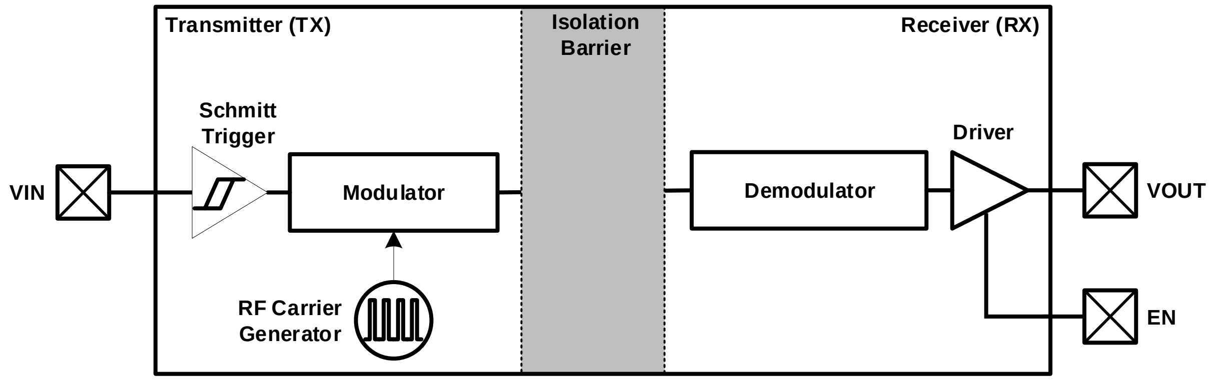


Figure. 9-1 Functional Block Diagram of a Single Channel

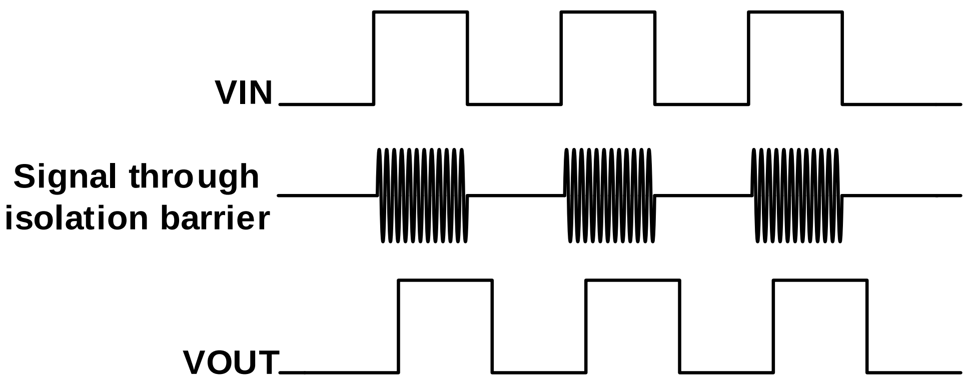


Figure. 9-2 Conceptual Operation Waveforms of a Single Channel

9.3. Device Operation Modes

Table 9-1 lists the operation modes for the CA-IS373x devices.

Tab. 9-1 Operation Mode Table

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx)[2]	ENABLE (ENx)[3]	OUTPUT (VOx)	OPERATION
PU	PU	H	H or open	H	Normal operation mode: A channel output follows the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default output mode: When input VIx is open, the corresponding channel output goes to its default logic state. Default is *High* for CA-IS373xH and Low for CA-IS373xL.
X	PU	X	L	Z	High impedance mode: A low level of Enable pin causes the output to be high impedance.
PD	PU	X	H or open	Default	Default output mode: When VDDI is unpowered, a channel output assumes the logic state based on its default option. Default is *High* for CA-IS373xH and Low for CA-IS373xL.
X	PD	X	X	Undetermined	If the output side V_{DDO} is unpowered, a channel output is undetermined.[4]

Note:

1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (V_{DD} ≥2.375 V); PD = Powered down (V_{DD} ≤2.25 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. It is recommended to connect the enable inputs to external logic high or low level when the CA-IS373x operates in noisy environments.
4. The outputs are in undetermined state when 2.25V < V_{DDI}, V_{DDO} < 2.375 V.

Table 9-2 is the truth table with Enable input for the CA-IS373x devices.

Tab. 9-2 Enable Control

PART NUMBER	ENA[1,2]	ENB[1,2]	STATUS
CA-IS3730	—	H	B-side outputs VO1, VO2, VO3 are enabled and each output follows the logic state of its input.
	—	L	B-side outputs VO1, VO2, VO3 are disabled, and go to high impedance state.
CA-IS3731	H	X	A-side output VO3 is enabled and follows the logic state of its input.
	L	X	A-side output VO3 is disabled and goes to high impedance state.
	X	H	B-side outputs VO1, VO2 are enabled and each output follows the logic state of its input.
	X	L	B-side outputs VO1, VO2 are disabled and go to high impedance state.

NOTE:

1. Enable inputs ENA and ENB can be used to put the respective outputs in high impedance for multi master driving applications, external clock synchronization etc. With internal pull-up resistors, these pins can be connected to logic high or left floating to enable the outputs. If ENA, ENB are unused, it is recommended to connect these pins to a logic level, especially in the noisy environment.
2. X = Irrelevant; H = High level; L = Low level.

10. Application and Implementation

Isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults and eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The CA-IS373x devices are the high-performance, triple-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS373x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF to 1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10-1 shows typical operating circuit of the CA-IS3731; Figure 10-2 is the typical applications for CA-IS37xx series products.

The CA-IS373x family devices do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance from the design. For digital circuit boards operating below 150 Mbps, we recommend to use the standard FR-4 PCB material and a minimum of four layers is required to accomplish a low EMI PCB design. Layer order from top-to-bottom is: high-speed signal layer, ground plane, power plane, and low-frequency signal layer. Also, keep the input/output traces as short as possible, avoid using vias to make low-inductance paths for the signals. Keep the area underneath the digital isolator ICs free from ground and signal planes.

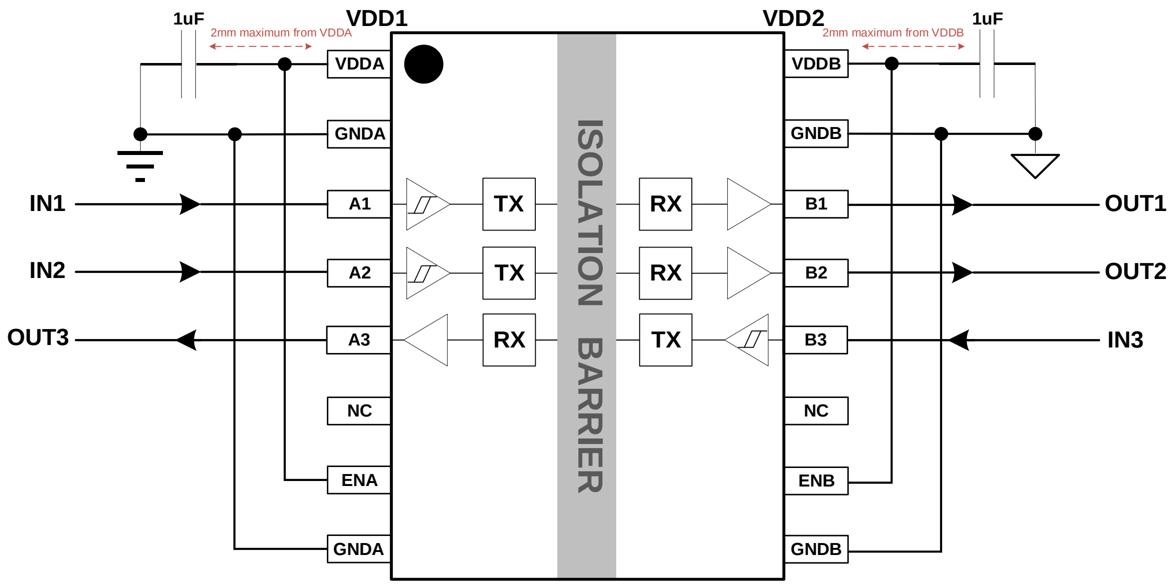


Figure. 10-1 Typical Application Circuit of CA-IS3731

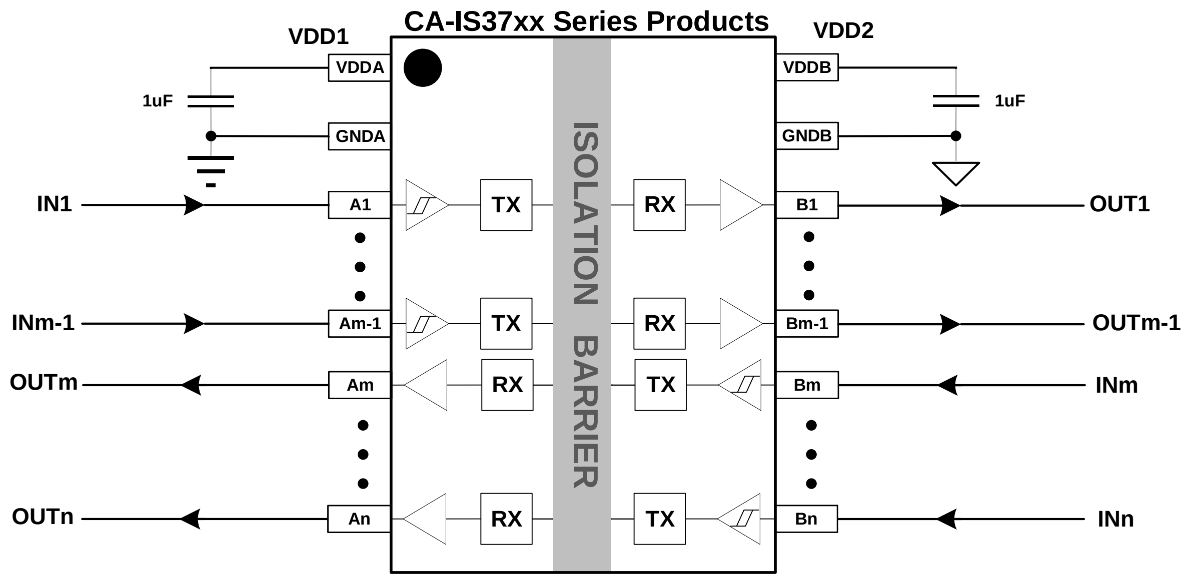
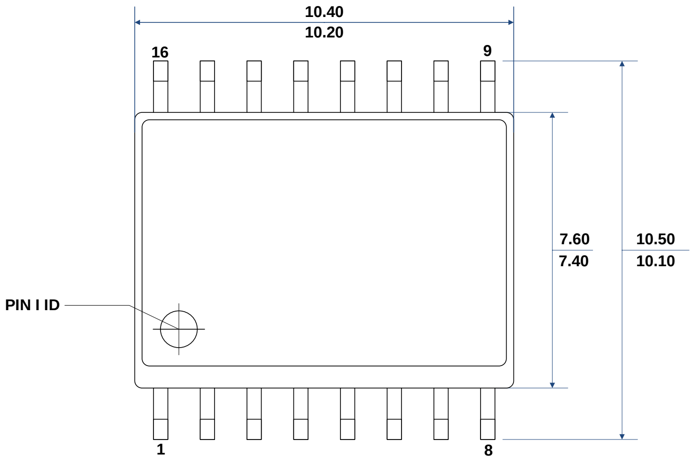


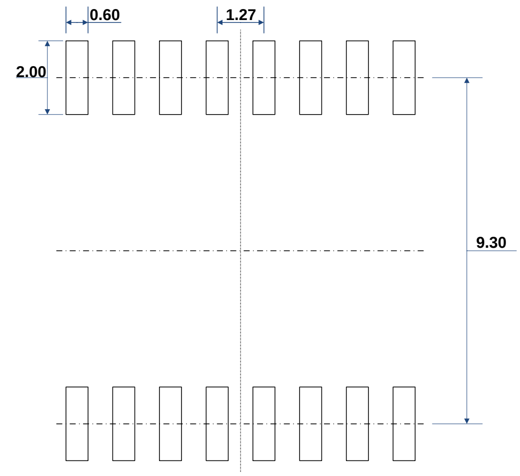
Figure. 10-2 Typical Applications for the CA-IS37xx Series Digital Isolators

11. Package Information

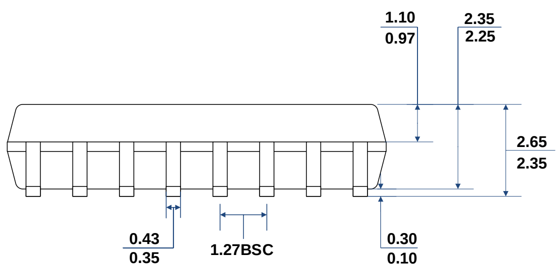
11.1. 16-Pin Wide Body SOIC Package Outline



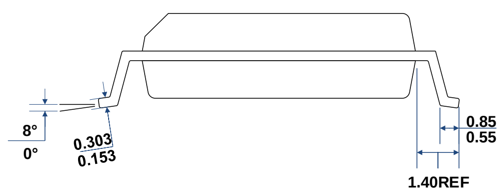
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

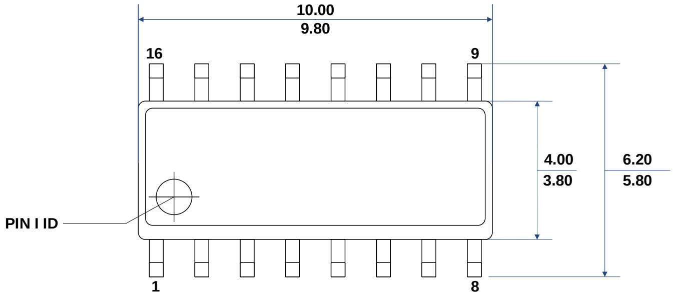


LEFT-SIDE VIEW

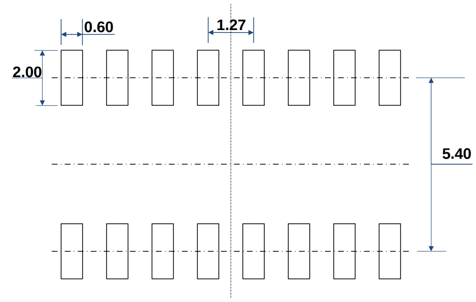
Note:

1. All dimensions are in millimeters, angles are in degrees.

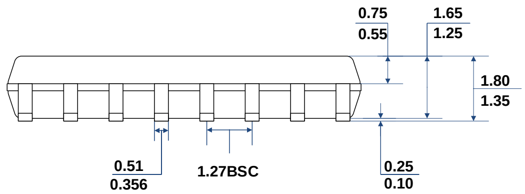
11.2. 16-Pin Narrow Body SOIC Package Outline



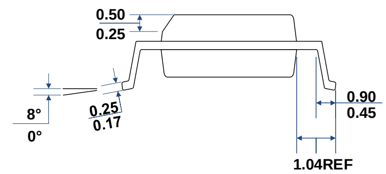
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW

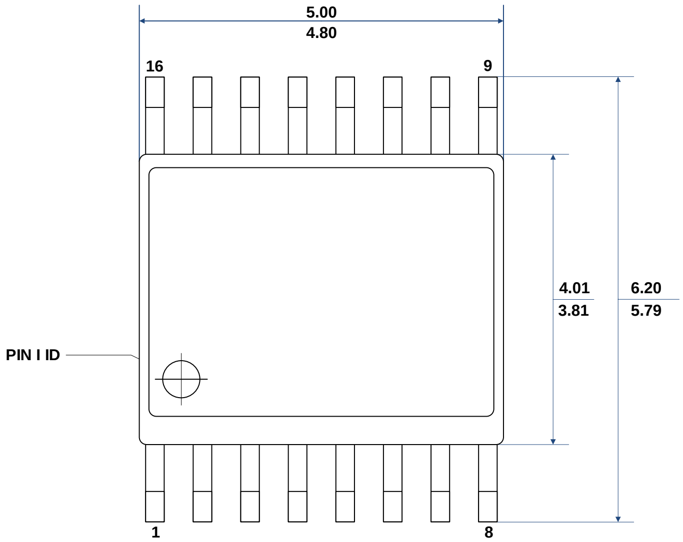


LEFT-SIDE VIEW

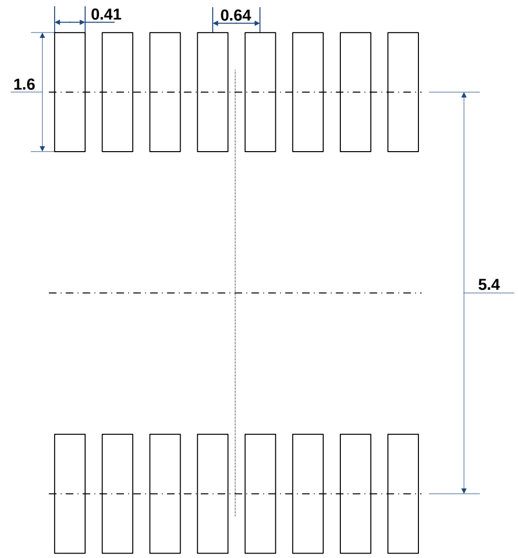
Note:

1. All dimensions are in millimeters, angles are in degrees.

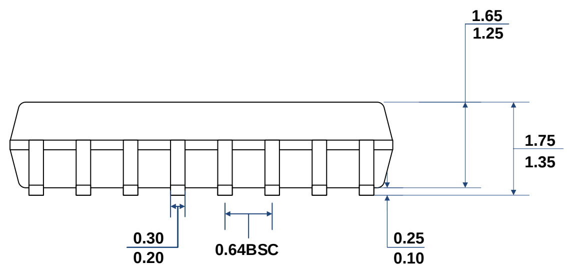
11.3. 16-Pin Narrow Body SSOP Package Outline



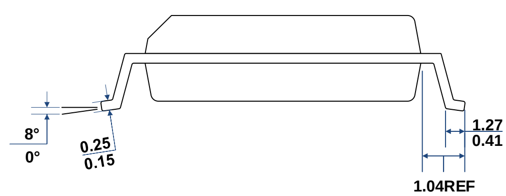
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

12. Soldering Temperature (reflow) Profile

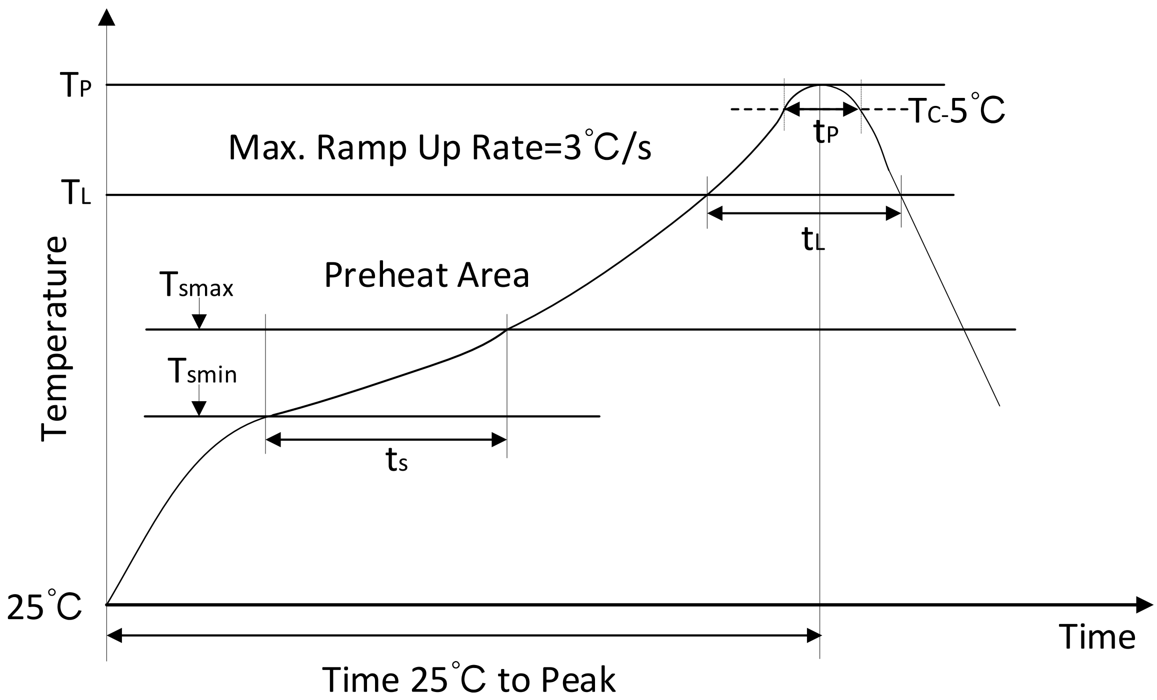


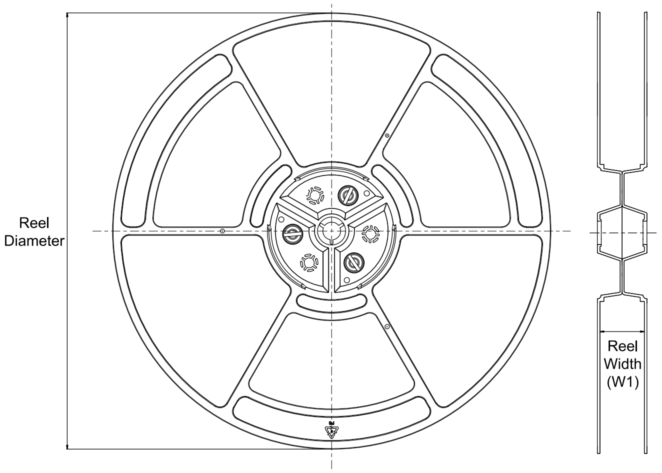
Figure. 12-1 Soldering Temperature (reflow) Profile

Tab. 12-1 Soldering Temperature Parameter

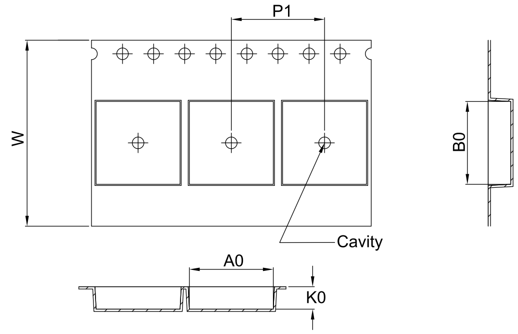
Profile Feature	**Pb-Free Assembly**
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

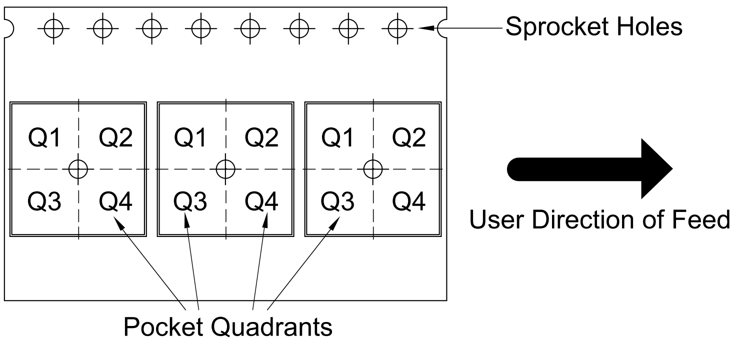


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3730LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3730LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3730HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3730HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3731LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3731LW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3731HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3731HW	SOIC	W	16	1000	330	16.4	10.9	10.7	3.2	12.0	16.0	Q1
CA-IS3731HB	SSOP	B	16	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1

14. Important statement

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