

CA-IS376x High-Speed Six-Channel Digital Isolators

1 Key Features

- Signal Rate: DC to 150Mbps
- Wide Operating Supply Voltage: 2.5V to 5.5V
- Wide Operating Temperature Range: -55°C to 125°C
- No Start-Up Initialization Required
- Default Output High and Low Options
- High Electromagnetic Immunity
- High CMTI: $\pm 100\text{kV}/\mu\text{s}$ (Typical)
- Low Power Consumption (Typical):
 - 1.5mA per Channel at 1Mbps with 5.0V Supply
 - 6.6mA per Channel at 100Mbps with 5.0V Supply
- Precise Timing (Typical)
 - 8ns Propagation Delay
 - 1ns Pulse Width Distortion
 - 2ns Propagation Delay Skew
 - 5ns Minimum Pulse Width
- Isolation Rating up to 5.0kVrms
- Isolation Barrier Life: >40 Years
- Tri-state Outputs with ENABLE
- Schmitt Trigger Inputs
- RoHS-Compliant Packages
 - SOIC16 Narrow Body
 - SOIC16 Wide Body

2 Applications

- Industrial Automation Systems
- Motor Control
- Medical Electronics
- Isolated Switch Mode Supplies
- Solar Inverters
- Isolated ADC, DAC

3 Description

The CA-IS376x devices are high-performance six-channel digital isolators with precise timing characteristics and low power consumption. The CA-IS376x devices provide high electromagnetic immunity and low emissions, while isolating CMOS digital I/Os. All device versions have Schmitt trigger input for high noise immunity. Each isolation channel consists of a transmitter and a receiver separated by silicon dioxide (SiO_2) insulation barrier. The CA-IS3760 device has

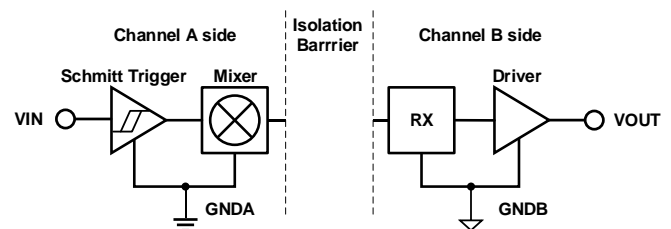
all six channels in the same direction, the CA-IS3761 device has five forward and one reverse-direction channels, the CA-IS3762 device has four forward and two reverse-direction channels, and the CA-IS3763 device has three forward and three reverse-direction channels. All devices have fail-safe mode option. If the input power or signal is lost, default output is low for devices with suffix L and high for devices with suffix H.

CA-IS376x devices has high insulation capability to handle noise and surge on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. High CMTI ability promises the correct transmission of digital signal. The CA-IS376x devices are available in 16-pin narrow body SOIC and 16-pin wide body SOIC packages. All products have 3.75kVrms isolation rating, and products in wide-body packages support insulation withstanding up to 5kVrms.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
CA-IS3760, CA-IS3761, CA-IS3762, CA-IS3763	SOIC16-NB (N)	9.90 mm × 3.90 mm
	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



Channel A side and B side are separated by isolation capacitors. GND A and GND B are the isolated ground for signals and supplies of A side and B side respectively.

4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3760LN	6	0	Low	3.75	No	SOIC16-NB
CA-IS3760LW	6	0	Low	5.0	No	SOIC16-WB
CA-IS3760HN	6	0	High	3.75	No	SOIC16-NB
CA-IS3760HW	6	0	High	5.0	No	SOIC16-WB
CA-IS3761LN	5	1	Low	3.75	No	SOIC16-NB
CA-IS3761LW	5	1	Low	5.0	No	SOIC16-WB
CA-IS3761HN	5	1	High	3.75	No	SOIC16-NB
CA-IS3761HW	5	1	High	5.0	No	SOIC16-WB
CA-IS3762LN	4	2	Low	3.75	No	SOIC16-NB
CA-IS3762LW	4	2	Low	5.0	No	SOIC16-WB
CA-IS3762HN	4	2	High	3.75	No	SOIC16-NB
CA-IS3762HW	4	2	High	5.0	No	SOIC16-WB
CA-IS3763LN	3	3	Low	3.75	No	SOIC16-NB
CA-IS3763LW	3	3	Low	5.0	No	SOIC16-WB
CA-IS3763HN	3	3	High	3.75	No	SOIC16-NB
CA-IS3763HW	3	3	High	5.0	No	SOIC16-WB

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5 Revision History

Revision 0: Initial version.

Revision 0 to Revision A

- Updated 3 Description
- Updated Table 4-1
 - Changes to Isolation Rating
- Updated Figure 6-1
 - Changes to Pin Names
- Updated Table 6-1
 - Changes to Pin Names
 - Added EN Description
- Updated 7.6 Insulation Specifications
- Updated 11.1 16-Pin Wide Body SOIC Package Outline

Revision A to Revision B

- Updated Key Features

Revision B to Revision C

- Updated Figure 6-1
 - Add the pin order
- Updated the SPQ of the tape and reel information

Revision C to Revision D

- Updated Package
 - Changes to Package tolerance information

Revision D to Revision E

- Updated 1. Key Features
 - Updated CMTI
- Updated 7.2 ESD Ratings
- Updated Table 7.8.1, 7.8.2, 7.8.3
 - Updated CMTI

Revision E to Revision F

- Updated 7.7 Electrical Characteristics
- Updated Table 7.8 Leakage Current

6 PIN Descriptions and Functions

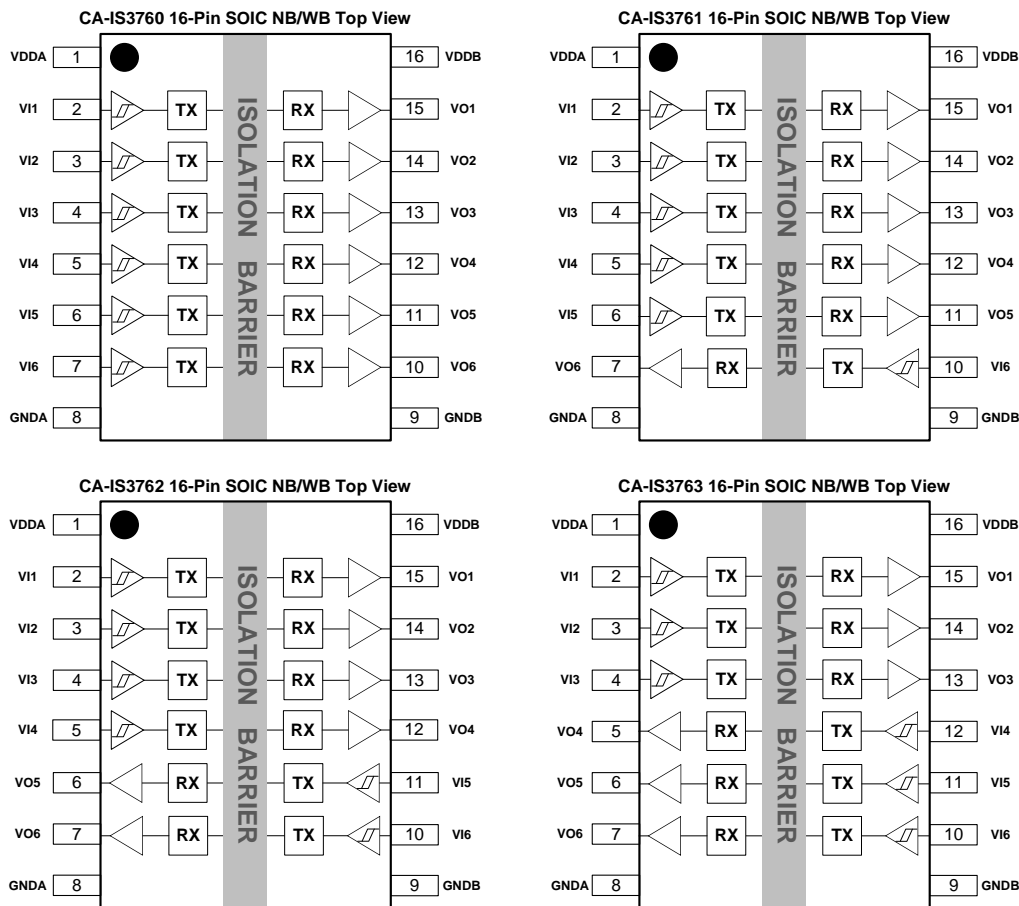


Figure 6-1 CA-IS376x Top View

Table 6-1 CA-IS376x Pin Description and Functions

Name	SOIC16 Pin#	Type	Description
VDDA	1	Supply	Side A Power Supply
VI1	2	Digital Input	Side A Digital Input
VI2	3	Digital Input	Side A Digital Input
VI3	4	Digital Input	Side A Digital Input
VI4/VO4	5	Digital I/O	Side A Digital Input for CA-IS3760/61/62 or Output for CA-IS3763
VI5/VO5	6	Digital I/O	Side A Digital Input for CA-IS3760/61 or Output for CA-IS3762/63
VI6/VO6	7	Digital I/O	Side A Digital Input for CA-IS3760 or Output for CA-IS3761/62/63
GNDA	8	Ground	Side A Ground
GNDB	9	Ground	Side B Ground
VI6/VO6	10	Digital I/O	Side B Digital Input for CA-IS3761/62/63 or Output for CA-IS3760
VI5/VO5	11	Digital I/O	Side B Digital Input for CA-IS3762/63 or Output for CA-IS3760/61
VI4/VO4	12	Digital I/O	Side B Digital Input for CA-IS3763 or Output for CA-IS3760/61/62
VO3	13	Digital Output	Side B Digital Output
VO2	14	Digital Output	Side B Digital Output
VO1	15	Digital Output	Side B Digital Output
VDDB	16	Supply	Side B Power Supply

7 Specifications

7.1 Absolute Maximum Ratings¹

		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage ²	-0.5	6.0	V
V_{in}	Voltage at Ax, Bx, ENx	-0.5	$V_{DDA}+0.5^3$	V
I_O	Output Current	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±6000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ²	±2000	

NOTE:

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage	2.375	3.3	5.5	V
$V_{DD} (UVLO+)$	VDD Undervoltage Threshold When Supply Voltage is Rising	1.95	2.24	2.375	V
$V_{DD} (UVLO-)$	VDD Undervoltage Threshold When Supply Voltage is Falling	1.88	2.10	2.325	V
$V_{HYS} (UVLO)$	VDD Undervoltage Threshold Hysteresis	70	140	250	mV
I_{OH}	High-level Output Current	$V_{DDO}^1 = 5V$	-4		mA
		$V_{DDO} = 3.3V$	-2		
		$V_{DDO} = 2.5V$	-1		
I_{OL}	Low-level Output Current	$V_{DDO} = 5V$		4	mA
		$V_{DDO} = 3.3V$		2	
		$V_{DDO} = 2.5V$		1	
V_{IH}	High-level Input Voltage	2.0			V
V_{IL}	Low-level Input Voltage			0.8	V
DR	Data Rate	0		150	Mbps
T_A	Ambient Temperature	-55	27	125	°C

NOTE:

- V_{DDO} = Output-side V_{DD}

7.4 Thermal Information

THERMAL METRIC	CA-IS376x		UNIT
	N (SOIC)	W (SOIC)	
	16 Pins	16 Pins	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	96.2	83.4	°C/W

7.5 Power Rating

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IS3760					
P_D Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_J = 150^\circ\text{C}$, Input a 75-MHz 50% duty cycle square wave			494	mW
P_{DA} Maximum Power Dissipation on Side-A				49	mW
P_{DB} Maximum Power Dissipation on Side-B				445	mW
CA-IS3761					
P_D Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_J = 150^\circ\text{C}$, Input a 75-MHz 50% duty cycle square wave			494	mW
P_{DA} Maximum Power Dissipation on Side-A				113	mW
P_{DB} Maximum Power Dissipation on Side-B				381	mW
CA-IS3762					
P_D Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_J = 150^\circ\text{C}$, Input a 75-MHz 50% duty cycle square wave			494	mW
P_{DA} Maximum Power Dissipation on Side-A				180	mW
P_{DB} Maximum Power Dissipation on Side-B				314	mW
CA-IS3763					
P_D Maximum Power Dissipation	$V_{DDA} = V_{DDB} = 5.5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_J = 150^\circ\text{C}$, Input a 75-MHz 50% duty cycle square wave			494	mW
P_{DA} Maximum Power Dissipation on Side-A				247	mW
P_{DB} Maximum Power Dissipation on Side-B				247	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE		UNIT
			W	N	
CLR	External clearance ¹	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage ¹	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	19	19	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 400 V _{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	n/a	
DIN V VDE V 0884-11:2017-01²					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	566	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDb) Test	600	400	V _{RMS}
		DC voltage	849	566	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	7070	5300	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ³	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	6250	5000	V _{PK}
Q _{pd}	Apparent charge ⁴	Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	≤5	
		Method b1, At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	≤5	
C _{IO}	Barrier capacitance, input to output ⁵	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	~0.5	pF
R _{IO}	Isolation resistance ⁵	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	>10 ⁹	
	Pollution degree		2	2	
UL 1577					
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	3750	V _{RMS}
NOTE:					
1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.					
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.					
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.					
4. Apparent charge is electrical discharge caused by a partial discharge (pd).					
5. All pins on each side of the barrier tied together creating a two-terminal device.					

7.7 Safety-Related Certifications

VDE(Pending)	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011 and GB 8898-2011	Certified according to EN/IEC 61010-1:2010 (3rd Ed) and EN /IEC 62368-1:2014+A11:2017
	SOP16-N: 3750 V _{RMS} ; SOP16-W: 5000 V _{RMS}	SOP16-N: Basic Insulation, 400 V _{RMS} maximum working voltage; SOP16-W: Reinforced Insulation, 600 V _{RMS} maximum working voltage (Altitude ≤ 5000 m)	5000 V _{RMS} (SOP16-W) and 3750 V _{RMS} (SOP16-N) Reinforced insulation per EN/IEC 61010-1:2010 (3rd Ed) and EN/IEC 62368-1:2014+A11:2017 up to working voltage of 600 V _{RMS} (SOP16-W) and 400 V _{RMS} (SOP16-N)
	File number: E511334	Certificate number SOP16-N: CQC20001251750 SOP16-W: CQC20001251466	CB Certificate number: JPTUV-111116; DE 2-027880 AK Certificate number: AK 50474784 0001; AK 50474786 0001

7.8 Electrical Characteristics

7.8.1 5 V Electrical Characteristics

 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$, $T_A = -55$ to 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; <i>See Figure 8-1</i>	$V_{DDO}^{1-0.4}$	4.8		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; <i>See Figure 8-1</i>		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold	1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold	1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at Ax or Bx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; <i>See Figure 8-3</i>	75	100		$\text{kV}/\mu\text{S}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 5\text{ V}$		2		pF

NOTE:

- V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}
- The nominal output impedance of an isolator driver channel is approximately $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

7.8.2 3.3 V Electrical Characteristics

 $V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -55$ to 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; <i>See Figure 8-1</i>	$V_{DDO}^{1-0.4}$	3.1		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; <i>See Figure 8-1</i>		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold	1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold	1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at Ax or Bx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; <i>See Figure 8-3</i>	75	100		$\text{kV}/\mu\text{S}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$		2		pF

NOTE:

- V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}
- The nominal output impedance of an isolator driver channel is approximately $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

7.8.3 2.5 V Electrical Characteristics

 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 5\%$, $T_A = -55$ to 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage $I_{OH} = -4\text{mA}$; <i>See Figure 8-1</i>	$V_{DDO}^{1-0.4}$	2.3		V
V_{OL}	Low-level Output Voltage $I_{OL} = 4\text{mA}$; <i>See Figure 8-1</i>		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold	1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold	1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis	0.30	0.44	0.50	V
I_{IH}	High-Level Input Leakage Current $V_{IH} = V_{DDA}$ at Ax or Bx or ENx			20	μA
I_{IL}	Low-Level Input Leakage Current $V_{IL} = 0\text{ V}$ at Ax or Bx	-20			μA
Z_O	Output Impedance ²		50		Ω
CMTI	Common-mode Transient Immunity $V_I = V_{DDI}^1$ or 0 V , $V_{CM} = 1200\text{ V}$; <i>See Figure 8-3</i>	75	100		$\text{kV}/\mu\text{S}$
C_i	Input Capacitance ³ $V_I = V_{DD}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$		2		pF

NOTE:

- V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}
- The nominal output impedance of an isolator driver channel is approximately $50\ \Omega \pm 40\%$.
- Measured from pin to Ground.

7.9 Supply Current Characteristics
7.9.1 5 V Supply Current Characteristics
 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$, $T_A = -55$ to 125°C

PARAMETER	TEST CONDITION	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3760						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L);	I_{DDA}		1.4	2.1	mA
	$V_{IN} = V_{DDA}$ (CA-IS3760H)	I_{DDB}		4.2	6.2	
	$V_{IN} = V_{DDA}$ (CA-IS3760L);	I_{DDA}		5.9	8.9	
	$V_{IN} = 0\text{V}$ (CA-IS3760H)	I_{DDB}		4.4	6.6	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	3.7	5.5	
		10Mbps (5MHz)	I_{DDB}	4.6	6.9	
			I_{DDA}	3.7	5.5	
		100Mbps (50MHz)	I_{DDB}	7.5	11.2	
			I_{DDA}	3.7	5.5	
		I_{DDB}	36.0	53.9		
CA-IS3761						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L);	I_{DDA}		1.9	2.9	mA
	$V_{IN} = V_{DDI}^1$ (CA-IS3761H)	I_{DDB}		2.9	5.9	
	$V_{IN} = V_{DDI}$ (CA-IS3761L);	I_{DDA}		5.7	8.5	
	$V_{IN} = 0\text{V}$ (CA-IS3761H)	I_{DDB}		4.9	7.3	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	3.9	5.8	
		10Mbps (5MHz)	I_{DDB}	4.7	7.0	
			I_{DDA}	4.4	6.5	
		100Mbps (50MHz)	I_{DDB}	7.0	10.5	
			I_{DDA}	9.1	13.7	
		I_{DDB}	30.8	46.2		
CA-IS3762						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L);	I_{DDA}		2.4	3.6	mA
	$V_{IN} = V_{DDI}$ (CA-IS3762H)	I_{DDB}		3.4	5.1	
	$V_{IN} = V_{DDI}$ (CA-IS3762L);	I_{DDA}		5.5	8.2	
	$V_{IN} = 0\text{V}$ (CA-IS3762H)	I_{DDB}		5.1	7.6	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	4.1	6.1	
		10Mbps (5MHz)	I_{DDB}	4.5	6.7	
			I_{DDA}	5.0	7.5	
		100Mbps (50MHz)	I_{DDB}	6.4	9.5	
			I_{DDA}	14.5	21.8	
		I_{DDB}	25.4	38.0		
CA-IS3763						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L);	I_{DDA}		2.9	4.4	mA
	$V_{IN} = V_{DDI}$ (CA-IS3763H)	I_{DDB}		2.9	4.4	
	$V_{IN} = V_{DDI}$ (CA-IS3763L);	I_{DDA}		5.3	7.9	
	$V_{IN} = 0\text{V}$ (CA-IS3763H)	I_{DDB}		5.3	7.9	
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	4.3	6.4	
		10Mbps (5MHz)	I_{DDB}	4.3	6.4	
			I_{DDA}	5.7	8.5	
		100Mbps (50MHz)	I_{DDB}	5.7	8.5	
			I_{DDA}	19.9	29.9	
		I_{DDB}	19.9	29.9		
Note:						
1. V_{DDI} = Input-side V_{DD}						

7.9.2 3.3 V Supply Current Characteristics
 $V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -55\text{ to }125^\circ\text{C}$

PARAMETER	TEST CONDITION	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3760						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)	I_{DDA}	1.4	2.1		mA
		I_{DDB}	4.2	6.2		
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0\text{V}$ (CA-IS3760H)	I_{DDA}	5.9	8.9		
		I_{DDB}	4.4	6.6		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	3.7	5.5	
			I_{DDB}	4.6	6.9	
		10Mbps (5MHz)	I_{DDA}	3.7	5.5	
			I_{DDB}	6.7	10.0	
		100Mbps (50MHz)	I_{DDA}	3.7	5.5	
			I_{DDB}	27.0	40.4	
CA-IS3761						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)	I_{DDA}	1.9	2.9		mA
		I_{DDB}	2.9	5.9		
	$V_{IN} = V_{DDI}$ (CA-IS3761L); $V_{IN} = 0\text{V}$ (CA-IS3761H)	I_{DDA}	5.7	8.5		
		I_{DDB}	4.9	7.3		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	3.9	5.8	
			I_{DDB}	4.7	7.0	
		10Mbps (5MHz)	I_{DDA}	4.2	6.3	
			I_{DDB}	6.4	9.6	
		100Mbps (50MHz)	I_{DDA}	7.6	11.4	
			I_{DDB}	23.3	34.9	
CA-IS3762						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L); $V_{IN} = V_{DDI}$ (CA-IS3762H)	I_{DDA}	2.4	3.6		mA
		I_{DDB}	3.4	5.1		
	$V_{IN} = V_{DDI}$ (CA-IS3762L); $V_{IN} = 0\text{V}$ (CA-IS3762H)	I_{DDA}	5.5	8.2		
		I_{DDB}	5.1	7.6		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	4.1	6.1	
			I_{DDB}	4.5	6.7	
		10Mbps (5MHz)	I_{DDA}	4.8	7.1	
			I_{DDB}	5.8	8.8	
		100Mbps (50MHz)	I_{DDA}	11.5	17.3	
			I_{DDB}	19.4	29.0	
CA-IS3763						
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L); $V_{IN} = V_{DDI}$ (CA-IS3763H)	I_{DDA}	2.9	4.4		mA
		I_{DDB}	2.9	4.4		
	$V_{IN} = V_{DDI}$ (CA-IS3763L); $V_{IN} = 0\text{V}$ (CA-IS3763H)	I_{DDA}	5.3	7.9		
		I_{DDB}	5.3	7.9		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}	4.3	6.4	
			I_{DDB}	4.3	6.4	
		10Mbps (5MHz)	I_{DDA}	5.3	8.0	
			I_{DDB}	5.3	8.0	
		100Mbps (50MHz)	I_{DDA}	15.4	23.2	
			I_{DDB}	15.4	23.2	
Note:						
1. V_{DDI} = Input-side V_{DD}						

7.9.3 2.5 V Supply Current Characteristics
 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 5\%$, $T_A = -55$ to 125°C

PARAMETER	TEST CONDITION	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
CA-IS3760							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3760L); $V_{IN} = V_{DDA}$ (CA-IS3760H)	I_{DDA}		1.4	2.1	mA	
		I_{DDB}		4.2	6.2		
	$V_{IN} = V_{DDA}$ (CA-IS3760L); $V_{IN} = 0\text{V}$ (CA-IS3760H)	I_{DDA}		5.9	8.9		
		I_{DDB}		4.4	6.6		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}		3.7		5.5
			I_{DDB}		4.6		6.9
		10Mbps (5MHz)	I_{DDA}		3.7		5.5
			I_{DDB}		6.1		9.2
		100Mbps (50MHz)	I_{DDA}		3.7	5.5	
			I_{DDB}		21.0	31.4	
CA-IS3761							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3761L); $V_{IN} = V_{DDI}^1$ (CA-IS3761H)	I_{DDA}		1.9	2.9	mA	
		I_{DDB}		2.9	5.9		
	$V_{IN} = V_{DDI}$ (CA-IS3761L); $V_{IN} = 0\text{V}$ (CA-IS3761H)	I_{DDA}		5.7	8.5		
		I_{DDB}		4.9	7.3		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}		3.9		5.8
			I_{DDB}		4.7		7.0
		10Mbps (5MHz)	I_{DDA}		4.1		6.2
			I_{DDB}		5.9		8.9
		100Mbps (50MHz)	I_{DDA}		6.6	9.9	
			I_{DDB}		18.3	27.4	
CA-IS3762							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3762L); $V_{IN} = V_{DDI}$ (CA-IS3762H)	I_{DDA}		2.4	3.6	mA	
		I_{DDB}		3.4	5.1		
	$V_{IN} = V_{DDI}$ (CA-IS3762L); $V_{IN} = 0\text{V}$ (CA-IS3762H)	I_{DDA}		5.5	8.2		
		I_{DDB}		5.1	7.6		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}		4.1		6.1
			I_{DDB}		4.5		6.7
		10Mbps (5MHz)	I_{DDA}		4.6		6.9
			I_{DDB}		5.5		8.2
		100Mbps (50MHz)	I_{DDA}		9.5	14.3	
			I_{DDB}		15.4	23.0	
CA-IS3763							
Supply Current – DC Signal	$V_{IN} = 0\text{V}$ (CA-IS3763L); $V_{IN} = V_{DDI}$ (CA-IS3763H)	I_{DDA}		2.9	4.4	mA	
		I_{DDB}		2.9	4.4		
	$V_{IN} = V_{DDI}$ (CA-IS3763L); $V_{IN} = 0\text{V}$ (CA-IS3763H)	I_{DDA}		5.3	7.9		
		I_{DDB}		5.3	7.9		
Supply Current – AC Signal	All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; $C_L = 15\text{ pF}$ for Each Channel	1Mbps (500kHz)	I_{DDA}		4.3		6.4
			I_{DDB}		4.3		6.4
		10Mbps (5MHz)	I_{DDA}		5.0		7.5
			I_{DDB}		5.0		7.5
		100Mbps (50MHz)	I_{DDA}		12.4	18.7	
			I_{DDB}		12.4	18.7	
Note:							
1. V_{DDI} = Input-side V_{DD}							

7.10 Timing Characteristics

7.10.1 5 V Timing Characteristics

 $V_{DDA} = V_{DDB} = 5\text{ V} \pm 10\%$, $T_A = -55$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW _{min}	Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL}	Propagation Delay Time	See Figure 8-1	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion t _{PLH} - t _{PHL}		0.2	4.5		ns
t _{sk}	Channel-to-channel Output Skew Time ¹	Same-direction channels	0.4	4.5		ns
t _r	Output Signal Rise Time	See Figure 8-1	2.5	4.0		ns
t _f	Output Signal Fall Time	See Figure 8-1	2.5	4.0		ns
t _{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2	8	12		ns
t _{SU}	Start-up Time		15	40		μs

NOTE:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.10.2 3.3 V Timing Characteristics

 $V_{DDA} = V_{DDB} = 3.3\text{ V} \pm 10\%$, $T_A = -55$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW _{min}	Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL}	Propagation Delay Time	See Figure 8-1	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion t _{PLH} - t _{PHL}		0.2	4.5		ns
t _{sk}	Channel-to-channel Output Skew Time ¹	Same-direction channels	0.4	4.5		ns
t _r	Output Signal Rise Time	See Figure 8-1	2.5	4.0		ns
t _f	Output Signal Fall Time	See Figure 8-1	2.5	4.0		ns
t _{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2	8	12		ns
t _{SU}	Start-up Time		15	40		μs

NOTE:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

7.10.3 2.5 V Timing Characteristics

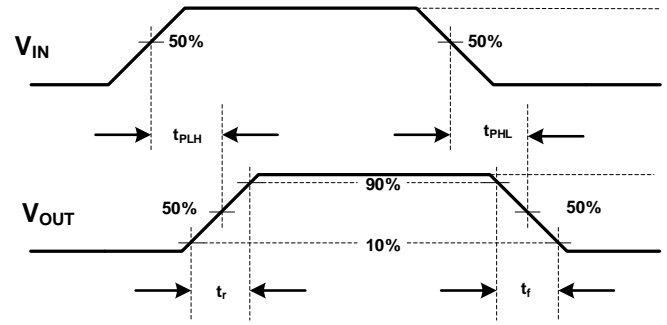
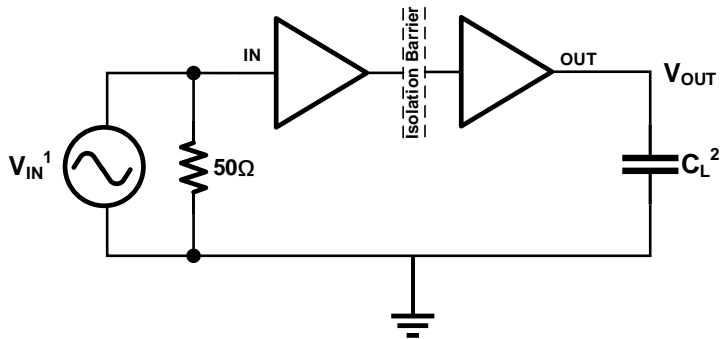
 $V_{DDA} = V_{DDB} = 2.5\text{ V} \pm 5\%$, $T_A = -55$ to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate		0		150	Mbps
PW _{min}	Minimum Pulse Width				5.0	ns
t _{PLH} , t _{PHL}	Propagation Delay Time	See Figure 8-1	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion t _{PLH} - t _{PHL}		0.2	5.0		ns
t _{sk}	Channel-to-channel Output Skew Time ¹	Same-direction channels	0.4	4.5		ns
t _r	Output Signal Rise Time	See Figure 8-1	2.5	4.0		ns
t _f	Output Signal Fall Time	See Figure 8-1	2.5	4.0		ns
t _{DO}	Default Output Delay Time from Input Power Loss	See Figure 8-2	8	12		ns
t _{SU}	Start-up Time		15	40		μs

NOTE:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

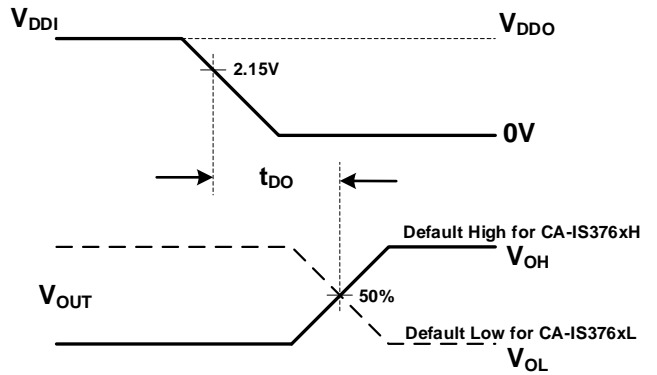
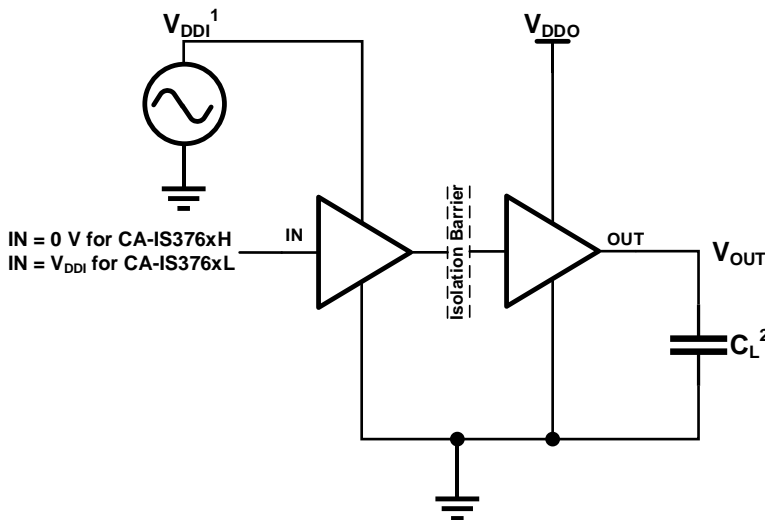
8 Parameter Measurement Information



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: waveform frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$. Since the waveform generator has an output impedance of $Z_{out} = 50\Omega$, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

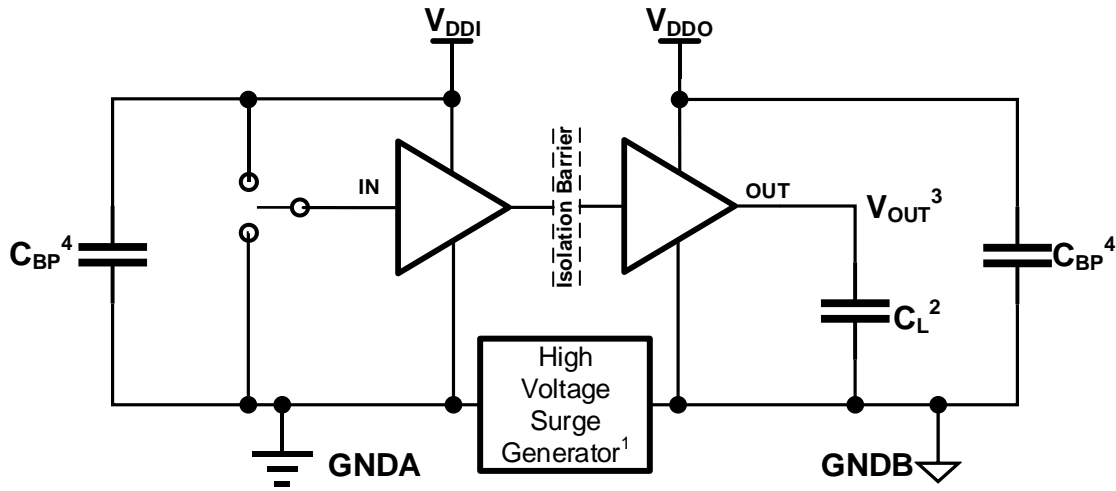
Figure 8-1 Timing Characteristics Test Circuit and Voltage Waveforms



NOTE:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.15V but no higher than 5.5V.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2 Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 100kV/μs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 ~ 1uF bypass capacitance.

Figure 8-3 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Theory of Operation

The CA-IS37xx family of devices use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO₂ isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. This simple architecture offers a robust isolated data path and requires no special considerations or initialization at start-up. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. Advanced circuitry techniques are applied for better EMI introduced by the carrier signal and IO switching. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively-coupled one. And OOK modulation scheme eliminates the missing-pulse error that occurs in the pulse modulation method. A simplified functional block diagram and conceptual operation waveforms of a single channel is shown in Figure 9-1 and Figure 9-2.

9.2 Functional Block Diagram

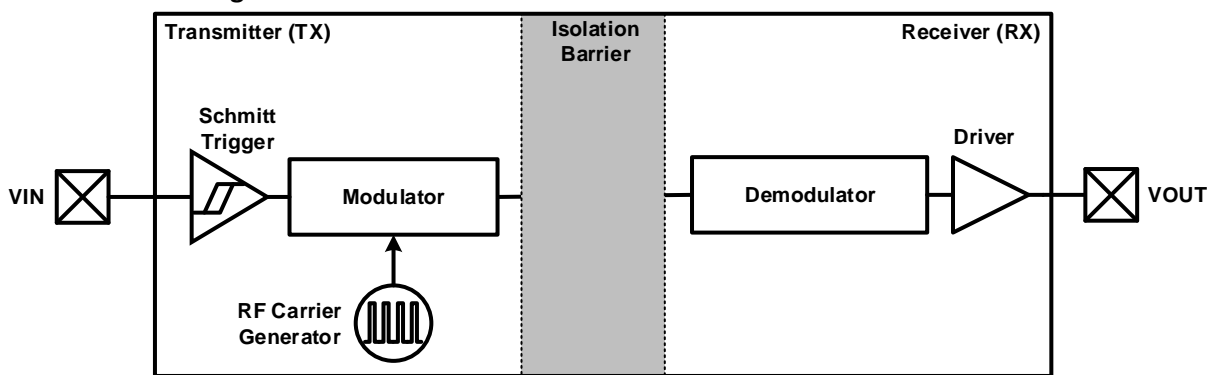


Figure 9-1 Functional Block Diagram of a Single Channel

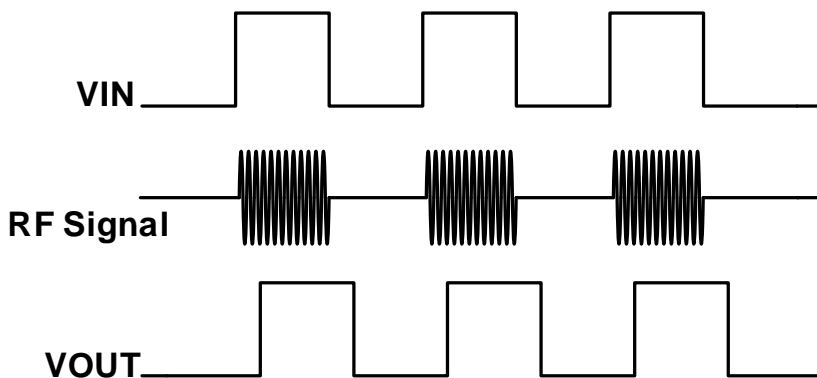


Figure 9-2 Conceptual Operation Waveforms of a Single Channel

9.3 Device Operation Modes

Table 9-1 provides the operation modes for the CA-IS376x devices.

Table 9-1 Operation Mode Table¹

V _{DDI}	V _{DDO}	INPUT(A _x /B _x) ²	OUTPUT (A _x /B _x)	OPERATION
PU	PU	H	H	Normal operation mode: A channel's output follows the input state
		L	L	
		Open	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default value (Low for CA-IS376xL and High for CA-IS376xH).
PD	PU	X	Default	Default output fail-safe mode: If the input side VDD is unpowered, the outputs go in to the default output fail-safe mode (Low for CA-IS376xL and High for CA-IS376xH)
X	PD	X	Undetermined	If the output side VDD is unpowered, the outputs' states are undetermined ³ .

NOTE:

1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (VCC ≥ 2.375 V); PD = Powered down (VCC ≤ 2.25 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when 2.25V < V_{DDI}, V_{DDO} < 2.375 V.

10 Application and Implementation

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the CA-IS376x family device CMOS digital isolator needs only two external VDD bypass capacitors (0.1μF to 1 μF) to operate. Its TTL level compatible input terminals draw only micro amps of leakage current, allowing them to be driven without external buffering circuits. The output terminals have a characteristic impedance of 50 Ω (rail-to-rail swing) and are available in both forward and reverse channel configurations. Figure 10-1 shows the typical application of CA-IS3763 device. And the circuit of Figure 10-2 is typical for most applications of CA-IS37xx series products and is as easy to use as a standard logic gate.

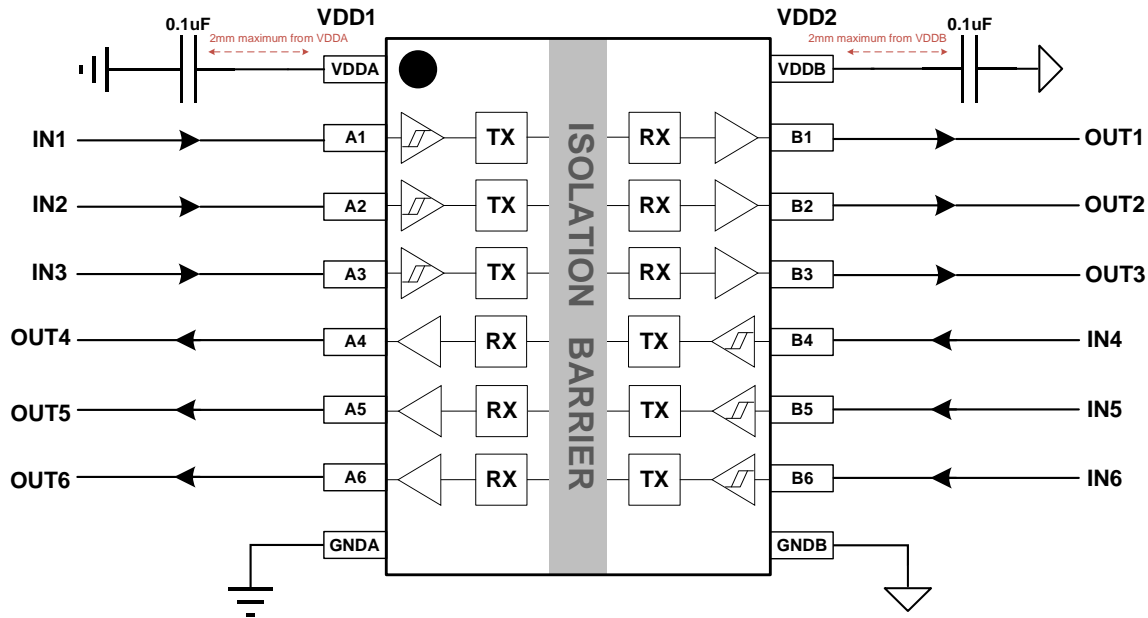


Figure 10-1 Typical Application Circuit of CA-IS3763

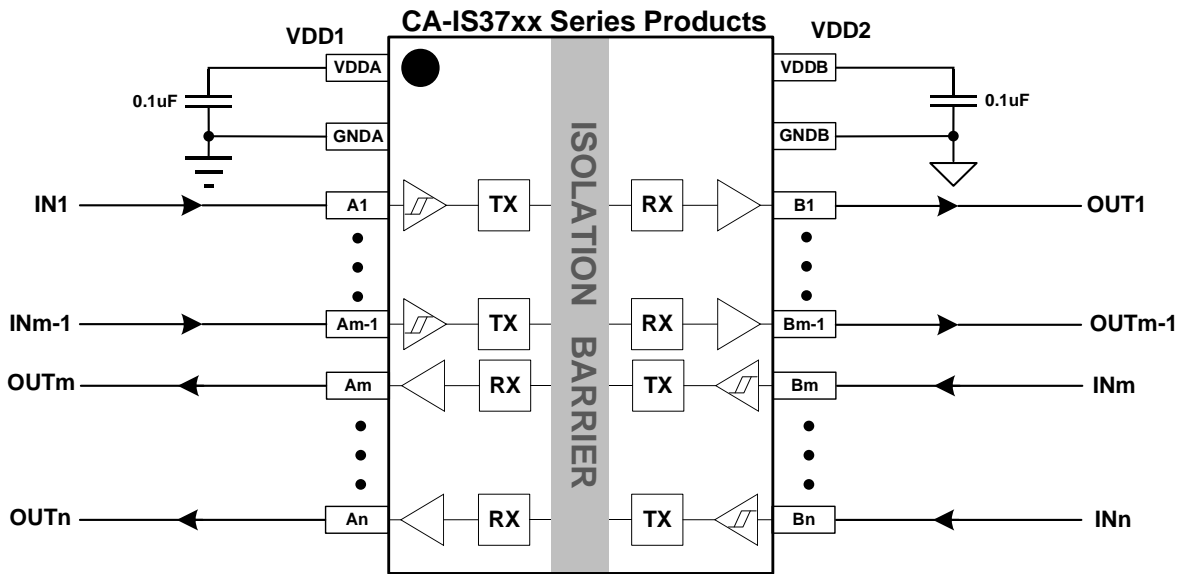
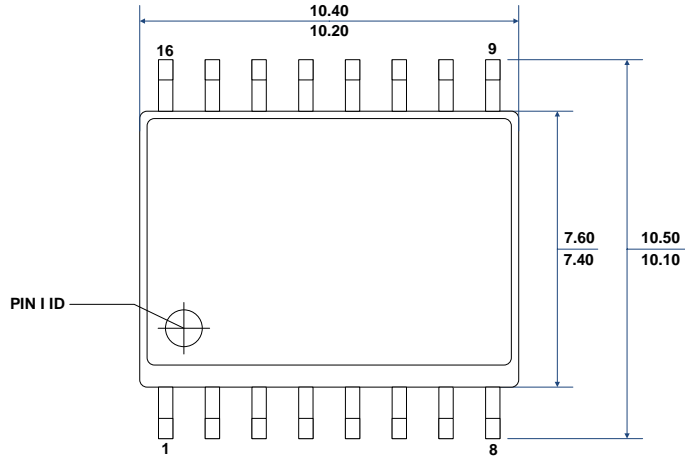


Figure 10-2 CA-IS37xx Series Digital Isolator Application Schematic

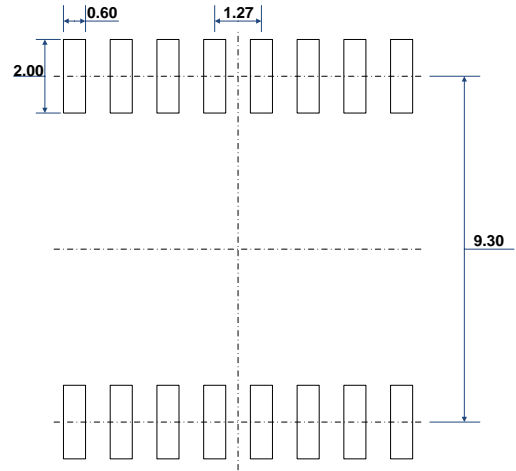
11 Package Information

11.1 16-Pin Wide Body SOIC Package

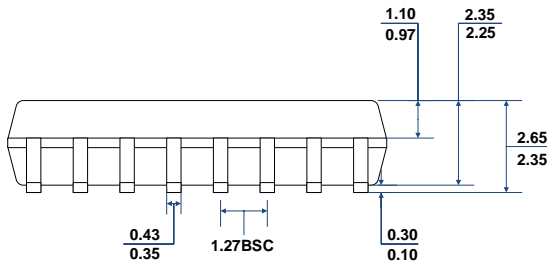
The figure below illustrates the package details and the recommended land pattern details for the CA-IS376x digital isolator in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



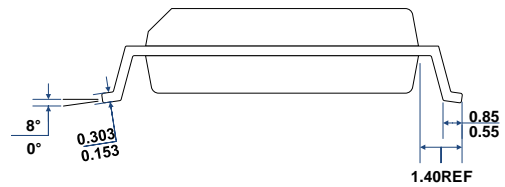
TOP VIEW



RECOMMENDED LAND PATTERN



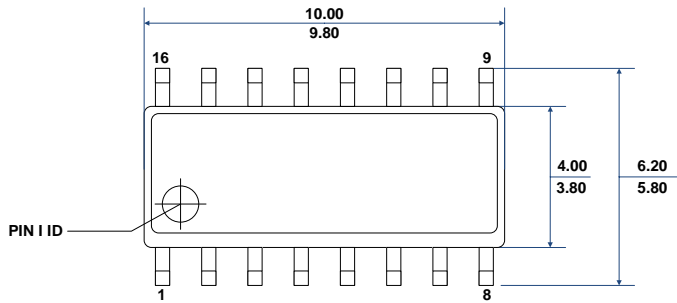
FRONT VIEW



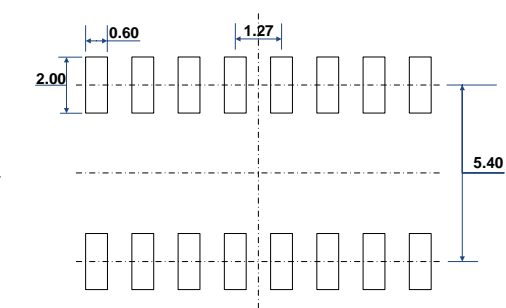
LEFT-SIDE VIEW

11.2 16-Pin Narrow Body SOIC Package

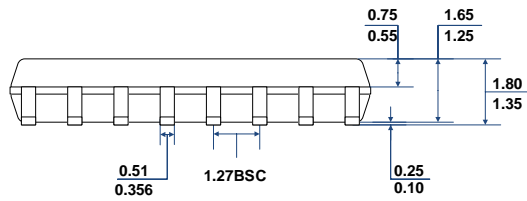
The figure below illustrates the package details and the recommended land pattern details for the CA-IS376x digital isolator in a 16-pin narrow-body SOIC package. The values for the dimensions are shown in millimeters.



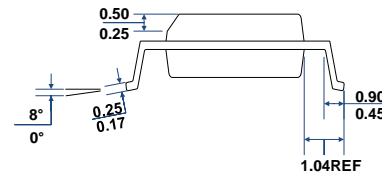
TOP VIEW



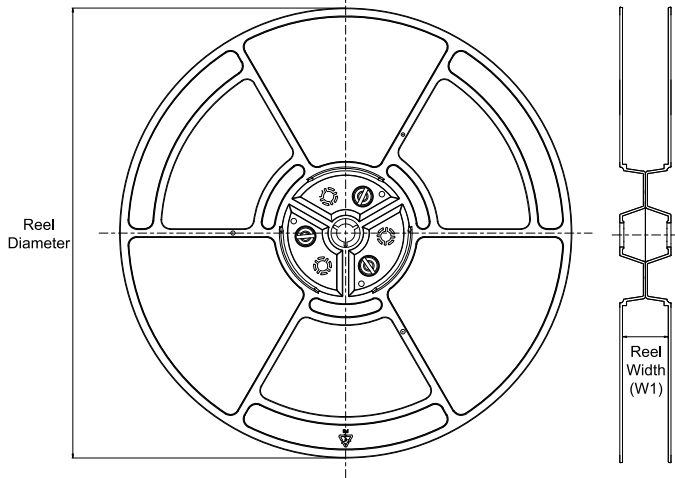
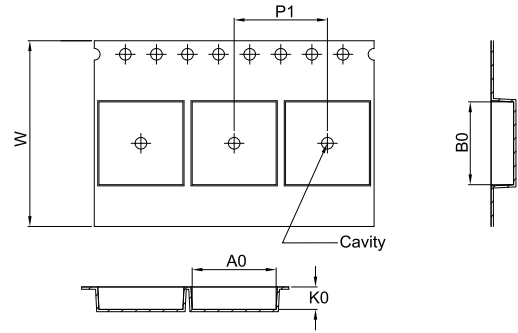
RECOMMENDED LAND PATTERN



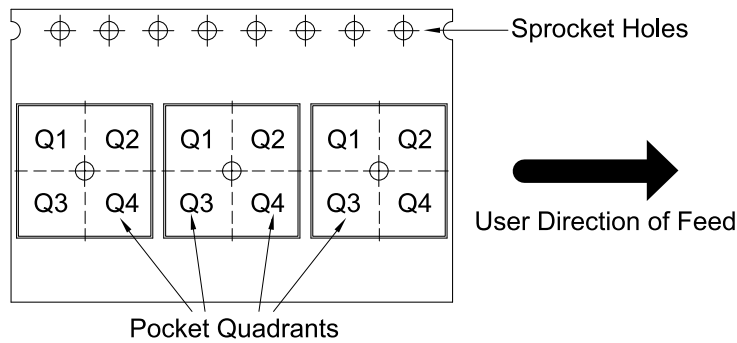
FRONT VIEW



LEFT-SIDE VIEW

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3760LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3760LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3760HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3760HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3761LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3761LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3761HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3761HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3762LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3762LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3762HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3762HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3763LN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3763LW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3763HN	SOIC	N	16	2500	330	12.4	6.5	10.3	2.1	8.0	16.0	Q1
CA-IS3763HW	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

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