

■ GENERAL DESCRIPTION

DK130G70 integrates an E-MODE GaN-specific driver IC and a 700V 101mΩ GaN power transistor. It can replace traditional silicon-based MOSFETs or D-MODE GaN devices.

■ FEATURES

- ◆ Compatible with conventional PWM controllers
- ◆ Integrated 700V 101mΩ enhancement-mode GaN power transistor
- ◆ Wide gate input voltage range: 8V to 20V
- ◆ Self-powered technology, no external supply required
- ◆ Direct replacement for NMOS transistors
- ◆ Adjustable turn-on speed via external gate resistor
- ◆ Supports up to 500 kHz switching frequency
- ◆ Zero reverse recovery time
- ◆ DESAT protection

■ APPLICATIONS

- ◆ Flyback topology
- ◆ PFC topology
- ◆ LLC topology
- ◆ Fast chargers & adapters
- ◆ LED power supplies

■ MARKING DIAGRAMS

Marking	Note	DK #2501 DK130G70 ● FCT10 T01
DK	DK Semiconductor	
#	Production test code includes space, "A~Z, *#Δ"	
2501	1 st batch of 2025	
130G70	Product No.	
FCT10	Ordering code	
T01	IC code and small batch number, usually from 01 to 25	

■ Ordering code Definition

1 st digit: Package	2 nd digit: Controller Version	3 rd digit: Integrated GaN Specs	4 th digit: Pins	5 th digit: Reserved
F:PDFN8*8	C: Main controller version is C	T: 700V/101mΩ	1	0: Reserved
N:PDFN5*6	G: Main controller version is G			
T:TO-220F				
K:TO252-4R			2	

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Ordering Information

Product No.	Ordering Code	Package	Integrated GaN Specs	Packaging form
DK130G70	FCT10	PDFN8*8	700V/101mΩ	2500pcs/Tray
DK130G70	NCT10	PDFN5*6	700V/101mΩ	5000pcs/Tray
DK130G70	TCT10	TO-220F	700V/101mΩ	1000pcs/Box
DK130G70	KCT20	TO252-4R	700V/101mΩ	4000pcs/Tray
DK130G70	FGT10	PDFN8*8	700V/101mΩ	2500pcs/Tray
DK130G70	NGT10	PDFN5*6	700V/101mΩ	5000pcs/Tray
DK130G70	TGT10	TO-220F	700V/101mΩ	1000pcs/Box
DK130G70	KGT20	TO252-4R	700V/101mΩ	4000pcs/Tray

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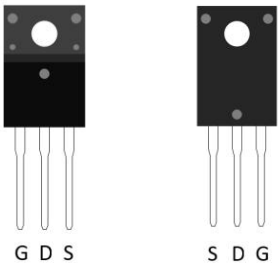
PIN CONFIGURATION

Pins name	Description
D	GaN drain
S	GaN source
G	Gate input

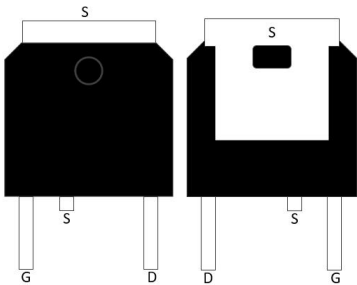
PDFN5*6/PDFN8*8



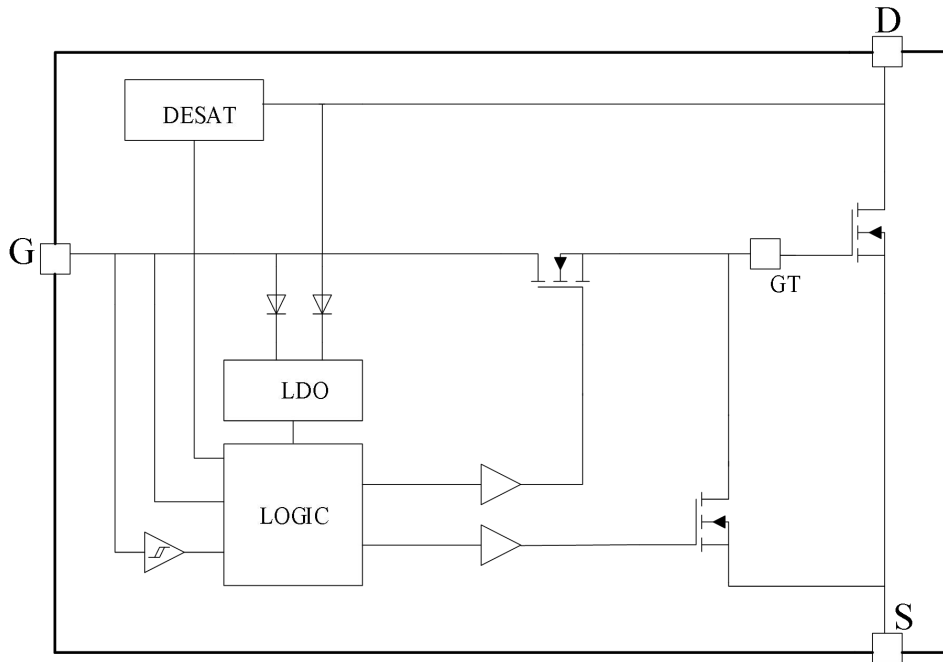
TO-220F



TO252-4R



■ **BLOCK DIAGRAM**



■ **Key Performance Parameters**($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Value	Unit
$V_{DS(max)}$	700	V
$R_{DS(on),(max)}$	130	m Ω
$I_{DS,Pulse}$	32	A
$Q_{OSS} @ 400V$	25.5	nC
Q_{rr}	0	nC

■ Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Maximum drain-source voltage	$V_{DS(MAX)}$		-2	700	V
Drain-source transient voltage ^①	$V_{DS,Pulse}$			750	V
Saturation current ^②	I_{SAT}	$TC = 125^{\circ}\text{C}$		10.5	A
Continuous drain current	I_D	$TC = 25^{\circ}\text{C}$		16	A
Pulsed drain current	$I_{D,Pulse}$	10us @ $TC = 25^{\circ}\text{C}$		32	A
Pulsed drain current	$I_{D,Pulse}$	10us @ $TC = 125^{\circ}\text{C}$		18	A
Gate voltage	V_{GS}		-0.6	20	V
Gate transient voltage	$V_{GS,Pulse}$	100ns	-5	22	V
Power dissipation	PD_{MAX}	PDFN8*8		3	W
		PDFN5*6		2	
		TO-220F		33	
		TO252-4R		1.1	
Operating junction temperature	T_j		-55	150	$^{\circ}\text{C}$
Thermal resistance (junction to case)	$R_{\theta JC}$	PDFN8*8		4	$^{\circ}\text{C/W}$
		PDFN5*6		5.5	
		TO-220F		3.8	
		TO252-4R		1.3	
Maximum junction temperature	$T_{J(MAX)}$			150	$^{\circ}\text{C}$
Storage temperature range	T_{STG}		-40	150	$^{\circ}\text{C}$
Soldering temperature	T_W			260	$^{\circ}\text{C}/10\text{s}$
Human body model (HBM) ESD	HBM	Main controller C	± 2000		V
		Main controller G	± 1750		V
Charged device model (CDM) ESD	CDM		± 1000		V

Note: Unless otherwise specified, all pins are referenced to the S-pin; Maximum ratings indicate that exceeding these limits may cause permanent damage to the device. Electrical characteristics define the DC and AC parameter specifications under guaranteed test conditions within the operating range. For parameters without specified limits, the specification does not guarantee their accuracy, but the typical values reasonably reflect device performance.

① $V_{DS,Pulse}$ allows:- Non-repetitive surge pulses <100μs (e.g., power-on, plug/unplug events)- Repetitive surge pulses <100ns (e.g., repetitive spikes caused by leakage inductance)

②: I_{SAT} is the maximum saturation current of the GaN device at 125°C . The device's saturation current is inversely proportional to its temperature, so device temperature must be considered during use. Refer to the normalized current capability curve of the GaN device in the OPERATION DESCRIPTION section below for saturation current data conversion. The actual system current setting should be determined based on the chip's temperature.

■ **Electrical Characteristics**(Unless otherwise specified: $T_A = 25^{\circ}\text{C}$, $V_{GS} = 12\text{V}$, $V_{DS} = 10\text{V to } 30\text{V}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source leakage current	I_{DSS}	$V_{DS}=700\text{V}; V_{GS}=0\text{V}; T_A = 25^{\circ}\text{C}$	-	0.6	37.5	μA
		$V_{DS}=700\text{V}; V_{GS}=0\text{V}; T_A = 150^{\circ}\text{C}$	-	4	-	μA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{V}; I_D=5\text{A}; T_A = 25^{\circ}\text{C}$	-	101	130	$\text{m}\Omega$
		$V_{GS}=6\text{V}; I_D=5\text{A}; T_A = 150^{\circ}\text{C}$	-	230	-	$\text{m}\Omega$
Gate threshold voltage	V_{GS_TH}		3.6	4	4.4	V
Gate quiescent current	I_{GON_Q}	$V_{GS}=12\text{V}$	110	135	160	μA
VGS operating voltage	V_{GS}		8		20	V
Turn-on propagation delay	T_{ON_PD}		50	75	100	ns
Turn-off propagation delay	T_{OFF_PD}		20	32	45	ns
DESAT protection threshold	V_{DS_DESAT}	Main controller version is C	3.5	3.9	4.4	V
		Main controller version is G	5.2	5.9	6.4	V
DESAT blanking time	t_{BLK_DESAT}		560	600	760	ns

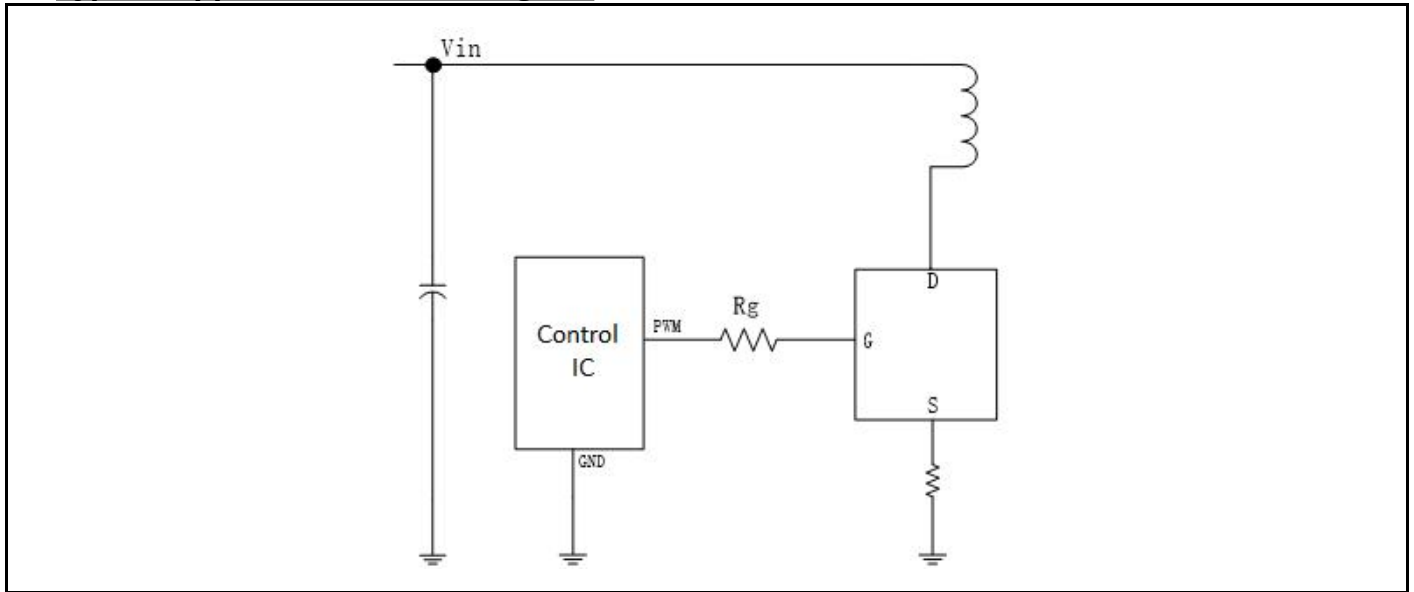
■ **Dynamic Parameters** ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output capacitance	C_{oss}	$V_{GS} = 0\text{V}; V_{DS} = 400\text{V}; f=100\text{kHz}$	-	36.5	-	pF
Effective output capacitance, energy-related	$Co(er)$	$V_{GS} = 0\text{V}; V_{DS} = 0\text{ to } 400\text{V}$	-	49	-	pF
Effective output capacitance, time-related	$Co(tr)$	$V_{GS} = 0\text{V}; V_{DS} = 0\text{ to } 400\text{V}$	-	65	-	pF
Output charge	Q_{oss}	$V_{GS} = 0\text{V}; V_{DS} = 0\text{ to } 400\text{V}$	-	25.5	-	nC

■ **Reverse Conduction Characteristics**($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-drain reverse voltage	V_{SD}	$V_{GS} = 0\text{V}; I_{SD}=5\text{A}$	-	2.4	-	V
Reverse recovery charge	Q_{rr}	$ISD = 5\text{A}; V_{DS} = 400\text{V}$	-	0	-	nC

■ Typical Application Circuit Diagram



Note: When $R_g > 500\Omega$, it is recommended to connect a reverse parallel diode to accelerate turn-off speed.

■ OPERATION DESCRIPTION

1. Operating Principle

After initial power-up, the internal VDD of the chip is charged through the D/G pin until successful power-on.

- When the chip detects a high-level input at G, the GaN turns on while VDD is powered through the G pin.
- When G input goes low, the GaN turns off. The D pin voltage then rises, and VDD is powered through D pin.

2. V_{GS} Startup and Shutdown Thresholds

GaN turns on immediately when $V_{GS} > 4V$. If V_{GS} high level is $< 4.4V$, GaN turns on after a delay (prevents false triggering from V_{GS} noise). Lower V_{GS} causes longer delays. Internal shutdown when $V_{GS} < 3.6V$.

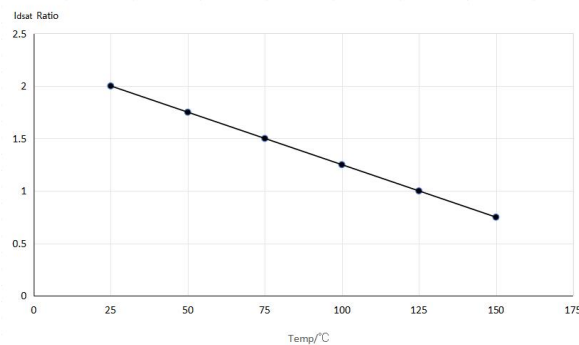
3. DESAT Protection

When GaN exceeds $I_{D,Pulse}$, DK130G70's internal driver instantly shuts off GaN to prevent saturation and ensure reliability.

Only one series resistor at G pin is needed to adjust turn-on speed (optimizes EMI). Turn-off speed is internally self-adaptive and unaffected by external adjustments.

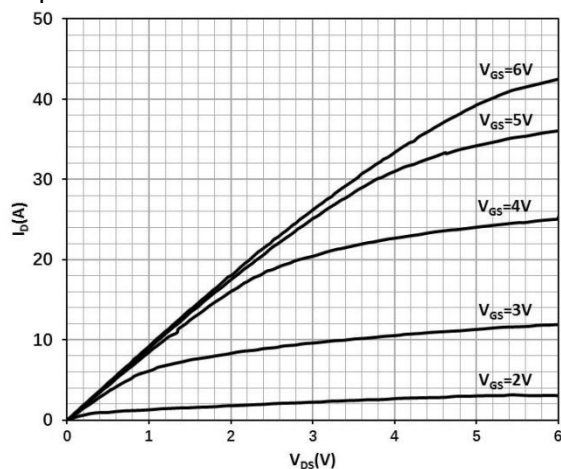
4. GaN Current Capability

Temperature significantly affects GaN's current capability. The normalized current vs. junction temperature (T_J) curve uses $T_J = 125^\circ C$ as reference. Derate current capability based on actual T_J .

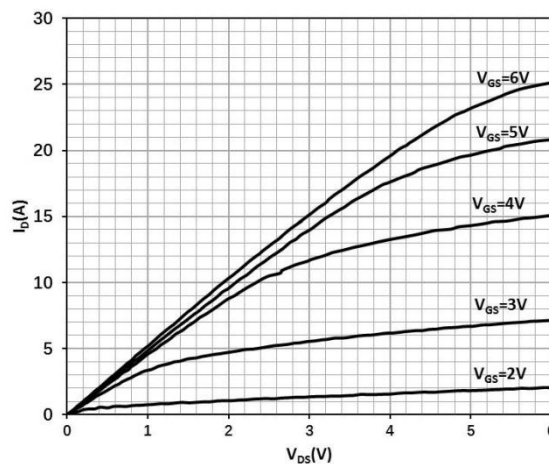


■ GaN Device Electrical characteristic curves

Typical output characteristic curve

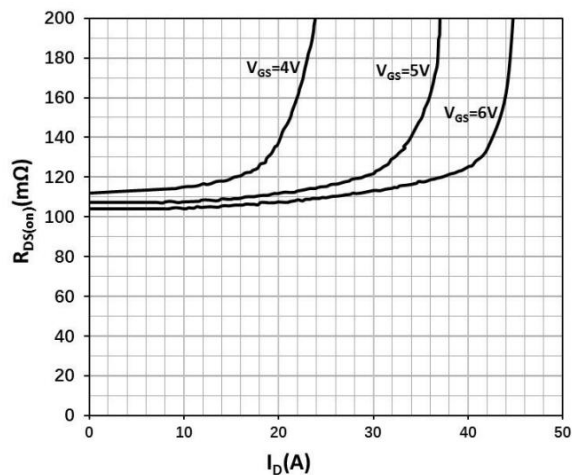


$$I_D = f(V_{DS}, V_{GS}); T_J = 25^\circ\text{C}$$

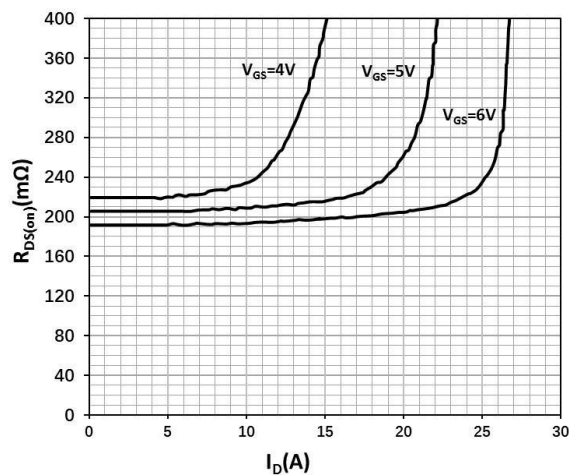


$$I_D = f(V_{DS}, V_{GS}); T_J = 125^\circ\text{C}$$

Typical drain-source on-resistance curve

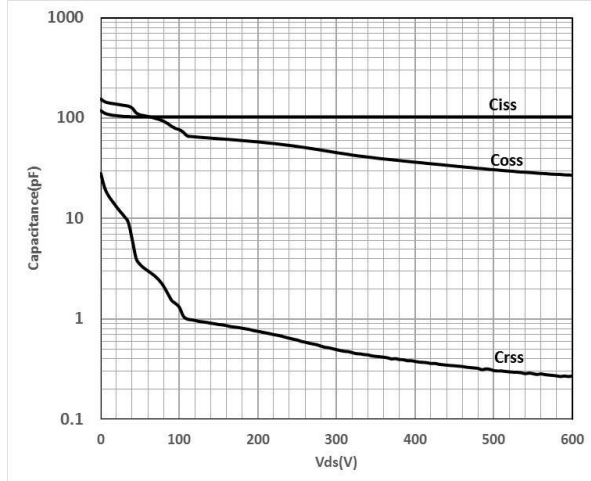


$$R_{DS(on)} = f(I_D, V_{GS}); T_J = 25^\circ\text{C}$$



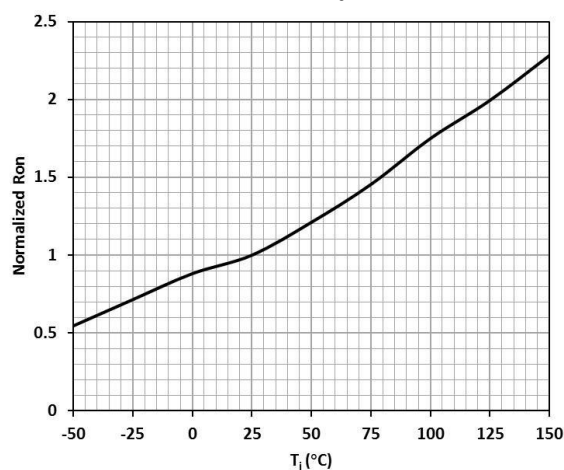
$$R_{DS(on)} = f(I_D, V_{GS}); T_J = 125^\circ\text{C}$$

Typical capacitance - VDS curve



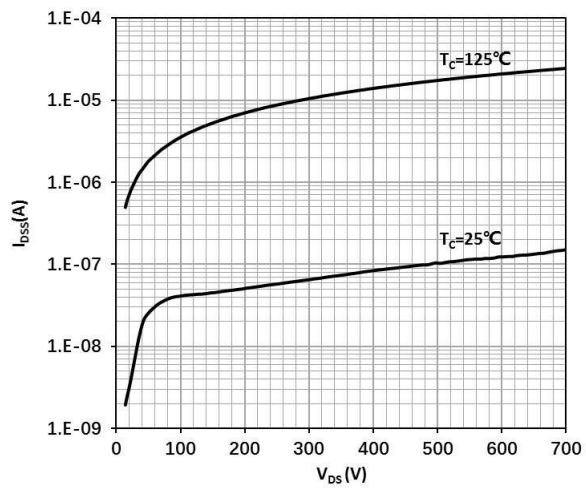
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$$

Drain-source on-resistance - Tj curve



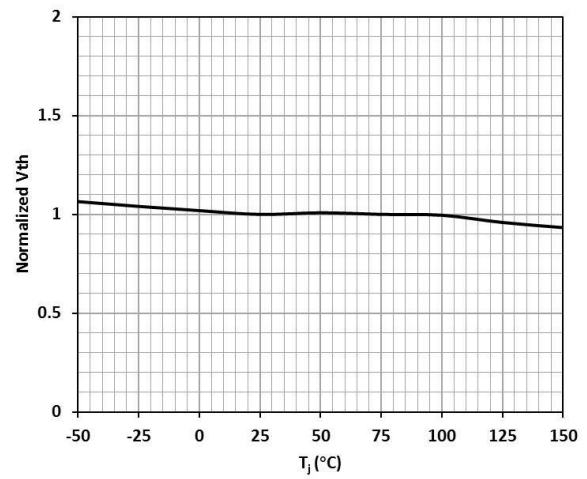
$$R_{DS(on)} = f(T_J); I_D = 5\text{A}; V_{GS} = 6\text{V}; \text{Duty} = 0.001\%$$

Drain-source leakage current - VDS curve



$$I_{DSS}=f(V_{DS}); V_{GS}=0V$$

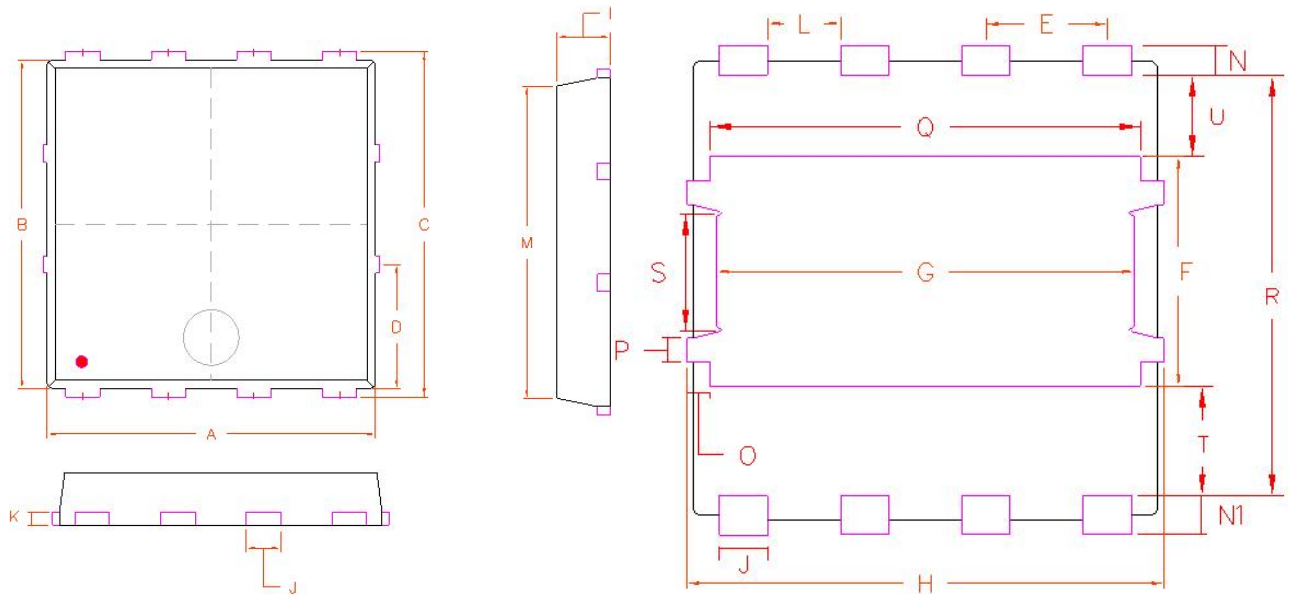
Gate threshold voltage - Tj curve



$$V_{TH}=f(T_j); V_{GS}=V_{DS}; I_D=14.3mA$$

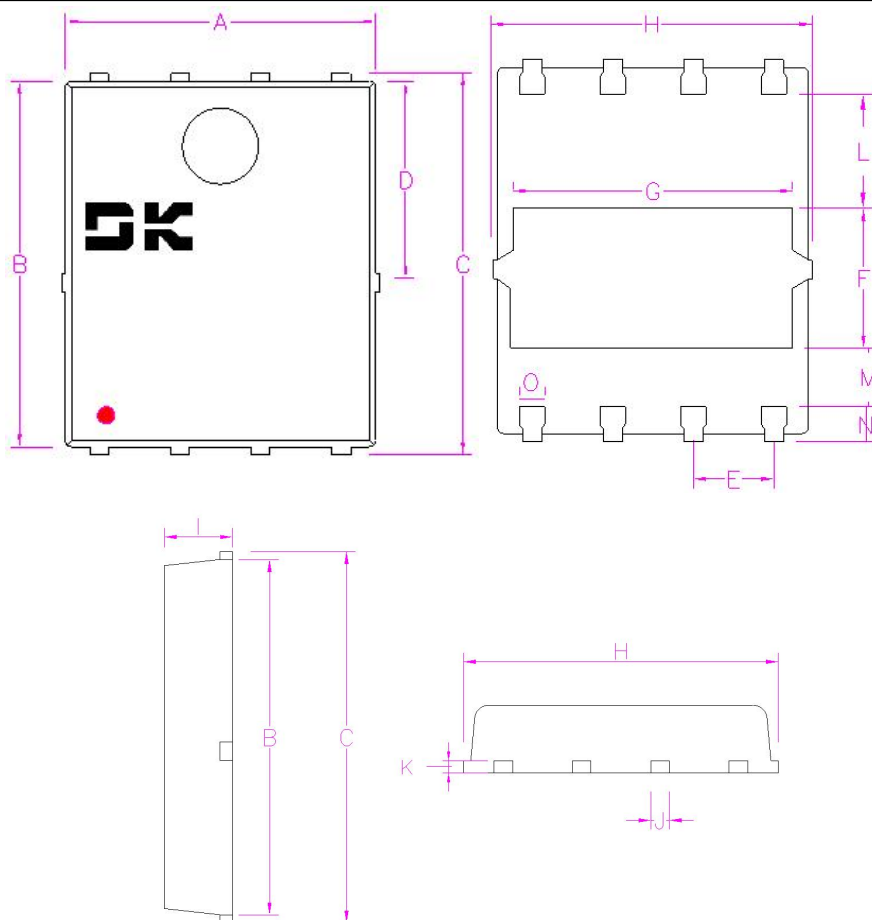
■ **PACKAGE OUTLINE DIMENSIONS**

PDFN8*8



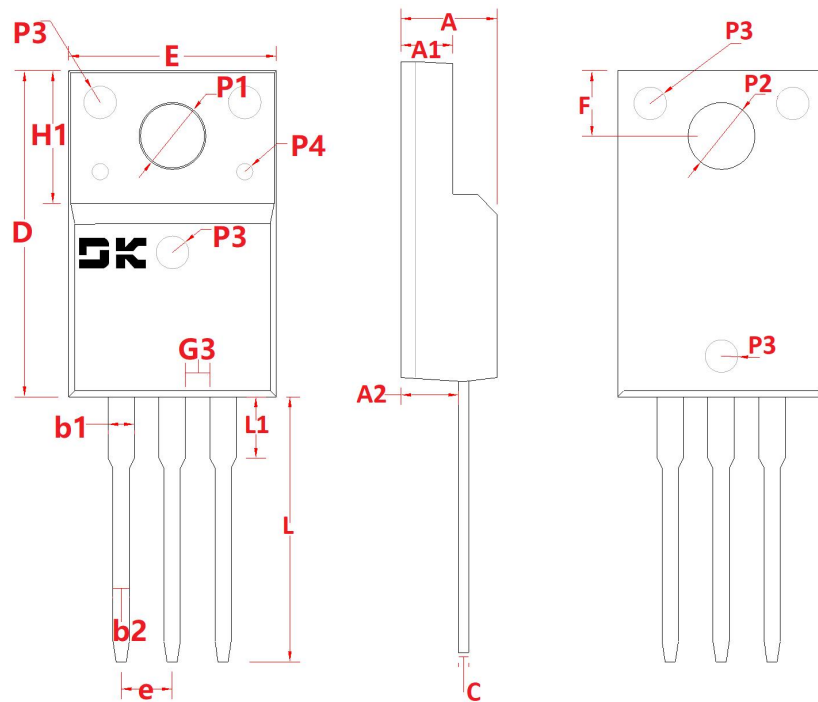
Symbol	Dimensions In Millimeters		
	Min	NOM	Max
A	7.60	7.68	7.78
B	7.60	7.68	7.78
C	8.00	8.08	8.18
D	2.90 (NOM)		
E	2.00 BSC		
F	3.80 (NOM)		
G	6.90 (NOM)		
H	7.75	7.85	7.95
I	1.20	1.23	1.30
J	0.80 (NOM)		
K	0.30 (NOM)		
L	1.15	1.20	1.25
M	7.30 (NOM)		
N	0.40	0.50	0.70
N1	0.50	0.65	0.80
O	0.30	0.40	0.50
P	0.30	0.40	0.50
Q	6.90	7.00	7.10
R	6.80	6.88	7.00
S	2.00	2.10	2.20
T	1.80	1.88	2.00
U	1.10	1.20	1.40

PDFN5*6



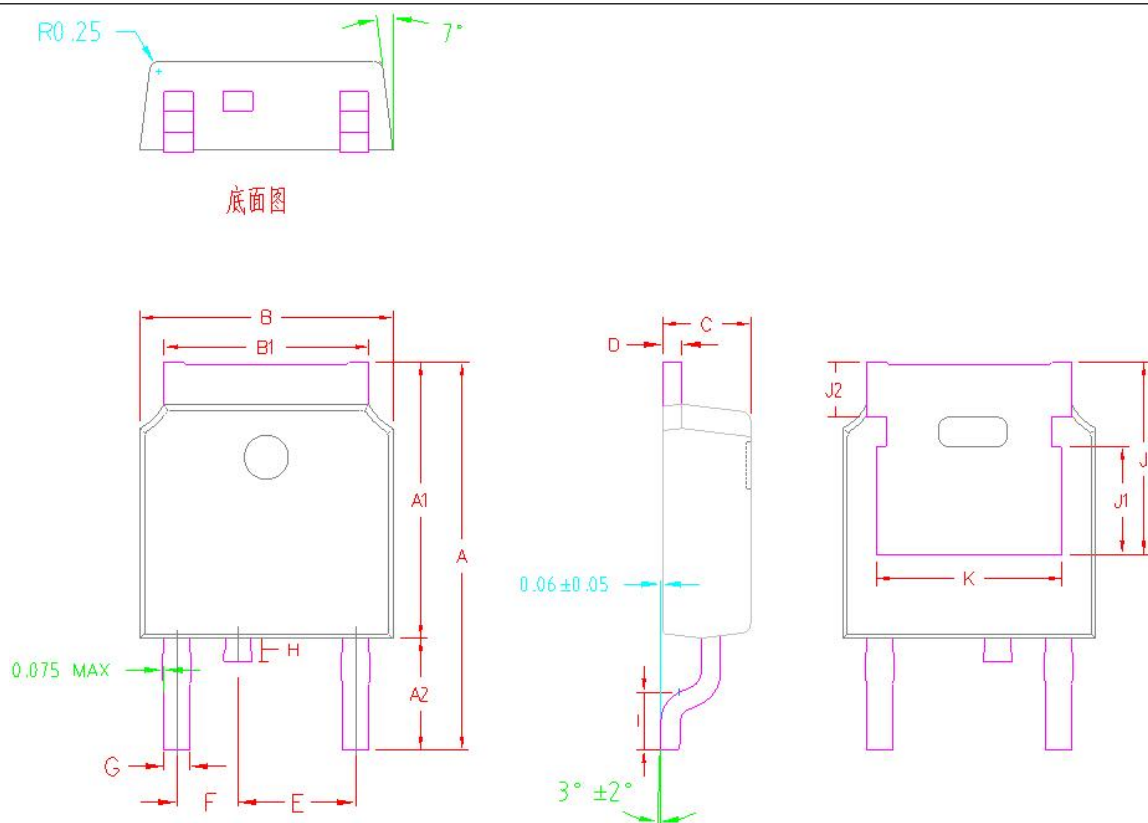
Symbol	Dimensions In Millimeters		
	Min	NOM	Max
A	4.85	4.90	4.95
B	5.70	5.75	5.80
C	6.00	6.02	6.10
D	3.00	3.10	3.20
E	1.27 BSC		
F	2.10	2.20	2.30
G	3.90	4.00	4.10
H	4.98	5.02	5.05
I	1.20	1.23	1.30
J	0.25	0.30	0.35
K	0.24	0.25	0.30
L	1.70	1.80	1.90
M	0.82	0.92	1.02
N	0.45	0.55	0.70
O	0.35	0.40	0.45

TO-220F



Symbol	mm		
	min	nom	max
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	2.50	2.65	2.80
C	0.40	0.50	0.60
E	9.95	10.15	10.35
H1	6.80REF		
D	15.60	15.90	16.20
G3	1.12	1.27	1.42
b1	1.15	1.25	1.35
b2	0.70	0.80	0.90
e	2.54BSC		
L	12.70	13.00	13.30
L1	2.75	2.85	3.05
P1	3.20	3.40	3.60
P2	2.90	3.10	3.30
P3	Diameter 1.5mm, depth of pogo pin hole 0.2mm		
P4	Diameter 0.8mm, depth of pogo pin hole 0.5mm		
F	3.15	3.30	3.45

TO252-4R



Symbol	mm		
	min	nom	max
A	9.90	10.10	10.30
A1	7.10	7.20	7.30
A2	2.80	2.90	3.10
B	6.50	6.60	6.70
B1	5.25	5.35	5.45
C	2.20	2.30	2.40
D	0.45	0.50	0.55
E	3.07(BSC)		
F	1.592(BSC)		
G	0.62	0.67	0.72
H	0.55	0.60	0.70
I	1.40	1.50	1.70
J	5.0(BSC)		
J1	2.70	2.80	2.90
J2	1.30	1.40	1.50
K	4.85(BSC)		