# Product Specification

Part Name: 3.12 inch PM OLED MODULE
ELEMENT TOUCH Part ID: TLEO25664E-Y

Ver: A

# Revision History

| Rev. | Date | Contents | Written | Approved |
|---|---|---|---|---|
| A | 2008/5/12 | Preliminary Specification | BIN | Zhang |
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Special Notes

| Note1. | |
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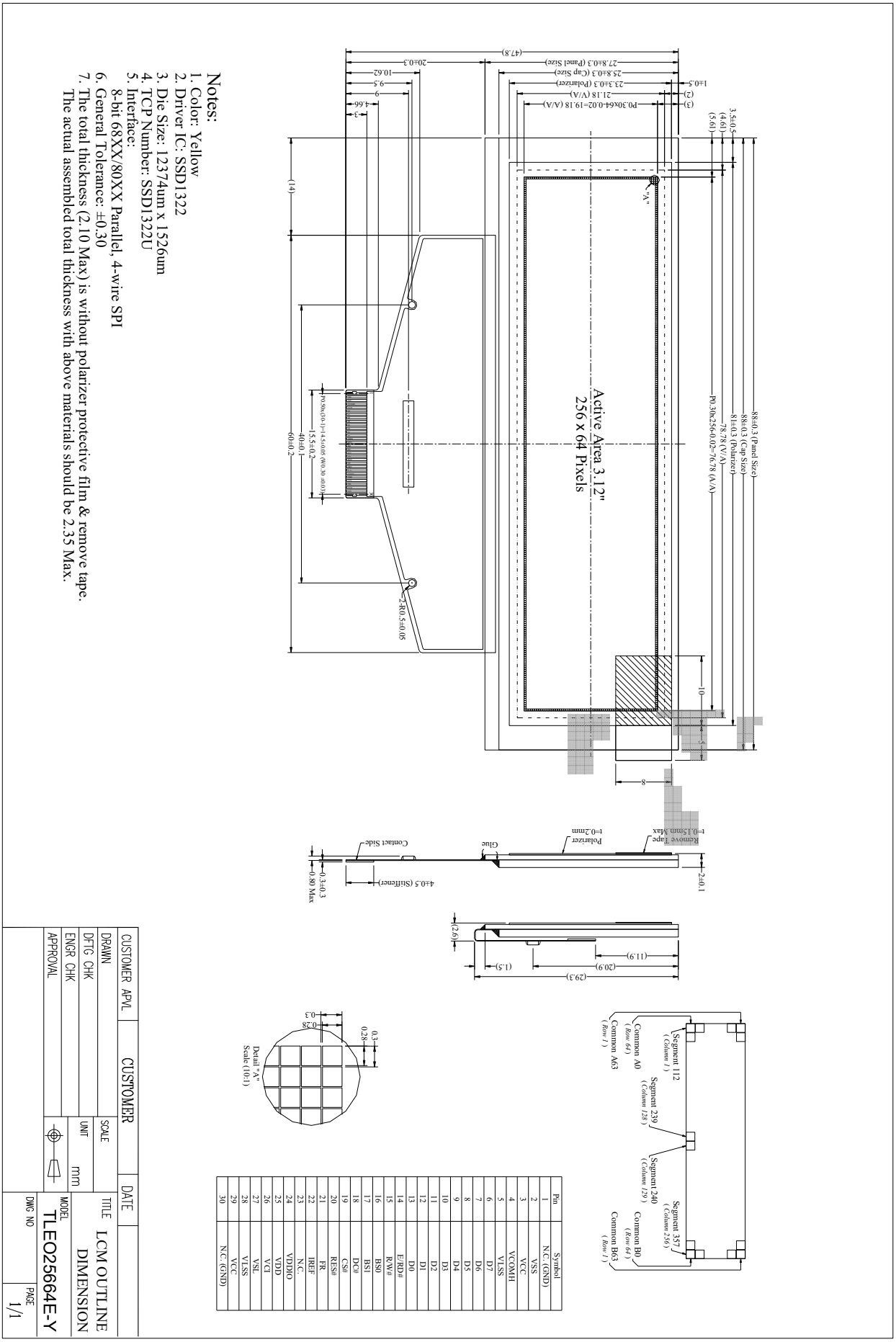
# Contents

## PHYSICAL DATA

| No. | Items | Specification | Unit |
|---|---|---|---|
| 1 | Display Mode | Passive Matrix OLED | - |
| 2 | Display Color | Monochrome (Yellow) | - |
| 3 | Duty | 1/64 | - |
| 4 | Resolution | 256 (H) x 64 (V) | Pixel |
| 5 | Active Area | 76.78 (W) x 19.18 (H) | mm |
| 6 | Outline Dimension | 88.00 (W) x 27.80 (H) x 2.00 (D) | mm |
| 7 | Pixel Pitch | 0.30 (W) x 0.30 (H) | mm |
| 8 | Pixel Size | 0.28 (W) x 0.28 (H) | mm |
| 9 | Driver IC | SSD1322 | - |
| 10 | Interface | 8-bit parallel,3-/4-wire SPI | - |
| 11 | Weight | 9.95 | g |

# EXTERNAL DIMENSIONS



## ABSOLUTE MAXIMUM RATINGS

| Items | Symbol | Min | Typ. | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage for logic | $V_{DD}$ | -0.5 | - | 2.75 | V | 1,2 |
| Supply voltage for operation | $V_{CI}$ | -0.3 | - | 4 | V | 1,2 |
| Supply voltage for I/O pins | $V_{DDIO}$ | -0.5 | - | $V_{CI}$ | V | 1,2 |
| Supply voltage for display | $V_{CC}$ | -0.5 | - | 16 | V | 1,2 |
| Operating current for $V_{CC}$ | $I_{CC}$ | - | - | 55 | mA | 1,2 |
| Operating temperature | $T_{OP}$ | -30 | - | 85 | ℃ | - |
| Storage temperature | $T_{ST}$ | -40 | - | 90 | ℃ | - |
| Life time(80cd/m² ) | - | 40,000 | - | - | hour | 3 |
| Humidity | - | - | - | 90 | %RH | - |

Note 1: All the above voltages are on the basis of "$V_{SS}$ = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur.Also,for normal operations,it is desirable to use this module under the conditions according to"electro-optical characteristics".If this module is used beyond these conditions,malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: $V_{CC}$ = 12.0V, $T_a$ = 25°C, 50% Checkerboard.
Software configuration follows Actual Application Example .
End of lifetime is specified as 50% of initial brightness reached.The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

# ELECTRICAL CHARACTERISTICS

## ◆DC Characteristics

| Items | Symbol | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage for logic | $V_{DD}$ | | 2.4 | 2.5 | 2.6 | V |
| Supply voltage for display | $V_{CC}$ | Note 4 | 11.5 | 12 | 12.5 | V |
| Supply voltage for operation | $V_{CI}$ | | 2.4 | 2.8 | 3.5 | V |
| Supply voltage for I/O pins | $V_{DDIO}$ | | 1.65 | 1.8 | $V_{CI}$ | V |
| High level input | $V_{IH}$ | | 0.8 $V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low level input | $V_{IL}$ | | 0 | - | 0.2 $V_{DDIO}$ | V |
| High level output | $V_{OH}$ | $I_{OUT}$ = 100μA, 3.3MH | 0.9 $V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low level output | $V_{OL}$ | $I_{OUT}$ = 100μA, 3.3MH | 0 | - | 0.1 $V_{DDIO}$ | V |
| Operating current for $V_{CI}$ | $I_{CI}$ | Note 5 | - | 1.8 | 2.25 | mA |
| | | Note 6 | - | 1.8 | 2.25 | mA |
| Operating current for $V_{CC}$ | $I_{CC}$ | Note 5 | - | 26.3 | 32.9 | mA |
| | | Note 6 | - | 41.1 | 51.4 | mA |
| Sleep mode current for $V_{CI}$ | $I_{CI,SLEEP}$ | | - | 1 | 5 | μA |
| Sleep mode current for $V_{CC}$ | $I_{CC,SLEEP}$ | | - | 1 | 5 | μA |

Note 4: Supply Voltage for Display ($V_{CC}$) are subject to the change of the panel characteristics and the customer's request.

Note 5: $V_{CI}$ = 2.8V, $V_{CC}$= 12V, 50% Display Area Turn on.

Note 6: $V_{CI}$ = 2.8V, $V_{CC}$= 12V, 100% Display Area Turn on.

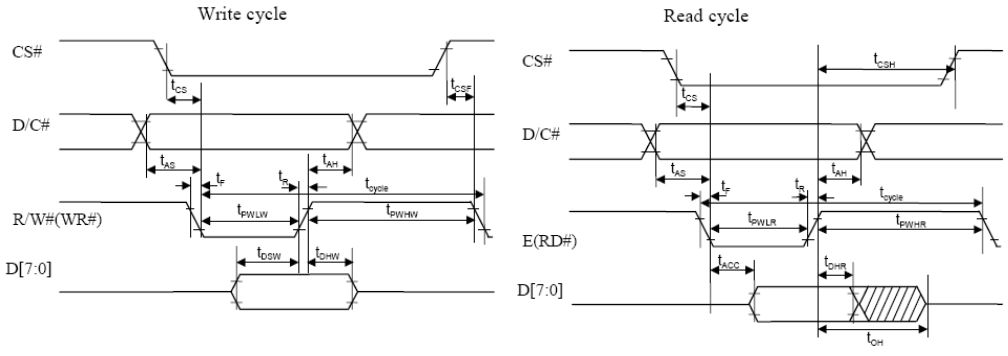
* Software configuration follows Actual Application Example .

# ε AC Characteristics

1. 80XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | ns |
| $t_{AS}$ | Address Setup Time | 10 | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 7 | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $t_{PWLR}$ | Read Low Time | 150 | - | ns |
| $t_{PWLW}$ | Write Low Time | 60 | - | ns |
| $t_{PWHR}$ | Read High Time | 60 | - | ns |
| $t_{PWHW}$ | Write High Time | 60 | - | ns |
| $t_{CS}$ | Chip Select Setup Time | 0 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time to Read Signal | 0 | - | ns |
| $t_{CSF}$ | Chip Select Hold Time | 20 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

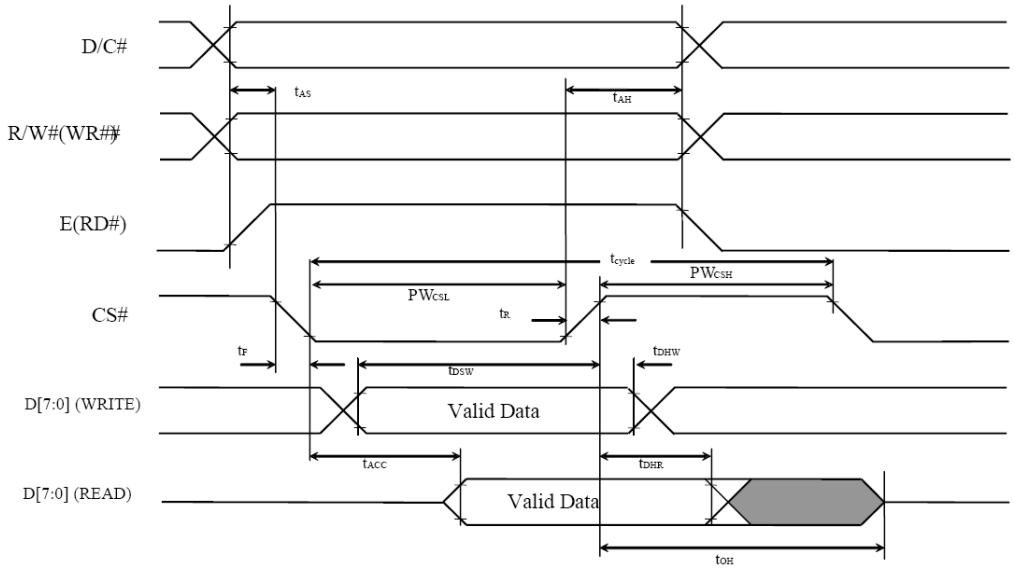
* ($V_{DD}$ - $V_{SS}$ = 2.4V to 2.6V, $V_{DDIO}$ = 1.6V, $V_{CI}$ = 2.8V, $T_a$ = 25°C)



2. 68XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 300 | - | ns |
| $t_{AS}$ | Address Setup Time | 10 | - | ns |
| $t_{AH}$ | Address Hold Time | 0 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 7 | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (Read) | 120 | - | ns |
| | Chip Select Low Pulse Width (Write) | 60 | | |
| $PW_{CSH}$ | Chip Select High Pulse Width (Read) | 60 | - | ns |
| | Chip Select High Pulse Width (Write) | 60 | | |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

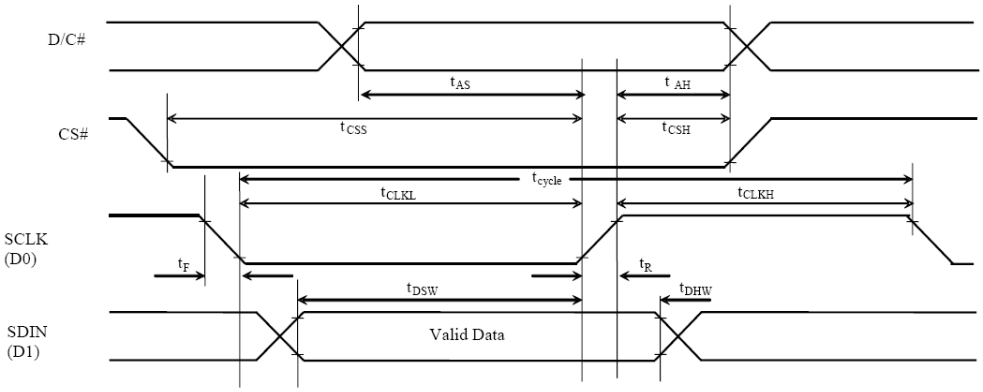
* ($V_{DD}$ - $V_{SS}$ = 2.4V to 2.6V, $V_{DDIO}$ = 1.6V, $V_{CI}$ = 2.8V, $T_a$ = 25°C)

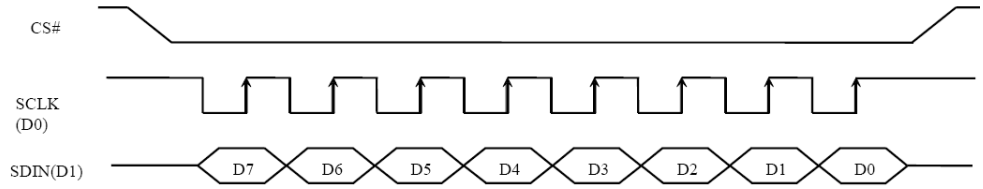


3. Serial Interface Timing Characteristics: (4-wire SPI)

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | ns |
| $t_{AS}$ | Address Setup Time | 15 | - | ns |
| $t_{AH}$ | Address Hold Time | 15 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 20 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 10 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 15 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | ns |
| $t_{CLKL}$ | Clock Low Time | 20 | - | ns |
| $t_{CLKH}$ | Clock High Time | 20 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

* ($V_{DD}$ - $V_{SS}$ = 2.4V to 2.6V, $V_{DDIO}$ = 1.6V, $V_{CI}$ = 2.8V, $T_a$ = 25°C)

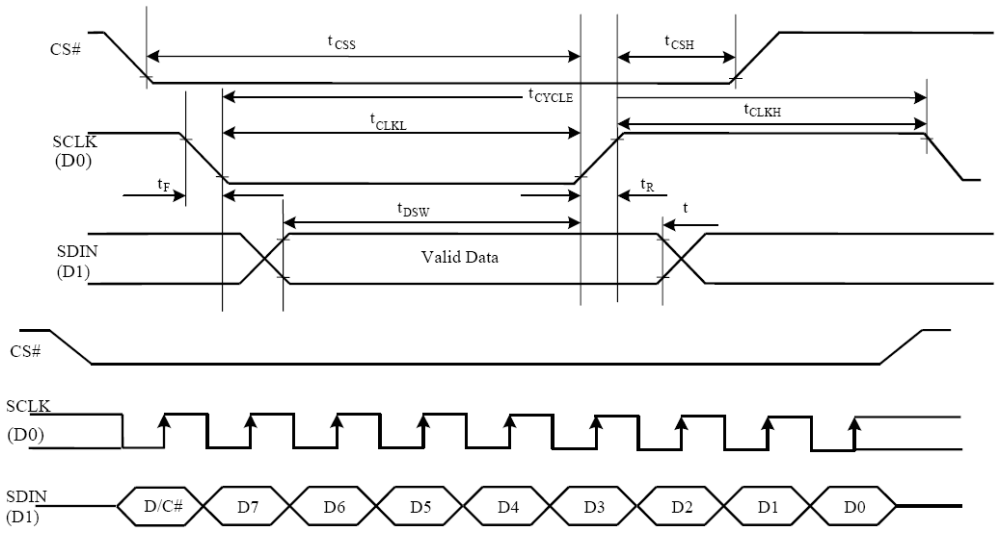


4. Serial Interface Timing Characteristics: (3-wire SPI)

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | ns |
| $t_{AS}$ | Address Setup Time | 15 | - | ns |
| $t_{AH}$ | Address Hold Time | 15 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 20 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 10 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 15 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | ns |
| $t_{CLKL}$ | Clock Low Time | 20 | - | ns |
| $t_{CLKH}$ | Clock High Time | 20 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

* ($V_{DD}$ - $V_{SS}$ = 2.4V to 2.6V, $V_{DDIO}$ = 1.6V, $V_{CI}$ = 2.8V, $T_a$ = 25°C)



# TIMING OF POWER SUPPLY

## 1. Commands

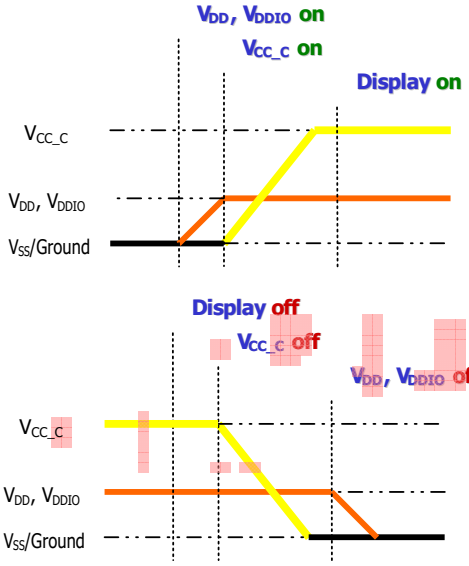
Refer to the Technical Manual for the SSD1322

## 2. Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

1.2.1 Power up Sequence:

1. Power up $V_{DD}$ & $V_{DDIO}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up $V_{CC\_C}$
6. Delay 100ms
   (When $V_{CC\_C}$ is stable)
7. Send Display on command




1.2.2 Power down Sequence:

1. Send Display off command
2. Power down $V_{CC\_C}$
3. Delay 100ms
   (When $V_{CC\_C}$ is reach 0 and panel is completely discharges)
4. Power down $V_{DD}$ & $V_{DDIO}$

Note 8:

1) Since an ESD protection circuit is connected between $V_{DD}$, $V_{DDIO}$ and $V_{CC\_C}$ inside the driver IC, $V_{CC\_C}$ becomes lower than $V_{DD}$ & $V_{DDIO}$ whenever $V_{DD}$ & $V_{DDIO}$ is ON and $V_{CC\_C}$ is OFF.
2) $V_{CC\_C}$ should be kept float (disable) when it is OFF.
3) Power Pins ($V_{DD}$, $V_{DDIO}$, $V_{CC\_C}$) can never be pulled to ground under any circumstance.
4) $V_{DD}$ & $V_{DDIO}$ should not be power down before $V_{CC\_C}$ power down.

## 3. Reset Circuit

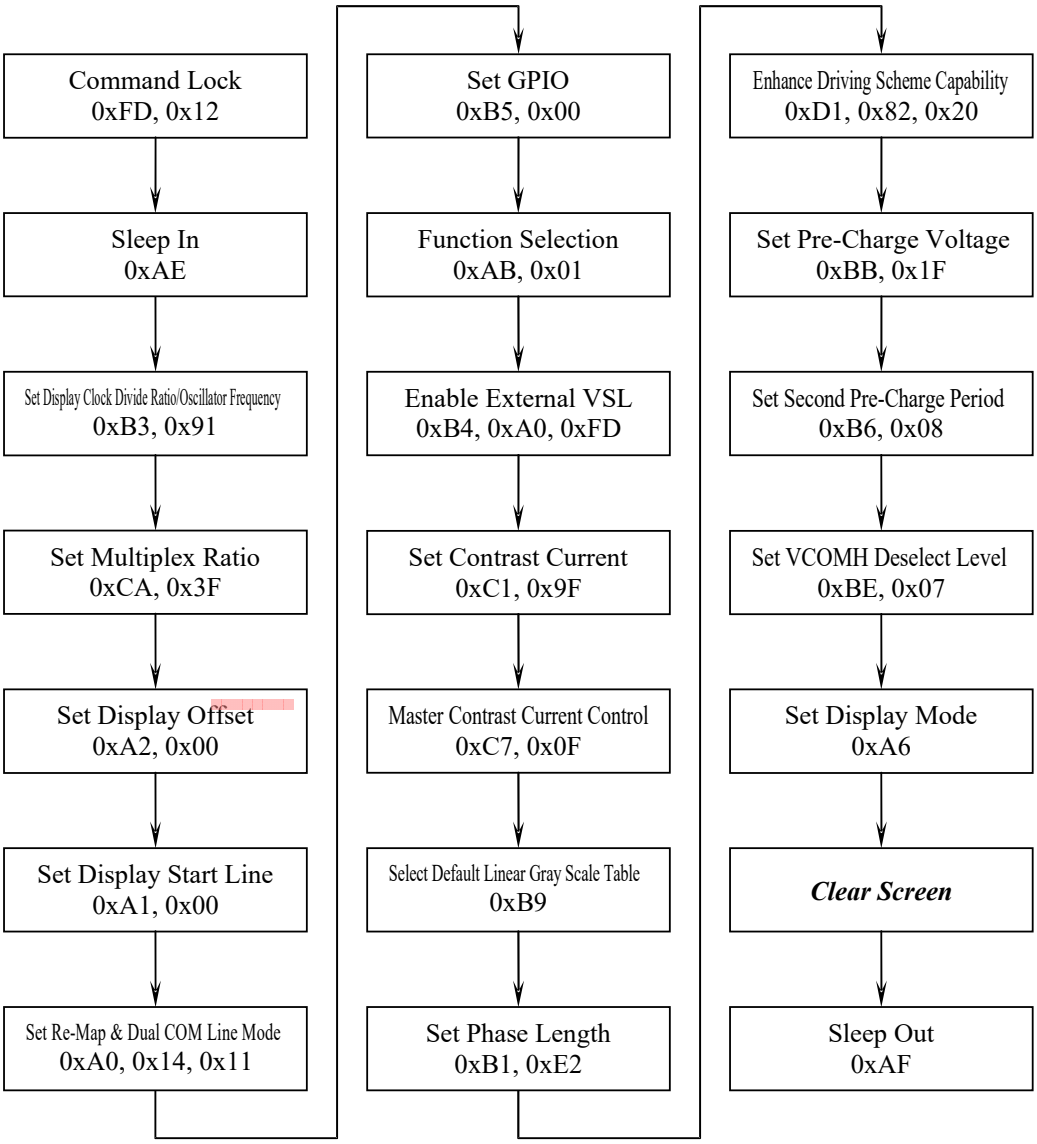
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 480· 128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

## 4. Actual Application Example

Command usage and explanation of an actual example

<Initialization>




If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

## ■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

| Items | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Operating Luminance | | L | 60 | 80 | - | cd /m$^2$ | Yellow |
| Power Consumption | | P | - | - | - | mW | 30% pixels ON<br>L=110cd/m$^2$ |
| Frame Frequency | | Fr | - | - | - | Hz | |
| Color Coordinate | Yellow | CIE x | 0.44 | 0.48 | 0.52 | CIE1931 | Darkroom |
| | | CIE y | 0.46 | 0.50 | 0.54 | | |
| Response Time | Rise | Tr | - | - | - | ms | - |
| | Decay | Td | - | - | - | ms | - |
| Contrast Ratio* | | Cr | 20000 :1 | - | - | | Darkroom |
| Viewing Angle Uniformity | | △ θ | 160 | - | - | Degree | - |

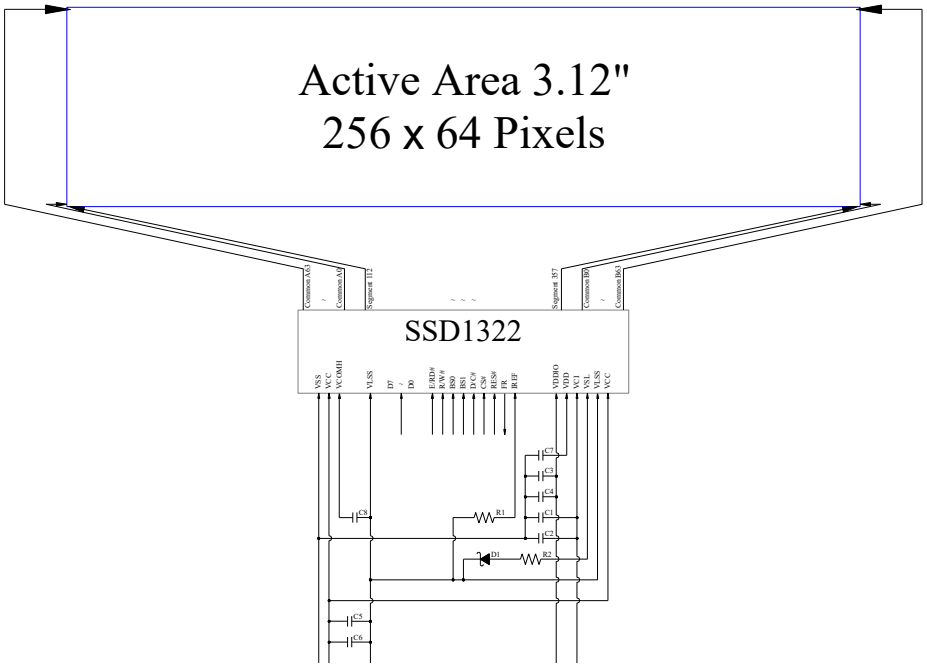
Note : Brightness ($L_{br}$) is subject to the change of the panel characteristics and the customer's request.

* Optical measurement taken at $V_{DD}$ = 2.8V, $V_{CC}$= 12V.

Software configuration follows Actual Application Example .

# INTERFACE PIN CONNECTIONS

### 1. Block Diagram




MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1
C2, C4: 4.7µF
C6: 10µF
C7: 1µF
C8: 4.7uF / 25V Tantalum Capacitor
R1: 680kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

## 2. Pin Definition

| Pin Number | Symbol | Type | Function |
|---|---|---|---|
| **Power Supply** | | | |
| 26 | VCI | P | *Power Supply for Operation*<br>This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO. |
| 25 | VDD | P | *Power Supply for Core Logic Circuit*<br>This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances. |
| 24 | VDDIO | P | *Power Supply for I/O Pin*<br>This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO. |
| 2 | VSS | P | *Ground of Logic Circuit*<br>This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground. |
| 3, 29 | VCC | P | *Power Supply for OEL Pan l*<br>These are the most positive voltage supply pin of the chip. They must be connected to external source. |
| 5, 28 | VLSS | P | *Ground of Analog Circuit*<br>These are the analog ground pins. They should be connected to VSS externally. |
| **Driver** | | | |
| 22 | IREF | I | *Current Reference for Brightness Adjustment*<br>This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA. |
| 4 | VCOMH | P | *Voltage Output High Level for COM Signal*<br>This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS. |
| 27 | VSL | P | *Voltage Output Low Level for SEG Signal*<br>This is segment voltage reference pin.<br>When external VSL is not used, this pin should be left open.<br>When external VSL is used, this pin should connect with resistor and diode to ground. |
| **Testing Pads** | | | |
| 21 | FR | O | *Frame Frequency Triggering Signal*<br>This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually. |

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>16<br>17</td><td>BS0<br>BS1</td><td>I</td><td>Communicating Protocol Select<br>These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>BS0</td><td>BS1</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>20</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver<br>This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select<br>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>D/C#</td><td>I</td><td>Data/Command Control<br>This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>14</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.<br>When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.<br>When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.<br>When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.<br>When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>6~13</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus<br>These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.<br>Unused pins must be connected to VSS except for D2 in serial mode.</td></tr>
</table>

| Pin Number | Symbol | I/O | Function |
|---|---|---|---|
| **Reserve** | | | |
| 23 | N.C. | - | *Reserved Pin*<br>The N.C. pin between function pins are reserved for compatible and flexible design. |
| 1, 30 | N.C. (GND) | - | *Reserved Pin (Supporting Pin)*<br>The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground. |

## RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage<br>(HTS)</td><td>90±2K , 500 hours</td><td rowspan="6">1. After testing, the function test is ok.<br>2. After testing, no addition to the defect.<br>3. After testing, the change of luminance should be within +/- 50% of initial value.<br>4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.<br>5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating<br>(HTO)</td><td>85±2K , 500 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage<br>(LTS)</td><td>-40±2K , 500 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating<br>(LTO)</td><td>-30±2K , 500 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage<br>(HTHHS)</td><td>60±3K , 90%±3%RH, 500 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation)<br>(TS)</td><td>-40±2K ~ 25K ~ 85±2K<br>(30min) (5min) (30min)<br>100cycles</td></tr>
<tr><td>Vibration (Packing)</td><td>10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z</td><td colspan="2" rowspan="2">1. One box for each test.<br>2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop (Packing)</td><td>Height : 1 m, each time for 6 sides, 3 edges, 1 angle</td></tr>
</table>

Note+ 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance ° 10MΩ).

# OUTGOING QUALITY CONTROL SPECIFICATION

## Standard

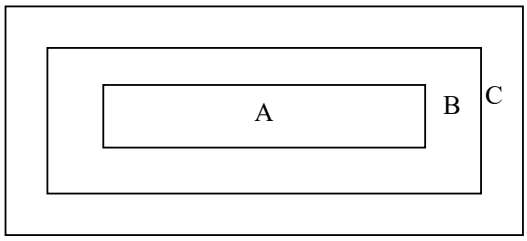
According to GB/T2828.1-2003/ISO 2859-1 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

## Definition

1 Major defect : The defect that greatly affect the usability of product.

2 Minor defect : The other defects, such as cosmetic defects, etc.

3 Definition of inspection zone:




Zone A: Active Area

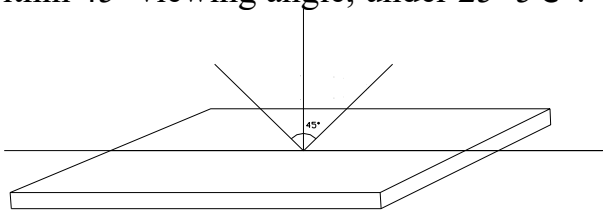
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

## Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃ .



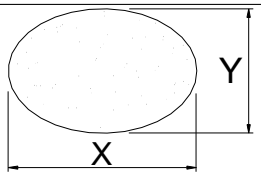
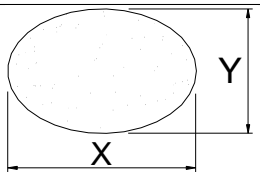

2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃ .

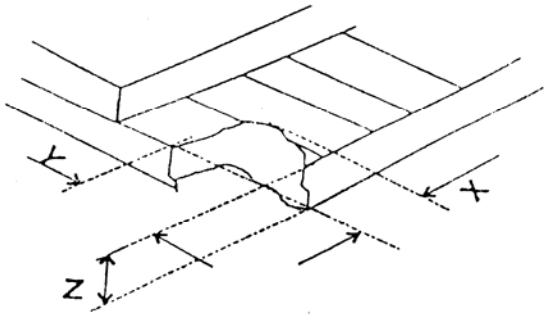
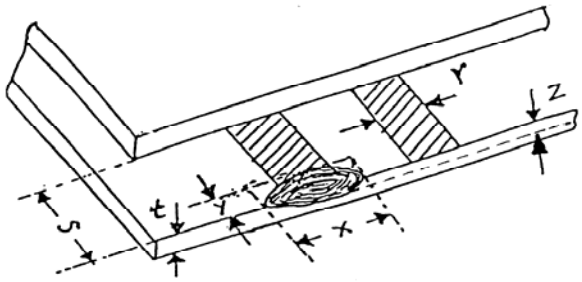
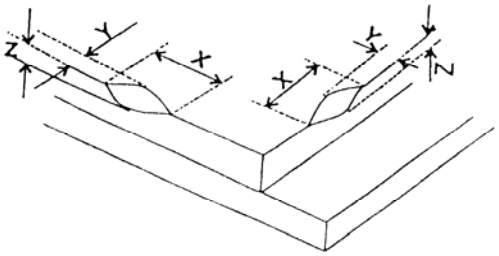
## Inspection Criteria

1 Major defect : AQL= 0.65

| Item | Criterion |
|---|---|
| Function Defect | 1. No display or abnormal display is not accepted |
| | 2. Open or short is not accepted. |
| | 3. Power consumption exceeding the spec is not accepted. |
| Outline Dimension | Outline dimension exceeding the spec is not accepted. |
| Glass Crack | Glass crack tends to enlarge is not accepted. |

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>≤ 0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10 < ≤ 0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15 < ≤ 0. 20</td><td>1</td></tr>
<tr><td>0.20 <</td><td>0</td></tr>
<tr><td colspan="4">Note : = ( x + y ) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L ( Length ) : mm</td><td>W ( Width ) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W ≤ 0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L ≥ 3.0</td><td>0.03 < W ≤ 0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L ≥ 2.0</td><td>0.05 < W ≤ 0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08 < W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L ( Length ) : mm</td><td>W ( Width ) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W ≤ 0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0 < L ≤ 10.0</td><td>0.03 < W ≤ 0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L ≤ 5.0</td><td>0.05 < W ≤ 0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08 < W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>≤ 0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20 < ≤ 0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50 < ≤ 0.80</td><td>1</td></tr>
<tr><td>0.80 <</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped )</td><td>1. On the corner<br>(mm)<br>  <br><br><table><tr><td>x</td><td>≦ 2.0</td></tr><tr><td>y</td><td>≦ S</td></tr><tr><td>z</td><td>≦ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge<br>(mm)<br>  <br><br><table><tr><td>x</td><td>≦ a / 2</td></tr><tr><td>y</td><td>≦ s / 3</td></tr><tr><td>z</td><td>≦ t</td></tr></table></td></tr>
<tr><td>3. On the other edges<br>(mm)<br>  <br><br><table><tr><td>x</td><td>≦ a / 5</td></tr><tr><td>y</td><td>≦ 1.0</td></tr><tr><td>z</td><td>≦ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

# CAUTIONS IN USING OLED MODULE

## Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD}$ → $V_{PP}$, and power off sequence: $V_{PP}$ → $V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13.When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

## Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C r 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

## Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0 °C and 30 °C , the relative humidity not over 60%.

## Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.