0.65W, 5kV$_{RMS}$ Complete Isolated DC-DC Converter

1 Features

- **Complete Switch Mode Power Supply**
  - High integration with internal transformer
  - Soft-start reduces input inrush current and output overshoot
  - Overload and short-circuit protection
  - Thermal shutdown
- **4.5 V to 5.5 V Input Voltage Range**
- **Selectable Output voltages**
  - 3.3V, 3.7V, 5V and 5.4V output options
- **Delivers up to 650mW(5V/130mA) Output Power**
- **Robust Galvanic Isolation Barrier**
  - High lifetime: > 40 years
  - Up to 5000 V_{RMS} isolation rating
  - ±150 kV/μs typical CMTI
- **Wide Operating Temperature Range: -40°C to 125°C**
- **Low Profile SOIC16-WB (10.30mm × 7.50) Package**
- **Safety-Related Certifications (Pending)**
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577
  - 7071V$_{PK}$ V_{IOTM} and 849V$_{PK}$ V_{IORM} reinforced isolation per DIN V VDE V 0884-11:2017-01
  - IEC 60950、 IEC 60601 and EN 61010 certifications per CQC, TUV and CSA

2 Applications

- Instruments and Apparatuses
- Industrial automation
- Motor Control
- Medical Equipment
- Industrial Sensors
- Telecom Equipment

3 General Description

The CA-IS3105 is a complete isolated DC-DC converter with up to 5kV$_{RMS}$ isolation rating. This device integrates most of the components needed for an isolated power supply — switching controller, power switches, transformer, soft-start, protection circuit etc. — into a single, compact SOIC package. The result is an efficient and compact fully integrated solution that is easy to comply with EMI requirements and makes power-supply design as easy as possible. Operating over an input voltage range of 4.5V to 5.5V, the CA-IS3105 provides a fixed output voltage of 3.3V, 3.7V, 5V or 5.4V set by pin SEL. Only output, input bypass capacitors, and a pull-up resistor (3.7V or 5.4V output) are needed to finish the design.

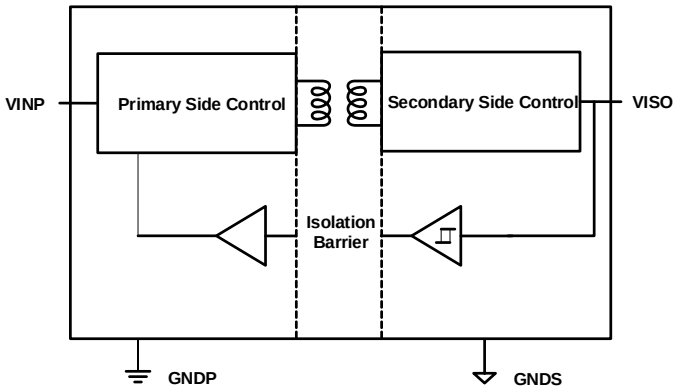
The CA-IS3105 features a unique control scheme, which can quickly respond to load transient and accurately regulate the output voltage. The device is capable of delivering a load up to 650mW output power and offering soft-start, current limit, short-circuit and thermal shutdown protection features to better enhance the reliability of the system. The CA-IS3105 includes an enable input pin (EN). Connect the EN pin to the VINP input voltage pin or force this pin high to turn on the DC-DC converter. Force this pin low to disable the device and enter shutdown mode. In shutdown mode, the device stops switching operation with microampere standby supply current.

The CA-IS3105 is available in wide-body SOIC16 package and operates over -40°C to +125°C temperature range.

Device Information

Part number	Package	Package size (NOM)
CA-IS3105W	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Block Diagram



4 Ordering Information

Table 4-1. Ordering Information

Part #	Input Voltage	Output Voltage	Output Power	Package
CA-IS3105W	4.5V to 5.5V	3.3V, 3.7V, 5V, 5.4V	650mW	SOIC16-WB(W)

Table of Contents

5 Revision history

Revision Number	Description	Page Changed	Revision Date
Version 1.00	N/A	N/A	2022-03-22

6 Pin Configuration and Description

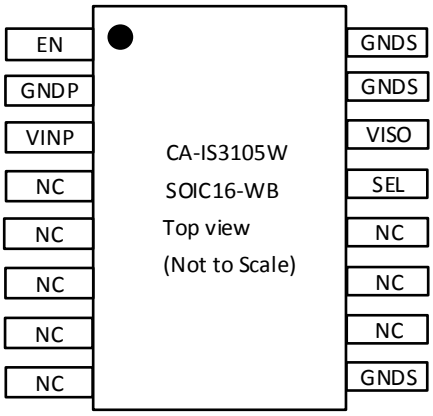


Figure 6-1 CA-IS3105W Top View

Table. 6-1 CA-IS3105W Pin Description

Pin name	Pin number	Type	Description
EN	1	Input	Enable Input Pin, active-high. Force this pin high to enable the device. Force this pin low to disable the device and enter shutdown mode.
GNDP	2	GND	Primary side local ground.
VINP	3	Power	Primary side supply input. Bypass VINP to GNDP with both 0.1µF and 10µF capacitors as close to the device as possible.
NC[1]	4, 5, 6, 7, 8	-	No internal connection. These pins belong to primary side voltage domain. Connect them to GNDP externally.
GNDS	9, 15, 16	GND	Secondary side ground return connection for V_{ISO}.
NC[1]	10, 11, 12	-	No internal connection. These pins belong to isolated voltage domain. Connect them to GNDS externally.
SEL	13	Input	Output voltage V_{ISO} select pin: V_{ISO} = 5.0 V when SEL is shorted to VISO; V_{ISO} = 5.4 V when SEL is connected to VISO through a 100kΩ resistor; V_{ISO} = 3.3 V when SEL is shorted to GNDS; V_{ISO} = 3.7V when SEL is connected to GNDS through a 100kΩ resistor. Don't leave this pin open.
VISO	14	Power	Isolated supply voltage pin. Bypass VISO to GNDS with both 0.1µF and 10µF capacitors as close to the device as possible.

Note:

1. These pins do not have internal connection. We recommend to connect them to the corresponding ground plane to improve the PCB heat dissipation.

7 Specifications

7.1 Absolute Maximum Ratings[1, 2]

Parameters		Minimum value	Maximum value	Unit
V_{INP}	Power supply voltage	-0.5	6.0	V
V_{ISO}	Isolated supply voltage	-0.5	6.0	V
EN	EN input voltage	-0.5	V_{INP}+0.3[3]	V
SEL	SEL input voltage	-0.5	V_{ISO}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

Notes:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
2. All voltage values are with respect to the local ground (GNDP or GNDS) and are peak voltage values.
3. Maximum voltage must not be exceed 6 V.

7.2 ESD Ratings

		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins[2]	±2000	

Notes:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
2. Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

7.3 Recommended Operating Conditions

Parameters		Minimum value	Typical value	Maximum value	Unit
V_{INP}	Power supply voltage	4.5	5	5.5	V
V_{EN}	EN input voltage	0		5.5	V
V_{ISO}	Isolated supply voltage	0		5.7	V
V_{SEL}	SEL input voltage	0		5.7	V
T_A	Ambient Temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

7.4 Thermal Information

Thermal Metric		CA-IS3105W SOIC16-WB(W)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.8	°C/W

7.5 Power Ratings

Parameters		Test Conditions	Minimum value	Typical value	Maximum value	Unit
P_D	Power dissipation	V_{INP} = 5.5V, V_{ISO} = 5.4V, 130mA output current		1.27W	1.4	W

7.6 Insulation Specifications

Parameters		Test Conditions	Specifications W	Unit
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)； IEC 60112	>400	V
	Material group	According to IEC 60664-1	I	
	IEC 60664-1 over-voltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[1]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	600	V_{RMS}
		DC voltage	849	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	6250	V_{PK}
q_{pd}	Apparent charge[3]	Method a, after input/output safety tests subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b1, at routine test (100% production test) and preconditioning (sample test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	3.5	pF
R_{IO}	Isolation resistance , input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (certified) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7 Safety-Related Certifications

VDE (pending)	UL (pending)	CQC (pending)	TUV (pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-20111	Certified according to EN61010-1:2010 (3rd Ed) and EN60950-1:2006/A2:2013

7.8 Electrical Characteristics

Over operating temperature range T_A = -40 to 125°C, V_{INP} = 4.5V to 5.5V, SEL connected to V_{ISO}, C_{VINP} = C_{VISO} = 10µF, unless otherwise specified. All typical specs are at T_A = 25°C and V_{INP} = 5V.

Parameters		Test Conditions	Minimum value	TYP	Maximum value	Unit
Power Supply Input						
I_{VINP_SD}	V_{INP} shutdown current	EN = LOW, see Figure 7- 27		0.05	10	µA
I_{VINP_O}	V_{INP} quiescent current I_{OUT} = 0% load	EN = HIGH, SEL connected to V_{ISO} (5V output), see Figure7- 28		8.4	20	mA
		EN = HIGH, SEL 100kΩ to VISO (5.4Voutput)		8.8	20	mA
		EN = HIGH, SEL connected to GNDS (3.3V output)		7.3	20	mA
		EN = HIGH, SEL 100kΩ to GNDS (3.7V output)		7.5	20	mA
I_{VINP_SC}	DC current from VINP supply under short circuit on VISO	VISO short to GNDS		42	100	mA
V_{UVLO+}	Input undervoltage lockout rising threshold			2.6	3.0	V
V_{UVLO-}	Input undervoltage lockout falling threshold		2.1	2.3		V
$V_{HYS(UVLO)}$	Input undervoltage lockout hysteresis			0.3	0.6	V
EN, SEL pins						
V_{IH_EN}	EN Input threshold, logic HIGH		2			V
V_{IL_EN}	EN Input threshold, logic LOW				0.8	V
I_{EN}	Input leakage current	V_{INP} = 5V, V_{EN} = 5V		5	20	µA
Isolated DC-DC Converter						
V_{ISO}	Isolated output voltage	SEL connected to V_{ISO} (5V output), I_{ISO} = 50mA	4.65	5.0	5.35	V
		SEL 100KΩ to VISO (5.4V output), I_{ISO} = 50mA	5.02	5.4	5.78	
		SEL connected to GNDS (3.3V output), I_{ISO} = 50mA	3.07	3.3	3.53	
		SEL 100KΩ to GNDS (3.7V output), I_{ISO} = 50mA	3.44	3.7	3.96	
$VISO_{(RIP)}$	Voltage ripple on isolated supply output (pk-pk)	20MHz bandwidth, SEL short to VISO (5V output), I_{ISO} = 100mA, see Figure 7- 9		65	100	mV
		20MHz bandwidth, SEL short to GNDS (3.3V output), I_{ISO} = 100mA, see Figure 7- 11		55	100	
$VISO_{(LINE)}$	Line regulation	SEL short to VISO (5V output), I_{ISO} = 50mA, V_{INP} = 4.5V to 5.5 V, see Figure7- 21		2	5	mV/V
		SEL short to GNDS (3.3V output), I_{ISO} = 50mA, V_{INP} = 4.5V to 5.5V, see Figure7- 23		2	5	
$VISO_{(LOAD)}$	Load regulation	SEL short to VISO (5V output), I_{ISO} = 0 to 130mA, see Figure7- 17		1%	2%	
		SEL short to GNDS (3.3V output), I_{ISO} = 0 to 130mA, see Figure7- 19		1%	2%	
EFF	Efficiency@maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1µF || 10µF; V_{ISO}=5V, see Figure7- 25, Figure7- 26		55%		
		I_{ISO} = 130mA, C_{LOAD} = 0.1µF || 10µF; V_{ISO}=3.3V, see Figure7- 25, Figure7- 26		48%		
CMTI	Common-mode transient immunity	Slew Rate of GNDP versus GNDS, V_{CM}=1200V_{RMS}	±100	±150		kV/µs
V_{ISO} ripple voltage (peak to peak)		10% to 90% load step with 10mA/us slew-rate; see Figure7- 13, Figure7- 14, Figure7- 15, Figure7- 16		80	100	mV
Transient Output Power (overload)		V_{INP} = 5V, V_{ISO} = 5.4V	1			W

7.9 MSL

Parameters	Standard	Level
MSL	IPC/JEDEC J-STD-020D.1	MSL 3

7.10 Typical Operating Characteristics

7.10.1 Soft-Start and Output Short-Circuit Protection

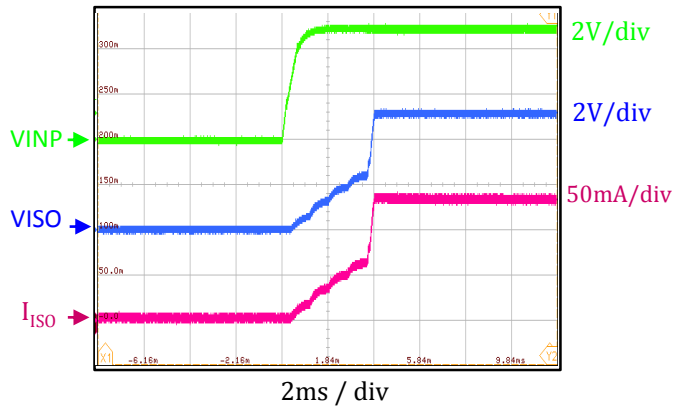


Figure7- 1 Soft start at I_{ISO} = 130mA, V_{INP} = 5V, V_{ISO} = 5V

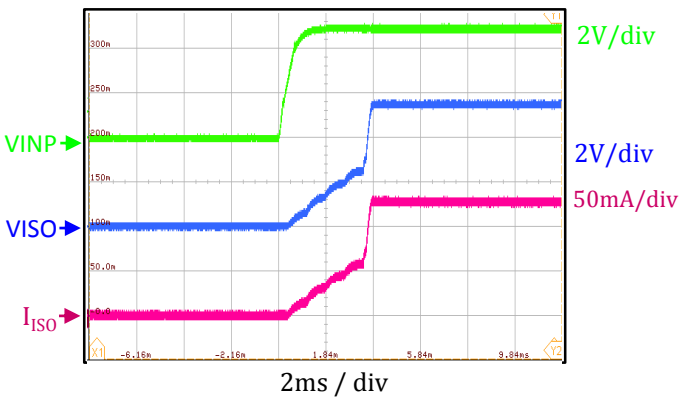


Figure 7- 2 Soft start at I_{ISO} = 130mA, V_{INP} = 5V, V_{ISO} = 5.4V

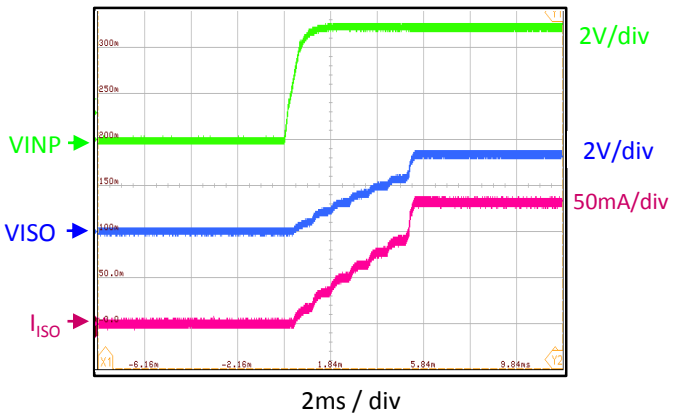


Figure7- 3 Soft start at I_{ISO} = 130mA, V_{INP} = 5V, V_{ISO} = 3.3V

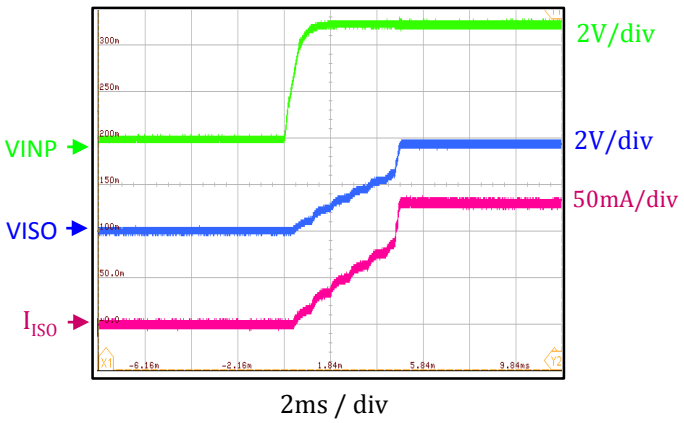


Figure7- 4 Soft start at I_{ISO} = 130mA, V_{INP} = 5V, V_{ISO} = 3.7V

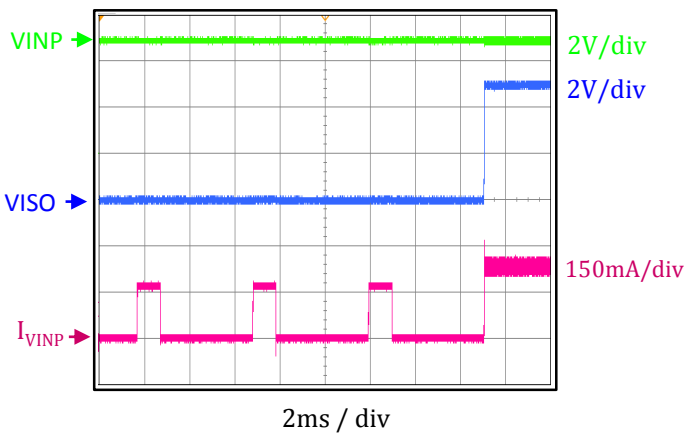


Figure7- 5 V_{INP} = 5V, V_{ISO} = 5V, output short to GNDS and recover to I_{ISO} = 130mA

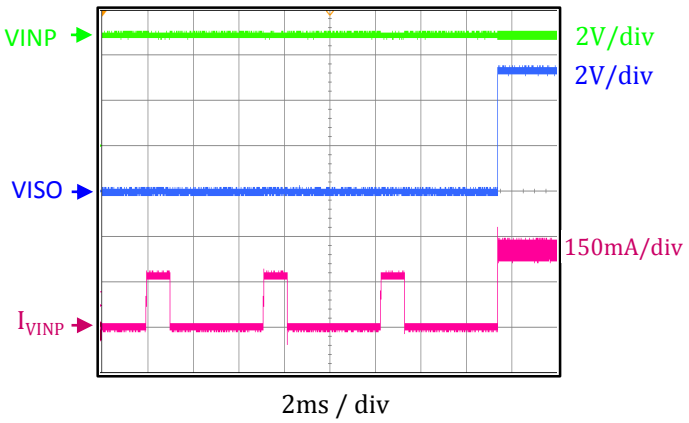


Figure7- 6 Startup at V_{INP} = 5V, V_{ISO} = 5.4V, output short to GNDS and recover to I_{ISO} = 130mA

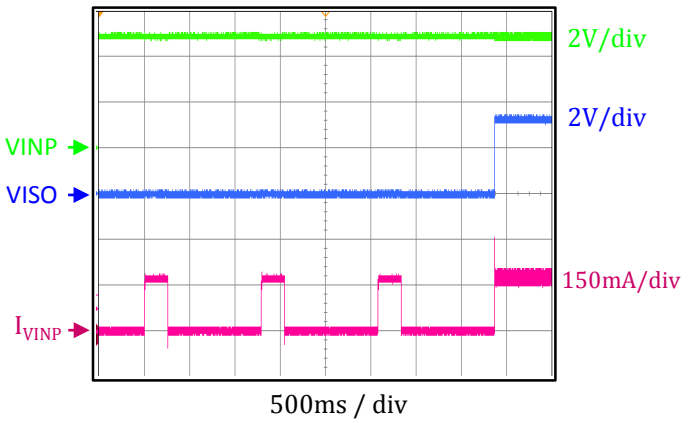


Figure 7- 7 V_{INP} = 5V, V_{ISO} = 3.3V, output short to GNDS and recover to I_{ISO} = 130mA

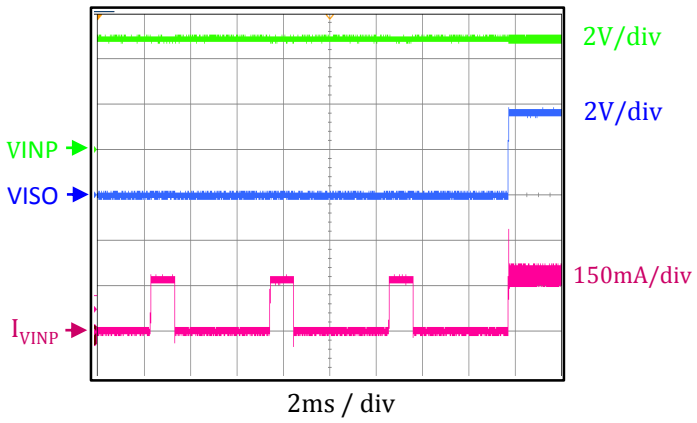


Figure 7- 8 V_{INP} = 5V, V_{ISO} = 3.7V, output short to GNDS and recover to I_{ISO} = 130mA

7.10.2 V_{ISO} Ripple and Load Transient Response

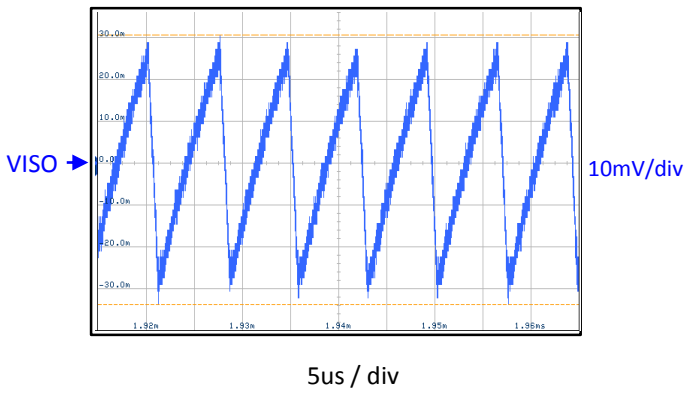


Figure 7- 9 V_{INP} = 5V, V_{ISO} = 5V, I_{ISO} = 130mA

V_{ISO} ripple voltage(peak to peak) : 64mV

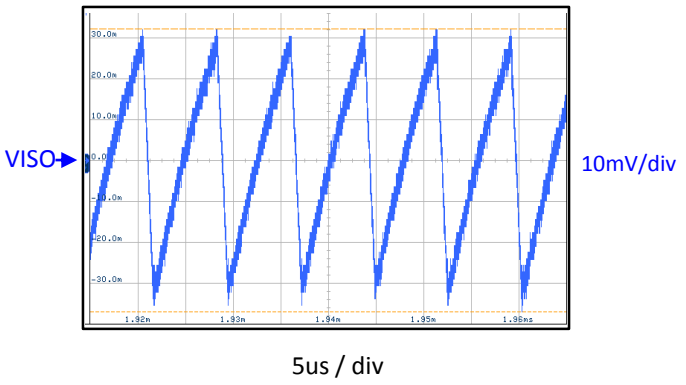


Figure7- 10 V_{INP} = 5V, V_{ISO} = 5.4V, I_{ISO} = 130mA

V_{ISO} ripple voltage(peak to peak) :69mV

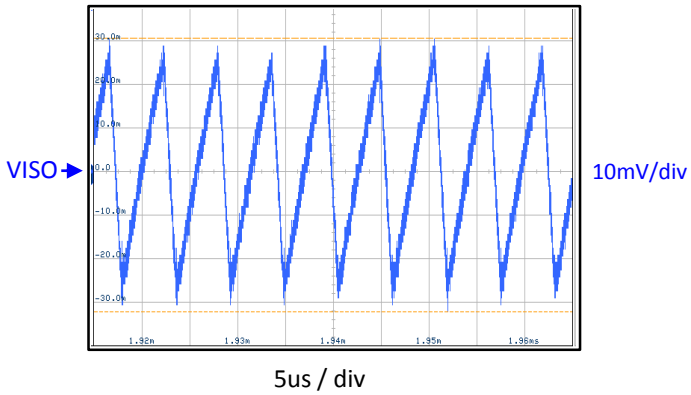


Figure 7- 11 V_{INP} = 5V, V_{ISO} = 3.3V, I_{ISO} = 130mA

V_{ISO} ripple voltage(peak to peak): 63mV

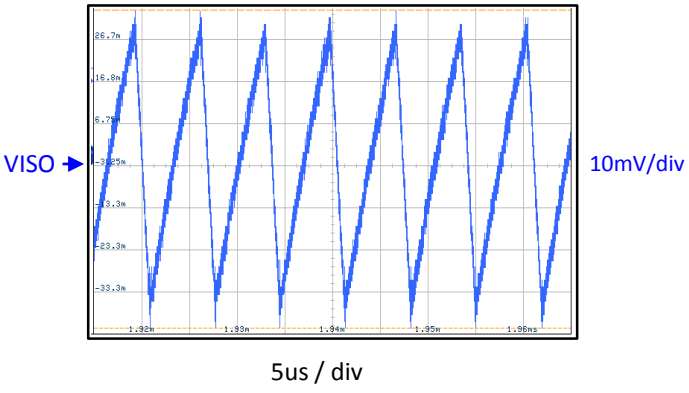


Figure 7- 12 V_{INP} = 5V, V_{ISO} = 3.7V, I_{ISO} = 130mA

V_{ISO} ripple voltage(peak to peak): 76mV

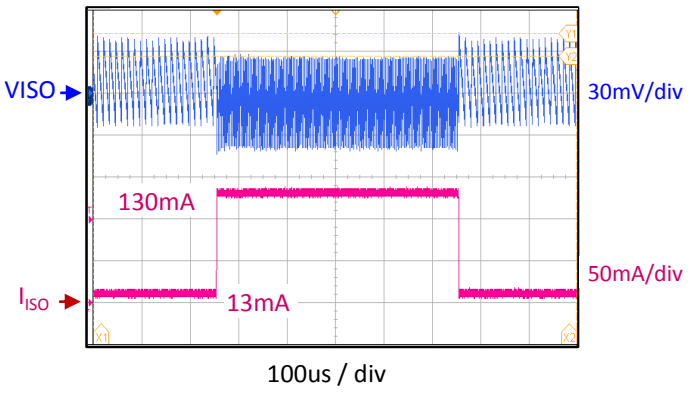


Figure7- 13 V_{ISO} Load transient response V_{INP} = 5V, V_{ISO} = 5V, Load step: 13mA to 130mA

V_{ISO} ripple voltage(peak to peak): 16mV

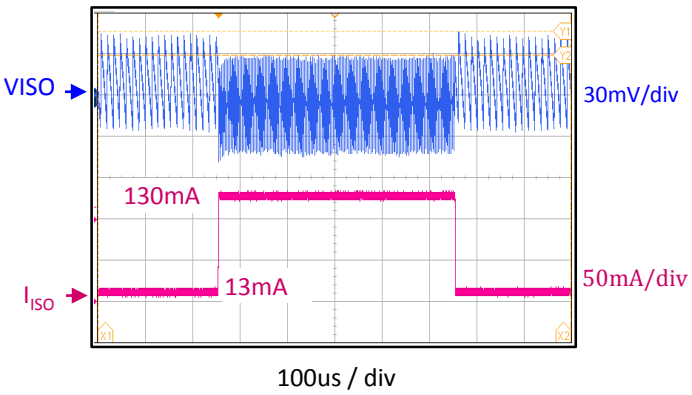


Figure7- 14 V_{ISO} Load transient response V_{INP} = 5V, V_{ISO} = 5.4V, Load step: 13mA to 130mA

V_{ISO} ripple voltage(peak to peak): 17mV

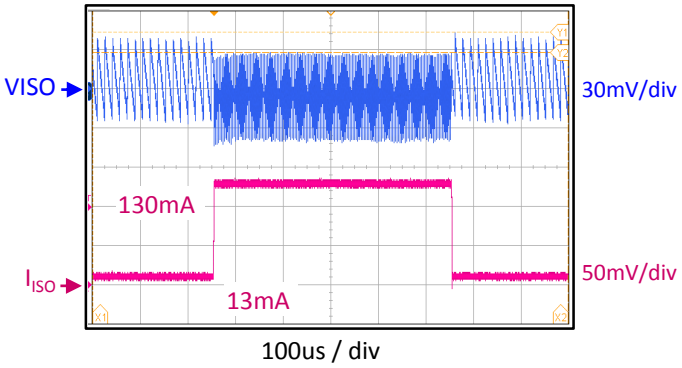


Figure7- 15 V_{ISO} Load transient response: V_{INP} = 5V, V_{ISO} = 3.3V, Load step: 13mA to 130mA

V_{ISO} ripple voltage(peak to peak): 15mV

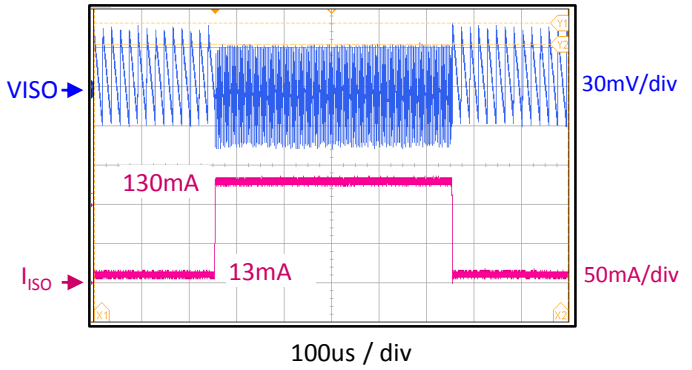


Figure7- 16 V_{ISO} Load transient response: V_{INP} = 5V, V_{ISO} = 3.7V, Load step: 13mA to 130mA

V_{ISO} ripple voltage(peak to peak): 16mV

7.10.3 Isolated Supply Voltage Typical Characteristics

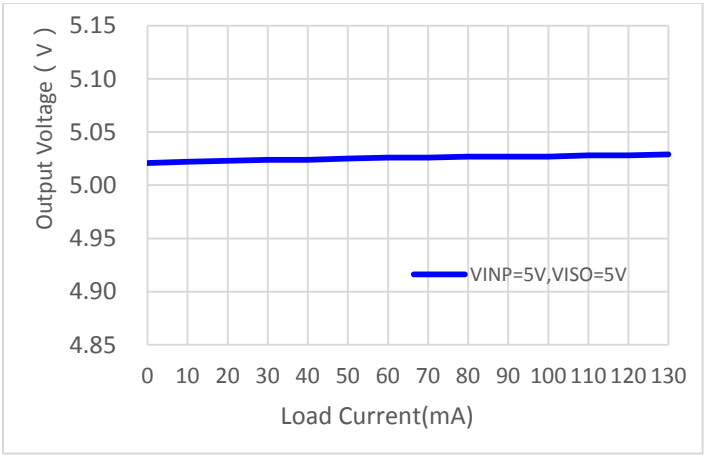


Figure7- 17 V_{ISO} Load Regulation; V_{INP} = 5V, V_{ISO} = 5V

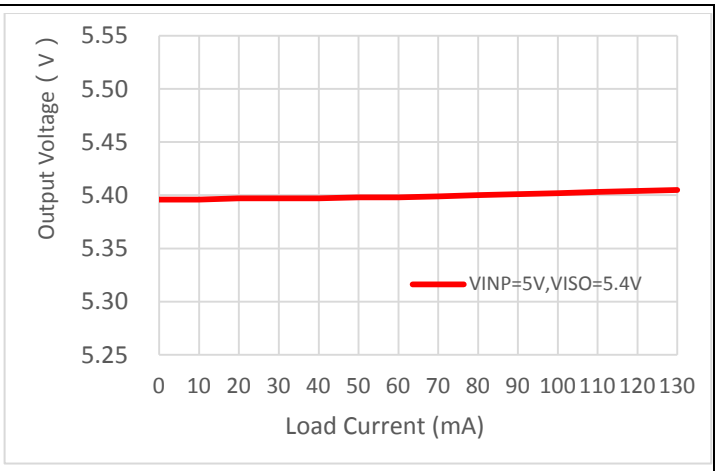


Figure7- 18 V_{ISO} Load Regulation; V_{INP} = 5V, V_{ISO} = 5.4V

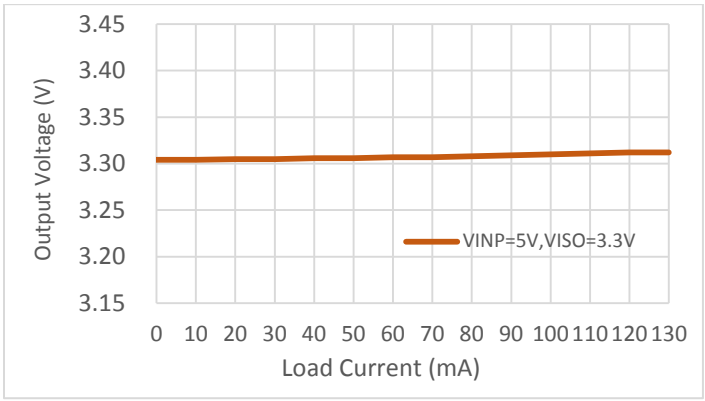


Figure7- 19 V_{ISO} Load Regulation; V_{INP} = 5V, V_{ISO} = 3.3V

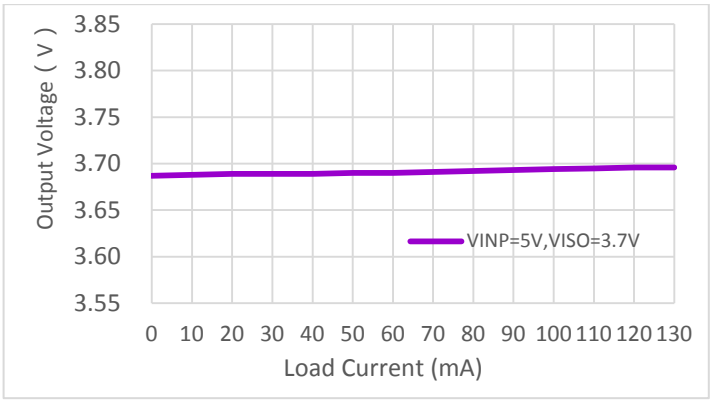


Figure7- 20 V_{ISO} Load Regulation; V_{INP} = 5V, V_{ISO} = 3.7V

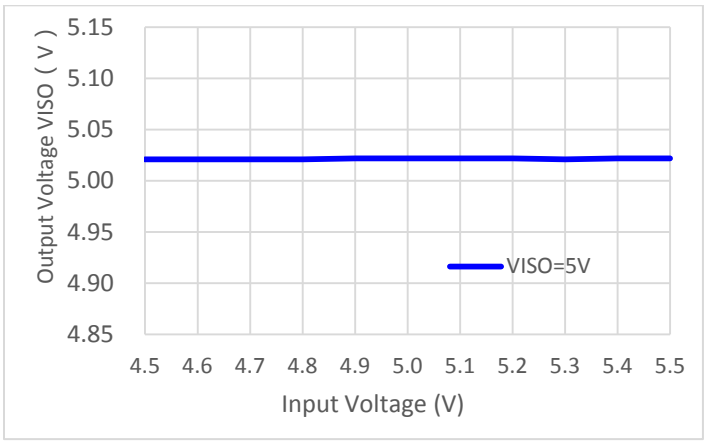


Figure7- 21 V_{ISO} Line Regulation; V_{INP} = 4.5V to 5V, V_{ISO} = 5V

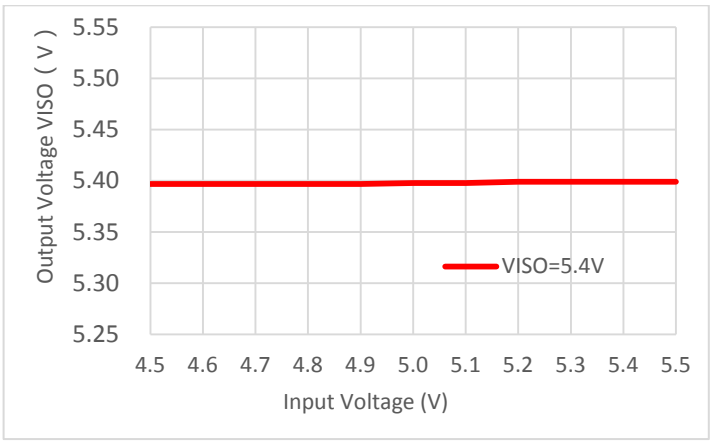


Figure7- 22 V_{ISO} Line Regulation; V_{INP} = 4.5V to 5V, V_{ISO} = 5.4V

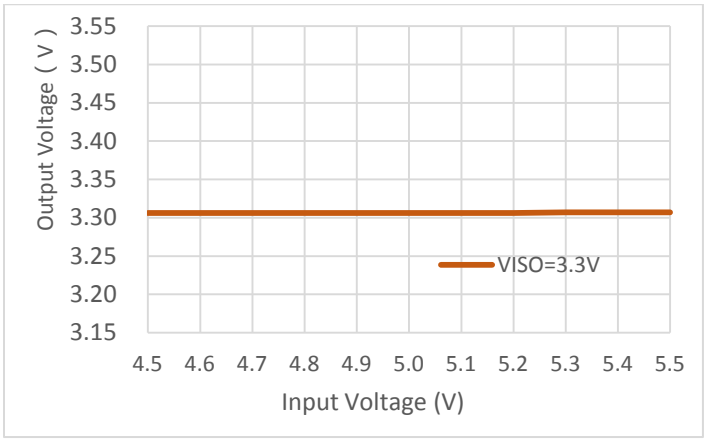


Figure7- 23 V_{ISO} Line Regulation; V_{INP} = 4.5V to 5V, V_{ISO} = 3.3V

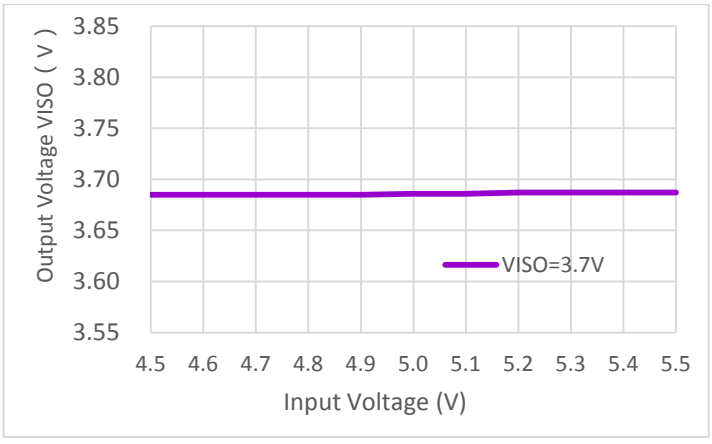


Figure7- 24 V_{ISO} Line Regulation; V_{INP} = 4.5V to 5V, V_{ISO} = 3.7V

7.10.4 Power Supply Efficiency vs. Load Current

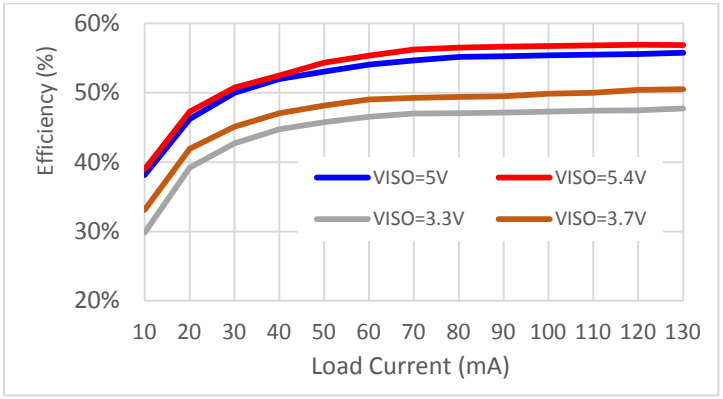


Figure7- 25 Power Supply Efficiency vs. Load Current

V_{INP} = 5V, V_{ISO} = 5V; V_{INP} = 5V, V_{ISO} = 5.4V;
V_{INP} = 5V, V_{ISO} = 3.3V; V_{INP} = 5V, V_{ISO} = 3.7V

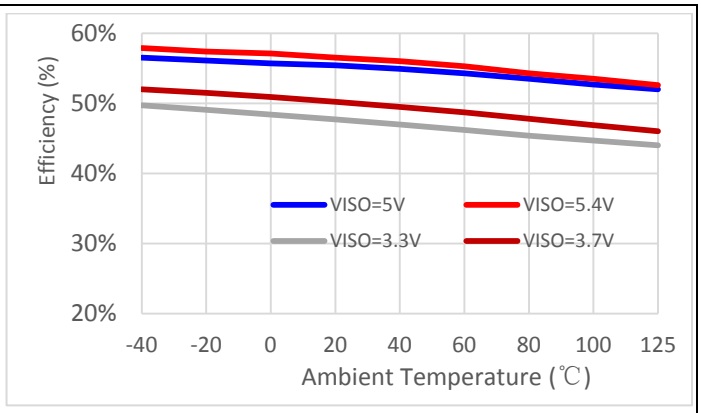


Figure7- 26 Power Supply Efficiency vs. Temperature

V_{INP} = 5V, V_{ISO} = 5V; V_{INP} = 5V, V_{ISO} = 5.4V;
V_{INP} = 5V, V_{ISO} = 3.3V; V_{INP} = 5V, V_{ISO} = 3.7V

7.10.5 Quiescent Current and Shutdown Current

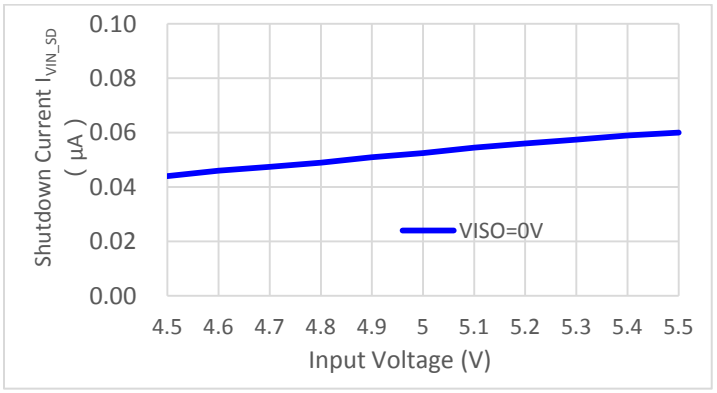


Figure 7- 27 Shutdown Current vs. Input voltage;
V_{INP} = 4.5V to 5.5V, EN connected to GNDP

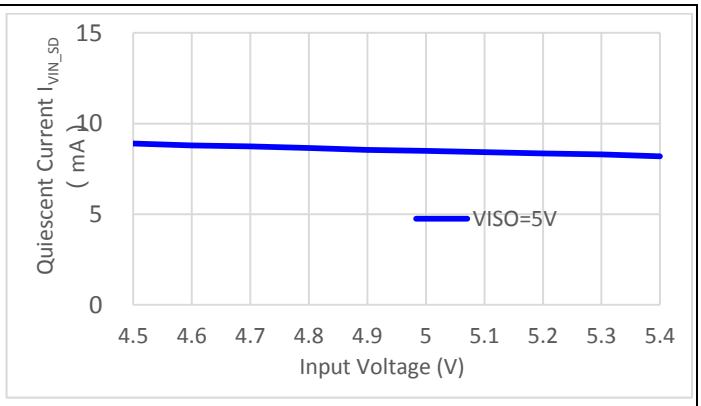


Figure7- 28 Quiescent Current vs. Input Voltage
V_{INP} = 4.5V to 5.5V, V_{ISO} = 5V, EN connected to VINP

7.10.6 Maximum Output Current vs. Temperature

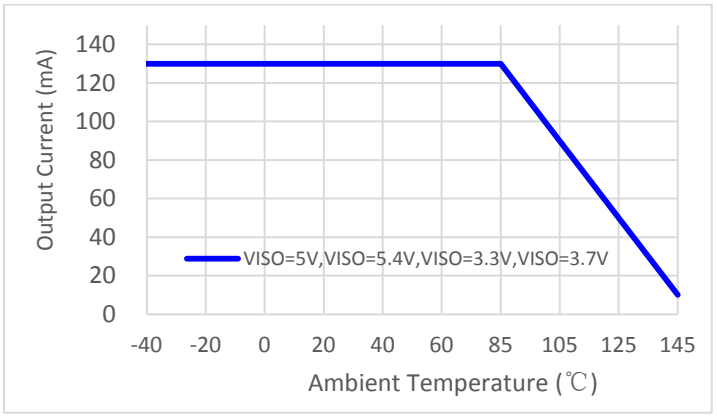


Figure 7- 29 Maximum V_{ISO} Output Current vs. Temperature V_{INP} = 4.5V to 5.5V

8 Detailed Description

8.1 Overview

The CA-IS3105W is a complete isolated DC-DC converter designed to provide isolated power with up to 650mW output power across a 5kV$_{RMS}$ isolation barrier. The device operates over 4.5V to 5.5V input and uses a proprietary control mechanisms. The input supply V$_{INP}$ is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side and regulated to a fixed output voltage set by the SEL pin. The soft-start feature allows to reduce input inrush current and avoid output overshoot. The device also incorporates an output enable (EN) control and undervoltage lockout function that allows the user to turn on the part at the desired input-voltage level. Figure 8-1 shows the CA-IS3105's functional block diagrams. Connect the EN pin to the VINP pin or force this pin high to turn on the DC-DC converter. Force this pin low to disable the device and enter low-current shutdown mode. This device offers a ready-made, reliable, easy-to-use solution and allows users save PCB space and reduce design time for the popular 5V, 3.3V voltage rails.

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the switching operation and triggers a hiccup mode. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode operation ensures low power dissipation under output short-circuit conditions.

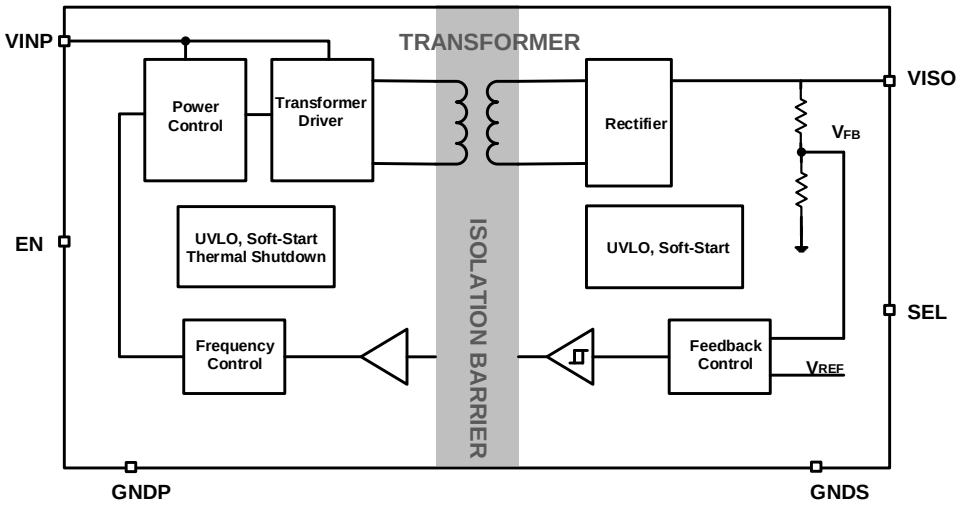


Figure 8-1 Functional Block Diagrams

8.2 Output Voltage Selection

At startup, the CA-IS3105W monitors the state of pin SEL after applying V$_{INP}$ supply voltage above the UVLO rising threshold or enabling via the EN pin, to detect the desired regulation voltage level for the V$_{ISO}$ output. After this initial monitoring, the SEL pin no longer affects the V$_{ISO}$ output level. In order to change the output level, either the EN pin must be toggled or the V$_{INP}$ power supply must be cycled off and back on. See Table. 8-1 for the output voltage selection.

Table. 8-1 V$_{ISO}$ Output Voltage Selection

EN	SEL	VISO
High	Sorted to VISO	5V
High	100kΩ to VISO	5.4V
High	Shorted to GNDS	3.3V
High	100KΩ to GNDS	3.7V
High	OPEN	Unsupported
Low	X	0V

8.3 Protection Functions

8.3.1 UVLO and Soft-Start

The CA-IS3105W has an undervoltage lockout (UVLO) on the V_{INP} power supply. Upon power-up, while the V_{INP} voltage is below the threshold voltage V_{UVLO+}(2.6V, typ.) the primary side transformer driver is disabled, and V_{ISO} output is off. The output powers up once the threshold is met. This allows the user to turn on the part at stable input-voltage level.

For many applications, it is necessary to minimize the inrush current at start-up. The CA-IS3105W built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. Once input power supply is applied at VINP pin, the internal soft-start circuit will control the power delivered to the output gradually increase, allowing for a graceful turn-on ramp.

8.3.2 Overcurrent Protection

The CA-IS3105W is provided with an over-current protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the switching operation and triggers a hiccup mode whenever the switch current exceeds the internal current limit. Once the hiccup timeout period expires, soft-start is attempted again. The hiccup condition is cleared when the over-current is removed.

8.3.3 Thermal Shutdown

Thermal-shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds T_{SD}, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools and junction temperature drops to normal operation temperature range of the device.

9 Applications Information

9.1 Typical Application Circuit

The CA-IS3105W is high-integration isolated power supply solution. Included in the package are the switching controller, power switches, transformer, and all support components. Only output and input bypass capacitors are needed to finish the design. For the applications with LDO post regulator, it may need a single 100kΩ external resistor to set the output level to 3.7V or 5.4V, see Figure 9-1 typical application circuit.

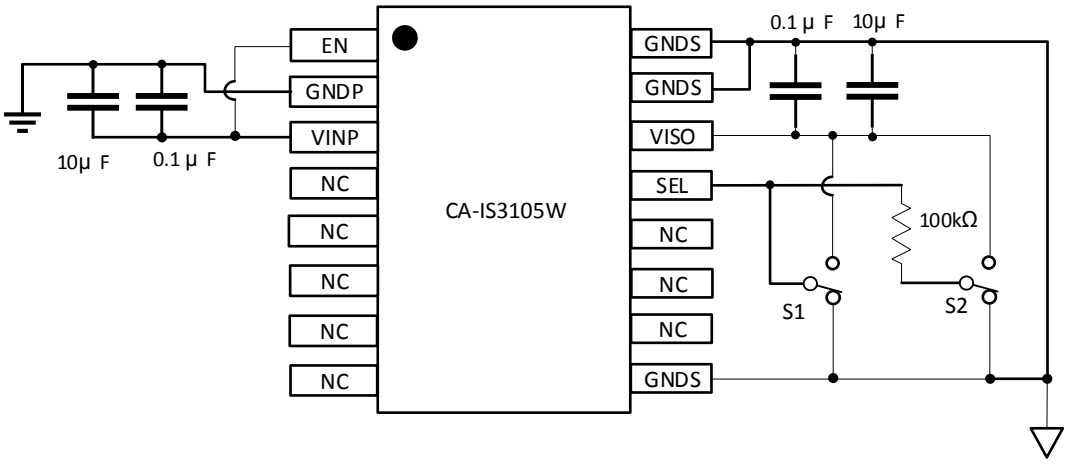


Figure 9-1 CA-IS3105W Typical Application Circuit

9.2 Input and Output Capacitors

The input capacitors (between VINP and GNDP) are required to reduce the peak current drawn from input power source and reduce the switching noise, increase efficiency. For the input capacitors, choose the ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. For most applications, we recommend to use at least 0.1μF and 10μF ceramic capacitors with X5R or X7R temperature characteristic. When operating at a VINP voltage close to the UVLO threshold, more input capacitance may be required to keep the input voltage ripple from tripping the UVLO protection.

The output capacitors between VISO and GNDS are required as well to keep the output voltage ripple small and to ensure loop stability. These bypass capacitors must have low impedance at the switching frequency. Ceramic capacitors are recommended due to their small size and low ESR. Make sure the capacitor does not degrade its capacitance significantly over temperature and DC bias. It is recommended to have at least 10μF of effective capacitance at output.

9.3 PCB Layout Guidelines

High switching frequencies and large peak currents make PCB layout a very important part of the DC-DC converter design. Good PCB design minimizes excessive electromagnetic interference (EMI) and voltage gradients in the ground plane to avoid instability and regulation errors. Even with the high level of integration, like CA-IS3105W, users may fail to achieve specified operation with a haphazard or poor layout. So careful PCB layout is critical to achieve clean and stable operation, and ensure that the grounding and heat sinking are acceptable.

The input capacitors should be placed as close as possible to the CA-IS3105W's VINP and GNDP pins. Place the output capacitors as close as possible to VISO and GNDS pins, see Figure 9-2 recommended components placement for the PCB layout. Connect all of the ground (GNDP, GNDS) connections to as large a copper pour or plane area as possible for best heat-sinking. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the CA-IS3105W device on the outer copper layers.

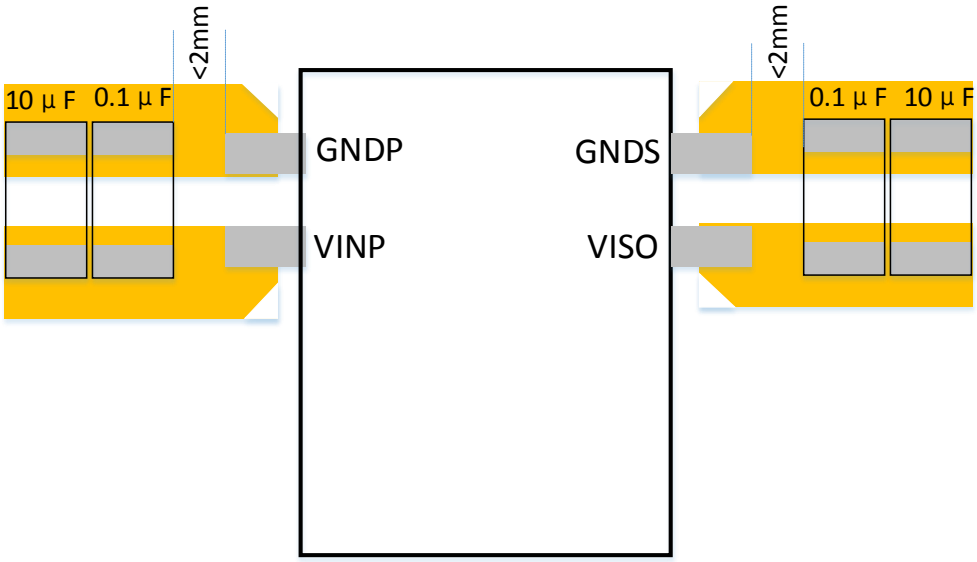
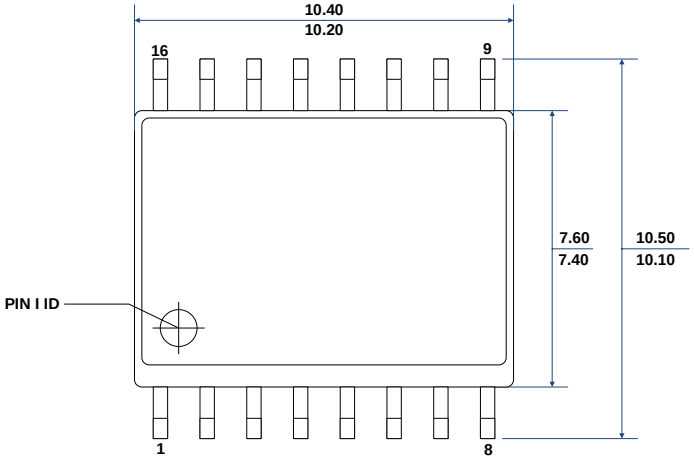


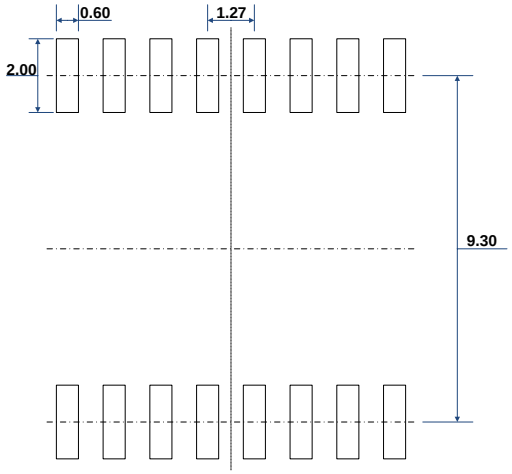
Figure 9-2 Recommended Bypass Capacitors Placement

10 Package Information

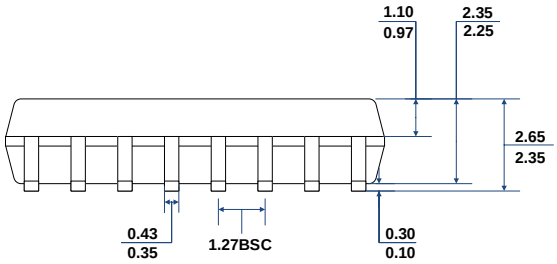
The following figure illustrates the size drawing and recommended pad size of SOIC16-WB wide-body package for the CA-IS3105W isolated DC-DC converter. All dimensions are in millimeters.



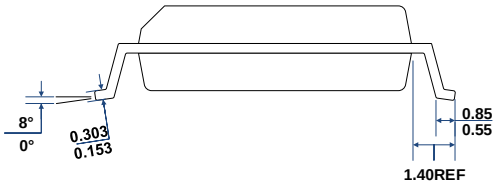
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

11 Soldering Temperature (reflow) Profile

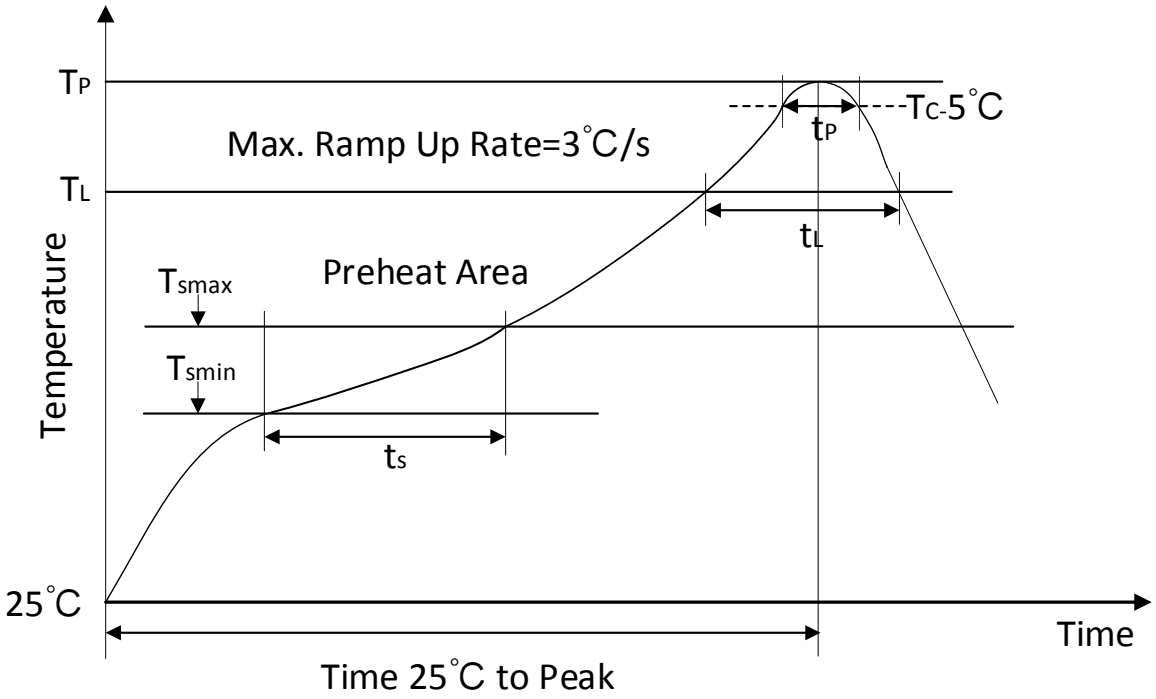


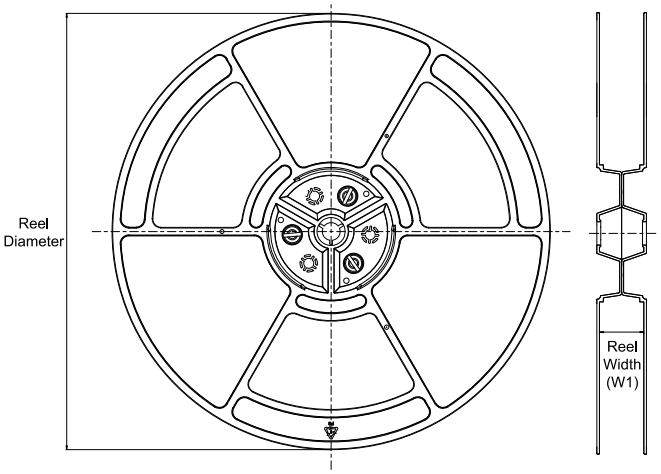
Figure11- 1 Soldering Temperature (reflow) Profile

Table 11- 1 Soldering Temperature Parameter

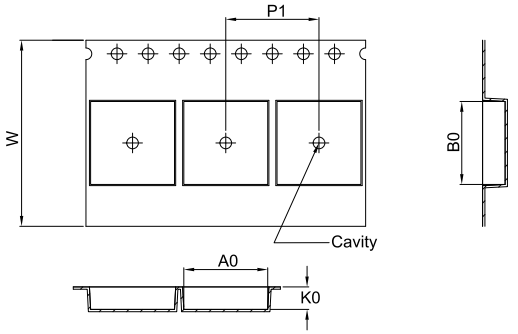
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217 ℃ to Peak)	3℃/second max
Time of Preheat temp(from 150 ℃ to 200 ℃	60-120 second
Time to be maintained above 217 ℃	60-150 second
Peak temperature	260 +5/-0 ℃
Time within 5 ℃of actual peak temp	30 second
Ramp-down rate	6 ℃/second max.
Time from 25℃ to peak temp	8 minutes max

12 Tape and Reel Information

REEL DIMENSIONS

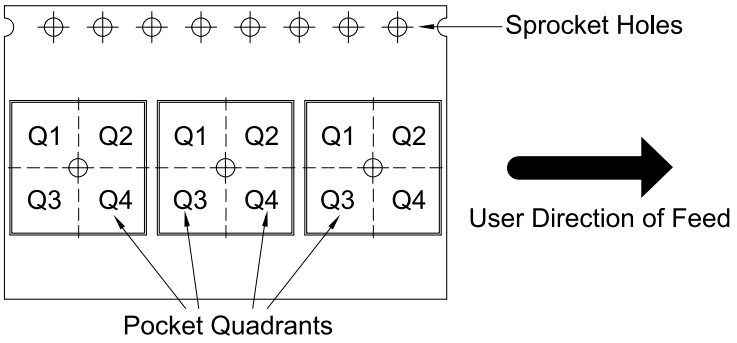


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3105W	SOIC	W	16	1000	330	16.4	10.8	10.7	2.9	12.0	24.0	Q1

13 Important statement

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