NSOPA905x

40-V Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amp

Preliminary Datasheet (EN) 0.1

Subject to change without notice

Product Overview

The NSOPA905x family (NSOPA9051, NSOPA9052, and NSOPA9054) is a family of high voltage (40 V) general purpose operational amplifiers. These devices offer exceptional DC precision and AC performance, including rail-to-rail input/output, low offset (±200 µV, typical), low offset drift (±0.5 µV/°C, typical), low noise (10.5 nV/√Hz and 6 µVPP), and 6MHz bandwidth. Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (65mA), high slew rate (25V/µs), high capacitive load drive (1nF), and shutdown functionality make the NSOPA905x a robust, high performance operational amplifier for high-voltage industrial applications.

The NSOPA905x family of op amps is available in standard packages (SOT-23, MSOP, SOIC, and TSSOP), and is specified from -40°C to 125°C.

Key Features

- High slew rate: 25 V/µs typ
- Low offset voltage: 200uV typ
- Low offset voltage drift: ±0.5 µV/°C typ
- Differential and common-mode input voltage range to supply rail MUX-friendly/comparator inputs

  Amplifier operates with differential inputs up to supply rail

  Amplifier can be used in open-loop or as comparator
- Low quiescent current: 600 µA per amplifier
- Wide supply: ±1.35 V to ±20 V, 2.7 V to 40 V
- Robust EMIRR performance: EMI/RFI filters on input and supply pins

Device Information

Part Number	*Package*	*Body Size*
NSOPA9051-DSTAR	SOT-23 (5)	2.90 mm × 1.60 mm
NSOPA9051-DSPR	SOIC (8)	4.90 mm × 3.90 mm
NSOPA9052-DSPR	SOIC (8)	4.90 mm × 3.90 mm
NSOPA9052-DMSR	MSOP (8)	3.00 mm × 3.00 mm
NSOPA9054-DSPKR	SOP (14)	8.65 mm × 3.9 mm
NSOPA9054-DTSKR	TSSOP (14)	5.00 mm × 4.40 mm

Typical Application

- Low-power audio preamplifier
- Multiplexed data-acquisition systems
- Test and measurement equipment
- ADC driver amplifiers
- SAR ADC reference buffers
- Programmable logic controllers
- High-side and low-side current sensing

INDEX

1. PIN CONFIGURATION AND FUNCTION

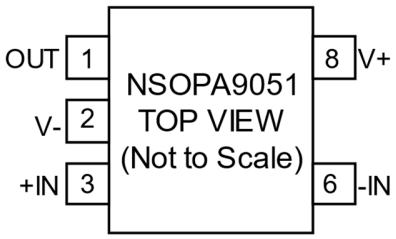

Figure 1-1 NSOPA9051 5-Pin SOT-23 Package Top View

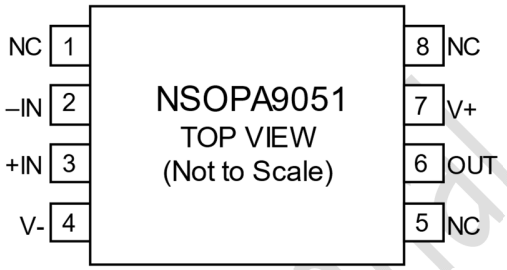

Figure 1-2 NSOPA9051 8-Pin SOIC Package Top View

Table 1 Pin Functions

SYMBOL	5-Pin SOT-23 *NO.*	8-Pin SOIC *NO.*	*FUNCTION*
+IN	3	3	Noninverting input
-IN	4	2	Inverting input
OUT	1	6	Output
V+	5	7	Positive Power supply
V-	2	4	Negative Power supply
NC	-	1, 5, 8	No internal connection

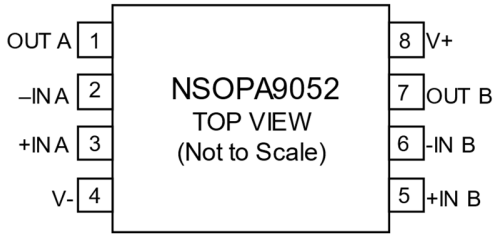

Figure 1-3 NSOPA9052 8-Pin SOIC and MSOP Package Top View

Table 2 Pin Functions

SYMBOL	*NO.*	*FUNCTION*
– IN A	2	Channel A Inverting input
+IN A	3	Channel A Noninverting input
OUT A	1	Channel A Output
–IN B	6	Channel B Inverting input
+IN B	5	Channel B Noninverting input
OUT B	7	Channel B Output
V+	8	Positive Power supply
V-	4	Negative Power supply

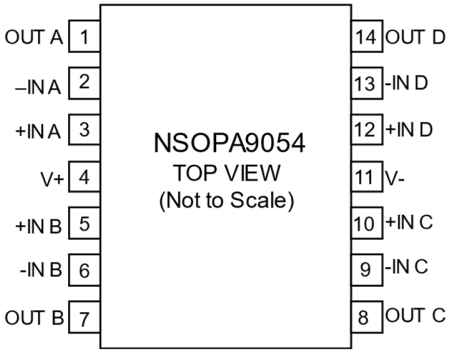

Figure 1-4 NSOPA9054 14-Pin SOIC and TSSOP Package Top View

SYMBOL	*NO.*	*FUNCTION*
IN– A	2	Channel A Inverting input
IN+ A	3	Channel A Noninverting input
OUT A	1	Channel A Output
IN– B	6	Channel B Inverting input
IN+ B	5	Channel B Noninverting input
OUT B	7	Channel B Output
IN– C	9	Channel C Inverting input
IN+ C	10	Channel C Noninverting input
OUT C	8	Channel C Output
IN– D	13	Channel D Inverting input
IN+ D	12	Channel D Noninverting input
OUT D	14	Channel D Output
V+	4	Positive Power supply
V-	11	Negative Power supply

2. SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Supply voltage $V_S = (V_+) - (V_-)$	V_S		42	V
Differential, IN+ to IN− inputs			V_S + 0.3	V
Common-Mode input voltage		−0.3	V_S + 0.3	V
Output		−0.3	V_S + 0.3	V
Ambient temperature	T_A	−40	125	°C
Junction temperature	T_J	−40	150	°C
Storage temperature	T_{stg}	−40	150	°C
Electrostatic discharge	HBM		±2000	V
	CDM		±1000	V

RECOMMENDED OPERATING CONDITIONS

Parameters	*Symbol*	*Min*	*Max*	*Unit*
Supply voltage	V_S	2.7	40	V
Input voltage		(V_-) - 0.2	(V_+) + 0.2	V
Operating free-air temperature	T_A	-40	125	°C

THERMAL INFORMATION

Parameters	*Symbol*	SOT23-5	SOIC-8	MSOP-8	TSSOP-14	SOIC-14	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}				134.4	114.2	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$				62.6	70.3	°C/W
Junction-to-board thermal resistance	θ_{JB}				77.6	70.2	°C/W

[1] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

3. ELECTRICAL CHARACTERISTICS

For V_S = (V_+) – (V_-) = 4.5 V to 36 V (±2.25 V to ±18 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and VOUT = V_S/2, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Unit
INPUT							
Offset voltage	V_{OS}	V_{CM} = V–			±0.2	±1.2	mV
		T_A = –40°C to 125°C				±1.5	
Offset voltage Drift	dV_{OS}/dT	T_A = –40°C to 125°C			0.5		µV/°C
Common-mode input range	V_{CM}	Guaranteed by CMRR tests		(V_-)-0.1		(V_+)+0.1	V
Common mode rejection ratio	CMRR	V_S = 40V, (V_-)–0.1V < V_{CM} < (V_+)–2.5V (PMOS pair)	T_A = –40°C to 125°C	110	128		dB
		V_S = 4V, (V_-)–0.1V < V_{CM} < (V_+)–2.5V (PMOS pair)		90	105		
		V_S = 2.7V~40V, (V_+)–2.5V < V_{CM} < (V_+)+0.1V			85		
Power supply rejection ratio	PSRR	V_S = 4V to 40V, V_{CM} = (V_-)		125	135		dB
		V_S = 2.7V to 40V, V_{CM} = (V_-)		110	120		
Input bias current	I_B	V_S = 2.7V to 40V, V_{CM} = V_S/2			TBD		pA
		T_A = –40°C to 125°C			TBD		nA
Input offset current	I_{OS}	V_S = 2.7V to 40V, V_{CM} = V_S/2			TBD		pA
		T_A = –40°C to 125°C			TBD		nA
input Impedance	Z_{ID}	Differential			0.2||15		GΩ||pF
	Z_{ICM}	Common-mode			1||10		TΩ||pF
OPEN-LOOP GAIN							
Open-loop voltage gain	A_{OL}	V_S = 40V	(V_-)+0.2V<V_O<(V_+)–0.2V T_A=–40°C to 125°C	120	140		dB
		V_S = 4V		105	125		
		V_S = 2.7V			120		
OUTPUT							
Output swing from rail headroom		V_S=2.7~40V, R_L=no load	V_{OD} = 50 mV		1	5	mV
		V_S=2.7V, R_L=10kΩ			5	10	
		V_S=40V, R_L=10kΩ			50	55	
		V_S=2.7V, R_L=2kΩ			22	40	
		V_S=40V, R_L=2kΩ			140	200	
Short-Circuit Current	I_{SC}	Sinking			65		mA
		Sourcing			90		
Output Impedance	Z_O	f = 1 MHz, I_O = 0 A			600		Ω

ELECTRICAL HARACTERISTICS (continued)

For V_S = (V_+) – (V_-) = 2.7 V to 40 V (±1.35 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and VOUT = V_S/2, unless otherwise noted.

Parameters	*Symbol*	*Condition*		*Min*	*Typ*	*Max*	*Unit*
FREQUENCY RESPONSE							
Gain-bandwidth product	GBP	V_S = 40 V, C_L = 10 pF			6		MHz
Phase margin	PM	V_S = 40 V, C_L = 10 pF			52		Degree
Settling time	T_S	To 0.1%, 10 V Step, C_L = 10 pF			2		µs
		To 0.1%, 2 V Step, C_L = 10 pF			1		
		To 0.01%, 10 V Step, C_L = 10 pF			TBD		
		To 0.01%, 2 V Step, C_L = 10 pF			TBD		
Slew rate	SR	10-V step, G= +1			25		V/µs
Total harmonic distortion + noise	THD+N	V_{rms} = 1 V, G = 1, f = 1 kHz, R_L= 10kΩ			TBD		dB
Overload recovery time		V_{IN} × Gain > V_S			300		ns
EMI rejection ratio	EMIRR	f = 1GHz			80		dB
NOISE (INPUT REFERRED)							
Input voltage noise density	e_n	f = 1 kHz			25		nV/$\sqrt{Hz}$
		f = 10 kHz			10		
Input Voltage noise	$e_{n\ p-p}$	f = 0.1 Hz to 10 Hz			6		uVpp
POWER SUPPLY							
Operating voltage range	V_S	Guaranteed by PSRR Tests		2.7		40	V
Quiescent current	I_Q	V_S=2.7V			560	720	uA
			T_A = –40°C to 125°C			830	
		V_S=40V			600		
			T_A = –40°C to 125°C			850	

4. TYPICAL PERFORMANCE CHARACTERISTICS

For $V_S = (V_+) - (V_-) = 2.7$ V to 40 V (±1.35 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_O = V_S/2$, unless otherwise noted.

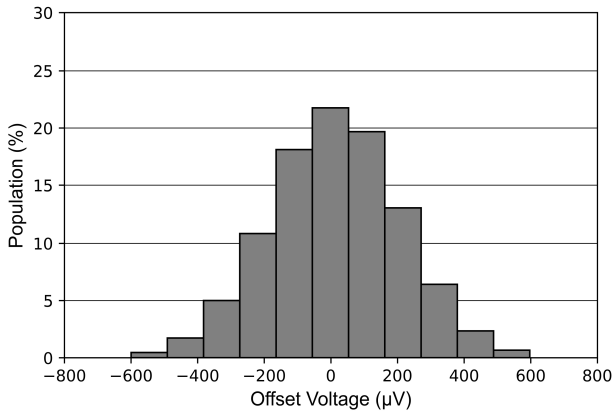

Figure 4-1 Offset Voltage Production Distribution

TBD

Figure 4-2 Offset Voltage Drift Distribution

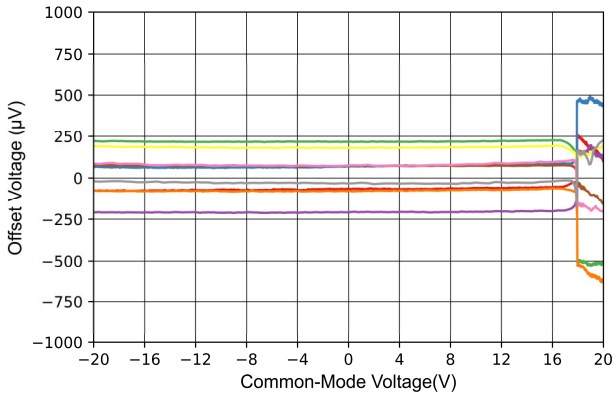

Figure 4-3 Offset Voltage vs Common-Mode Voltage

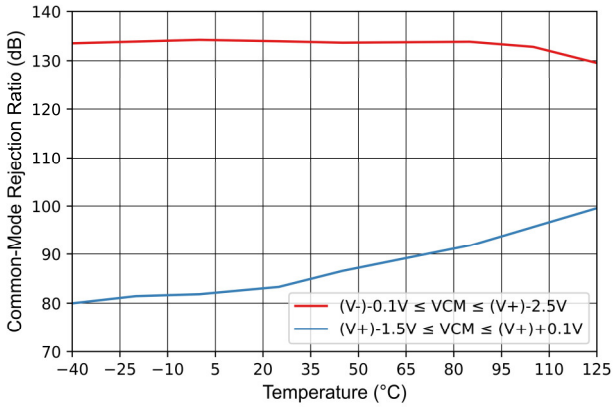

Figure 4-4 CMRR vs Temperature

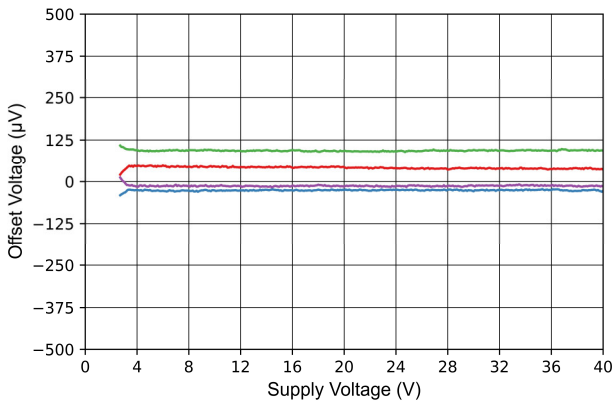

Figure 4-5 Offset Voltage vs Power Supply

TBD

Figure 4-6 PSRR vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For $V_S = (V_+) - (V_-) = 2.7$ V to 40 V (± 1.35 V to ± 20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_O = V_S/2$, unless otherwise noted.

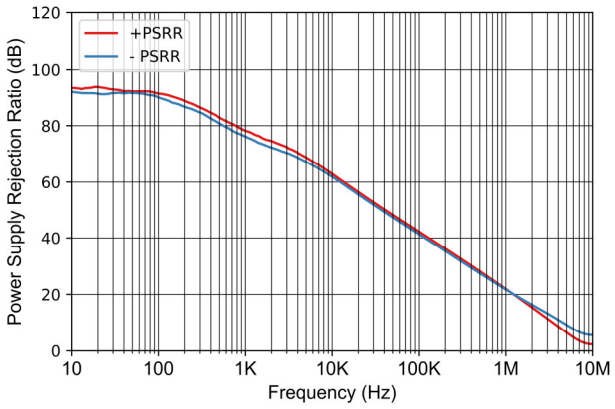

Figure 4-7 Power-Supply Rejection Ratio vs Frequency

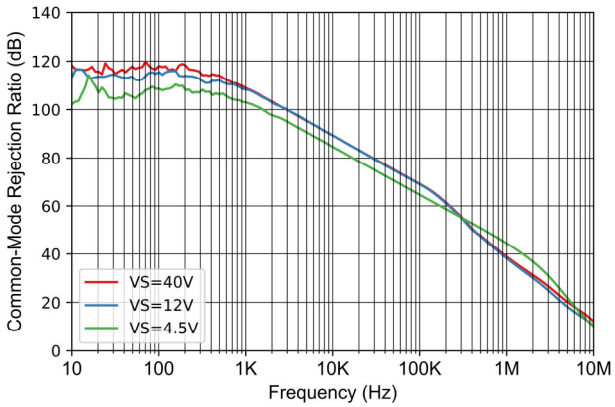

Figure 4-8 Common-Mode Rejection Ratio vs Frequency

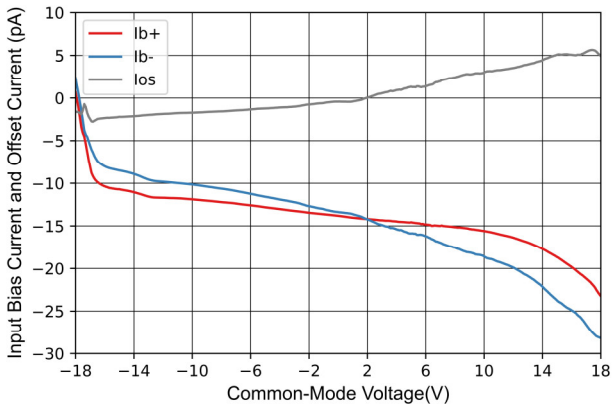

Figure 4-9 Input Bias Current vs Common-Mode Voltage

TBD

Figure 4-10 Input Bias Current vs Temperature

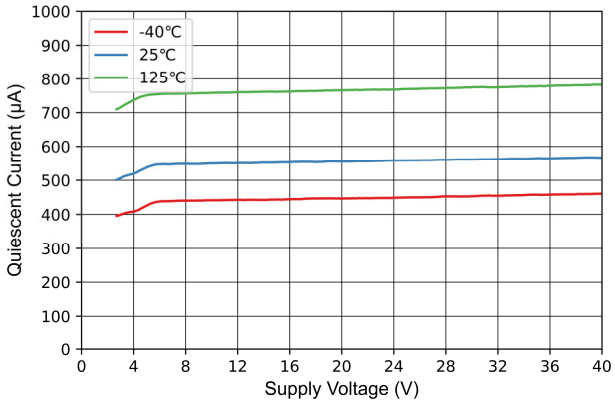

Figure 4-11 Quiescent Current vs Supply Voltage

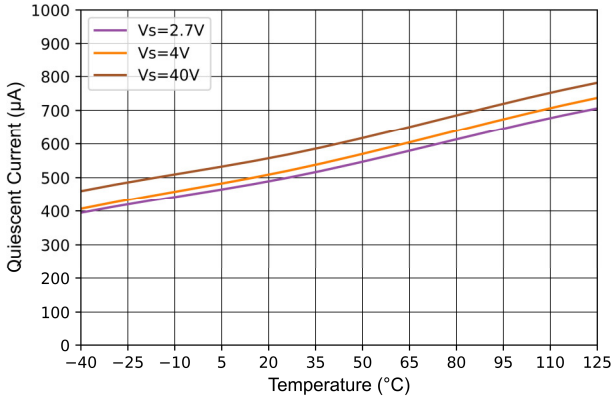

Figure 4-12 Quiescent Current vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For VS = (V+) – (V–) = 40 V (±20 V) at T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

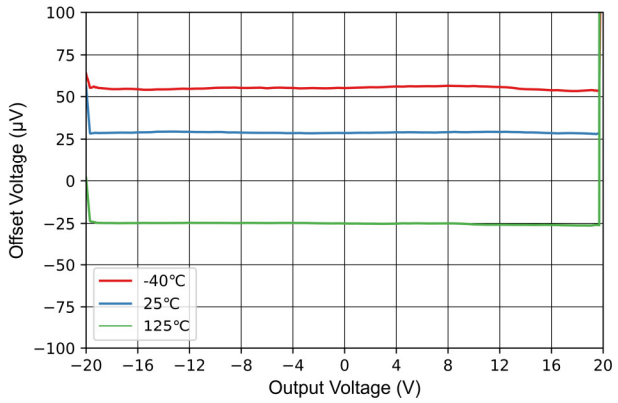

Figure 4-13 Offset Voltage vs Output Voltage

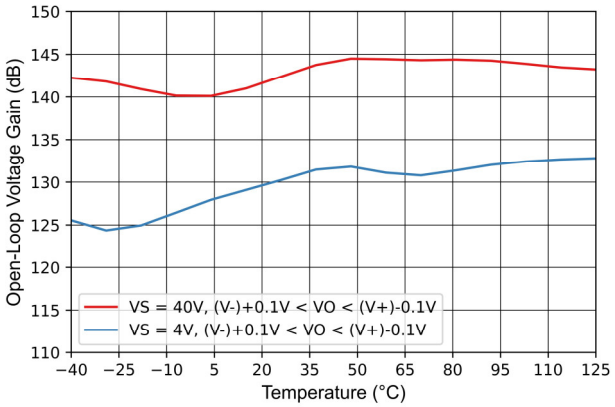

Figure 4-14 Open-Loop Voltage Gain vs Temperature

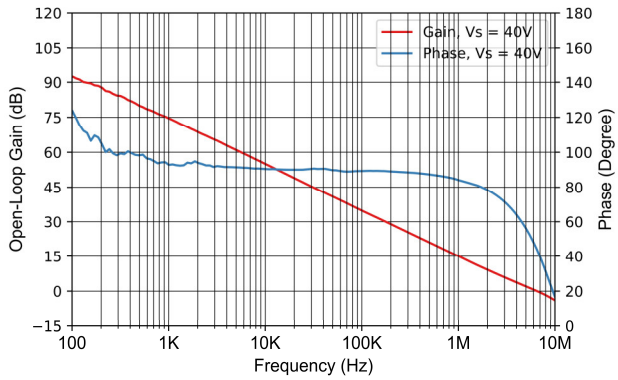

Figure 4-15 Open Loop Gain vs Frequency

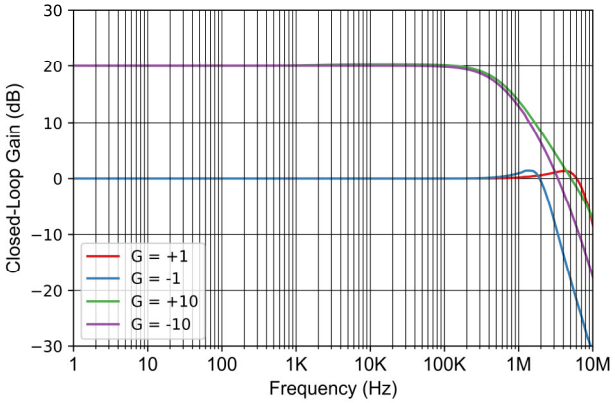

Figure 4-16 Closed Loop Gain and Phase vs Frequency

TBD

Figure 4-17 Maximum Peak Output Voltage vs. Frequency

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Figure 4-18 Maximum Peak Output Voltage vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For $V_S = (V_+) - (V_-) = 2.7$ V to 40 V ($\pm$1.35 V to ±20 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

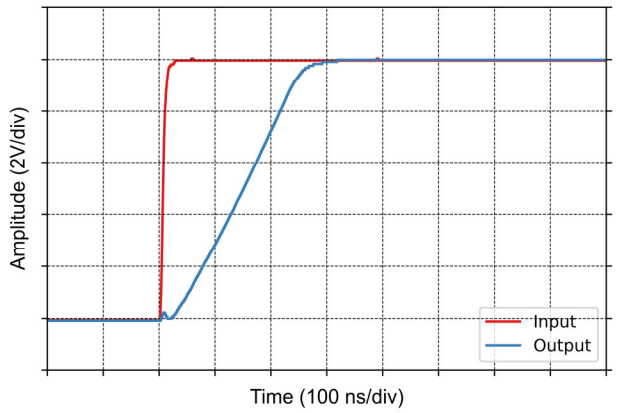


Figure 4-19 Large-Signal Step Response (Rising)

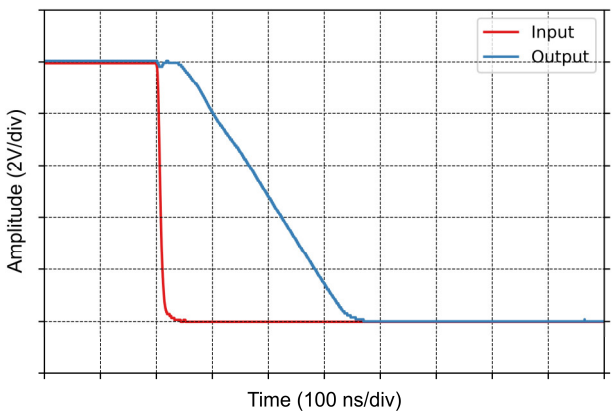


Figure 4-20 Large-Signal Step Response (Falling)

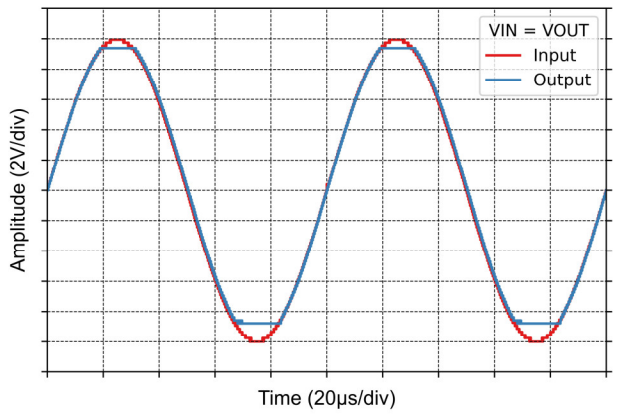


Figure 4-21 No Phase Reversal

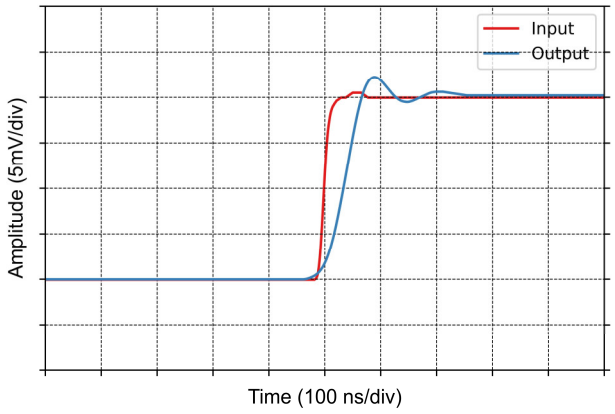


Figure 4-22 Small-Signal Step Response

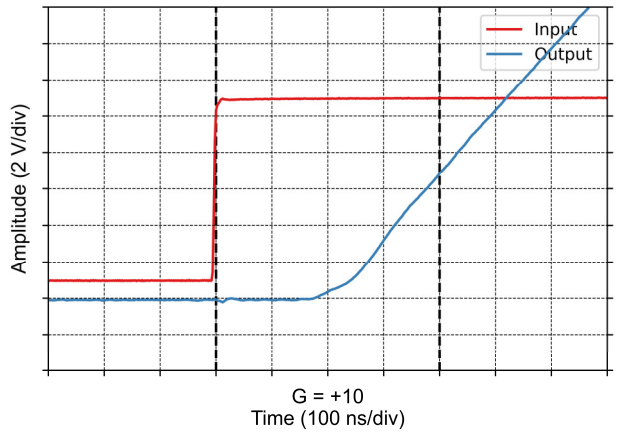


Figure 4-23 Positive Overload Recovery

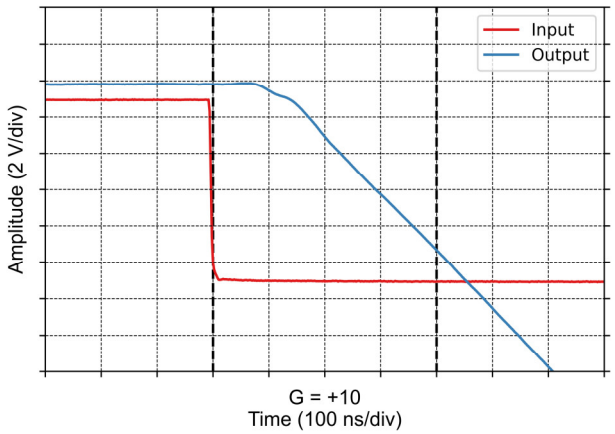


Figure 4-24 Negative Overload Recovery

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For VS = (V+) – (V–) = 40 V (±20 V) at T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

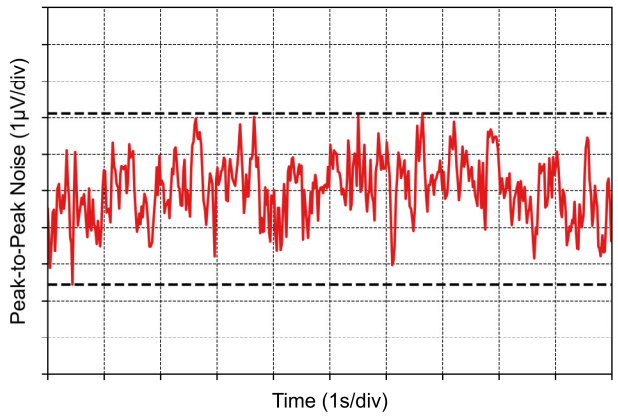


Figure 4-25 0.1-Hz to 10-Hz Noise

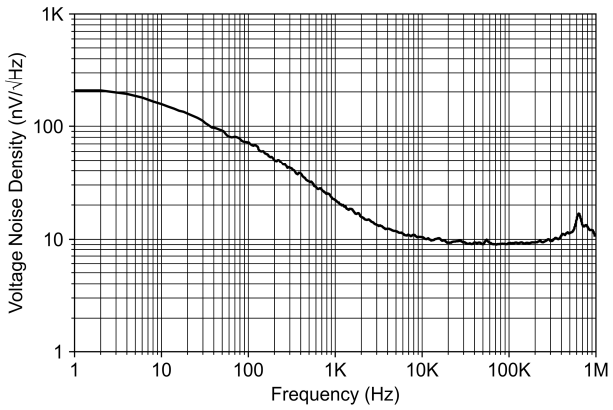


Figure 4-26 Input Voltage Noise Spectral Density

TBD

Figure 4-27 THD+N Ratio vs Frequency

TBD

Figure 4-28 THD+N vs Output Amplitude

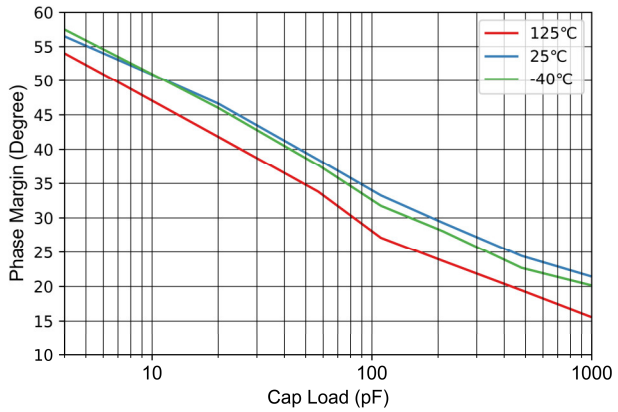


Figure 4-29 Phase Margin vs Capacitive Load

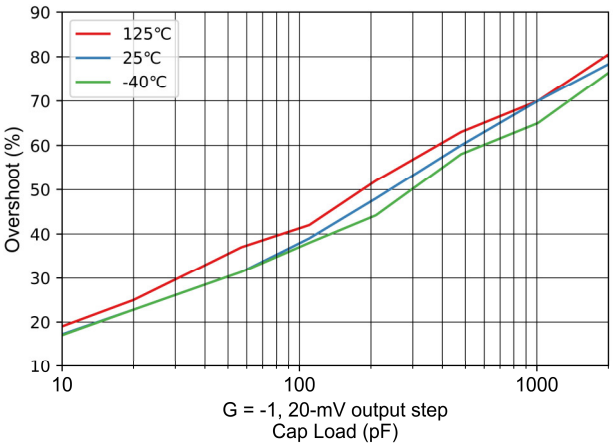


Figure 4-30 Small-Signal Overshoot vs Capacitive Load

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

For VS = (V+) – (V–) = 40 V (±20 V) at T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and VOUT = $V_S/2$, unless otherwise noted.

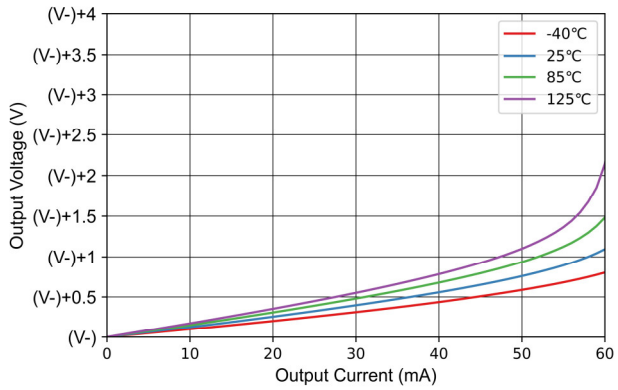


Figure 4-31 Output Voltage Swing vs Output Sinking Current

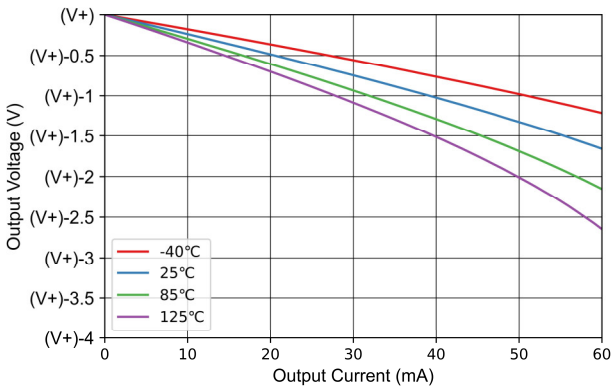


Figure 4-32 Output Voltage Swing vs Output Sourcing Current

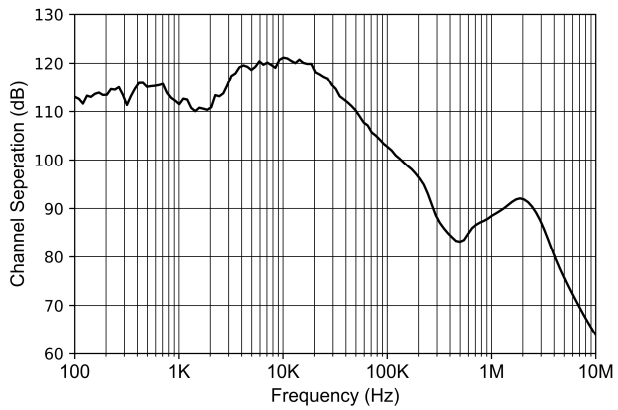


Figure 4-33 Channel Separation vs Frequency

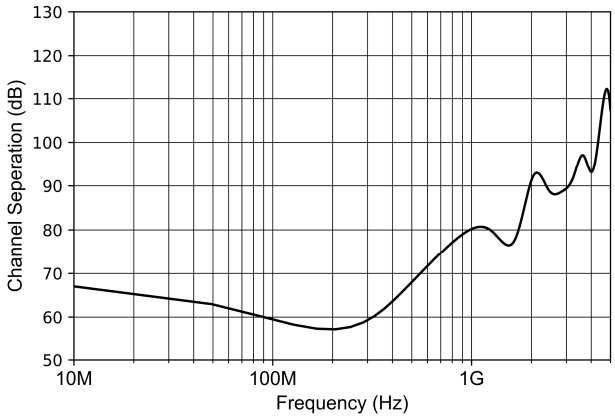
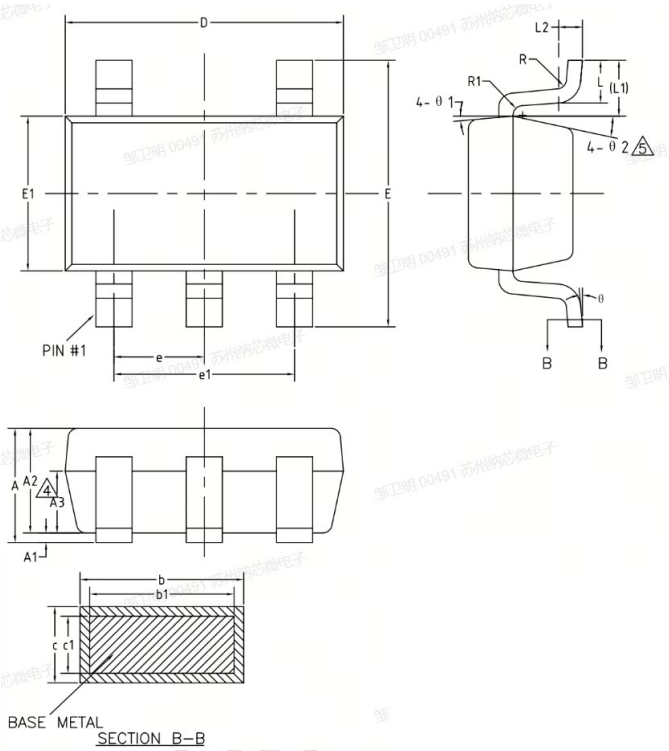


Figure 4-34 EMIRR vs Frequency

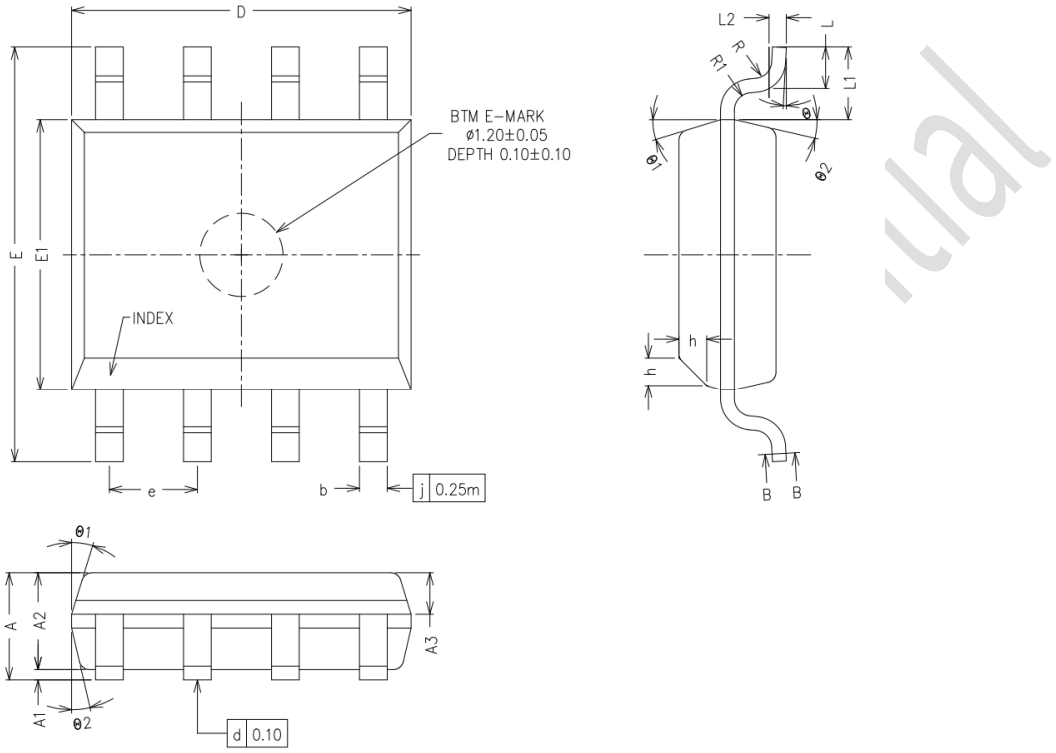
5. PACKAGE INFORMATION

SOT-23(5)



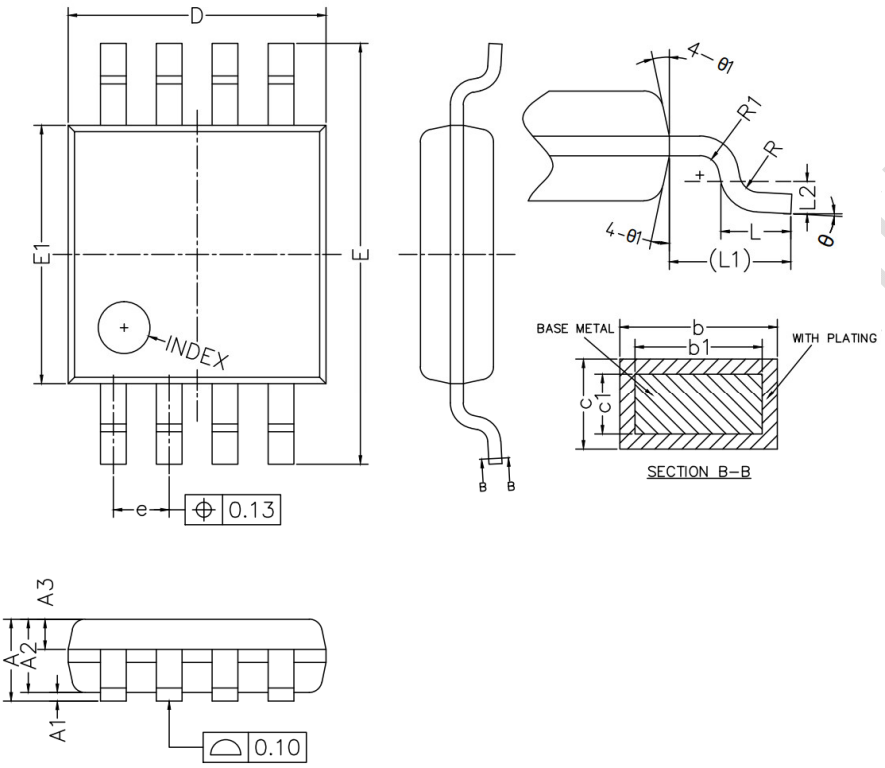
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.25	— —	0.049
A1	— —	0.15	— —	0.006
A2	1.00	1.20	0.039	0.047
A3	0.60	0.70	0.024	0.028
b	0.36	0.50	0.014	0.020
b1	0.36	0.45	0.014	0.018
c	0.14	0.20	0.006	0.008
c1	0.14	0.16	0.006	0.006
D	2.826	3.026	0.111	0.119
E	2.60	3.00	0.102	0.118
E1	1.526	1.726	0.060	0.068
e	0.90	1.00	0.035	0.039
e1	1.80	2.00	0.071	0.079
L	0.35	0.60	0.014	0.024
L1	0.59REF		0.023REF	
L2	0.25BSC		0.010BSC	
R	0.10	— —	0.004	— —
R1	0.10	0.25	0.004	0.010
θ	0°	8°	0°	8°
θ1	3°	7°	3°	7°
θ2	6°	14°	6°	14°

SOIC(8)



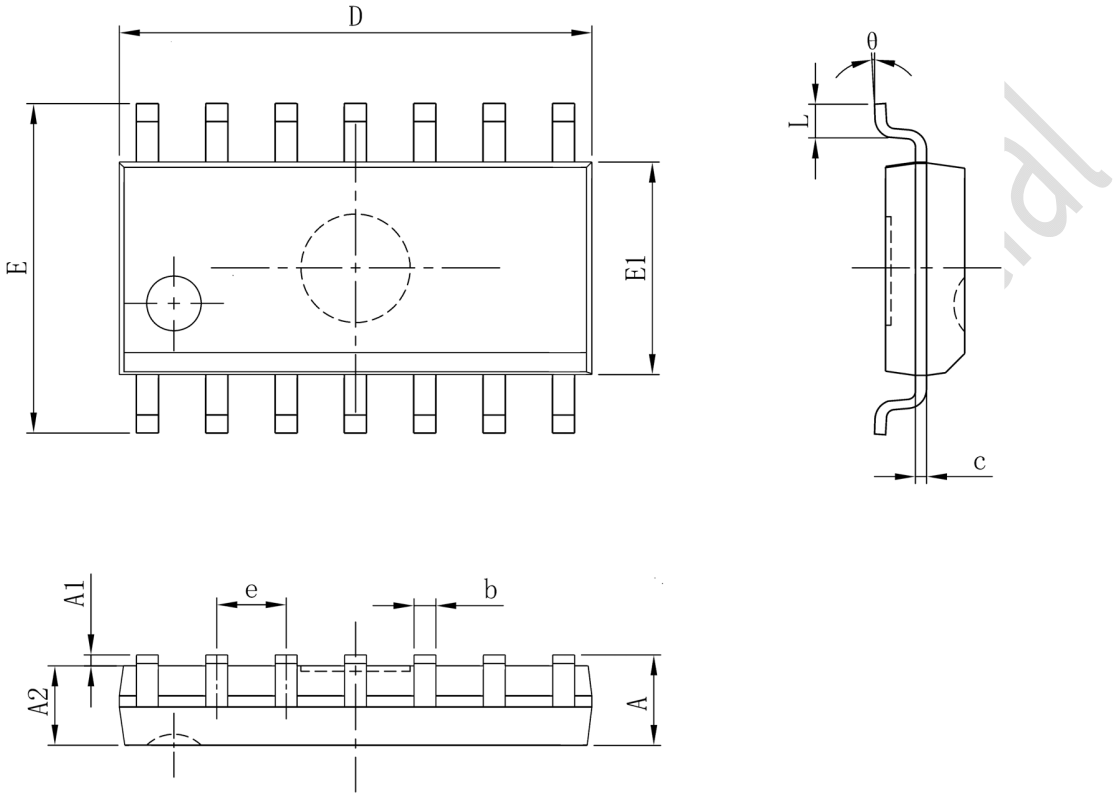
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.1	0.25	0.004	0.01
A2	1.30	1.50	0.051	0.059
A3	0.50	0.70	0.020	0.028
b	0.38	0.47	0.015	0.019
b1	0.37	0.40	0.015	0.016
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.15	0.157
e	1.17	1.37	0.046	0.054
L	0.45	0.80	0.018	0.031
L1	1.04REF		0.041REF	
L2	0.25BSC		0.010BSC	
R	0.07	— —	0.003	— —
R1	0.07	— —	0.003	— —
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°
θ1	15°	19°	15°	19°
θ2	11°	15°	11°	15°

MSOP (8)



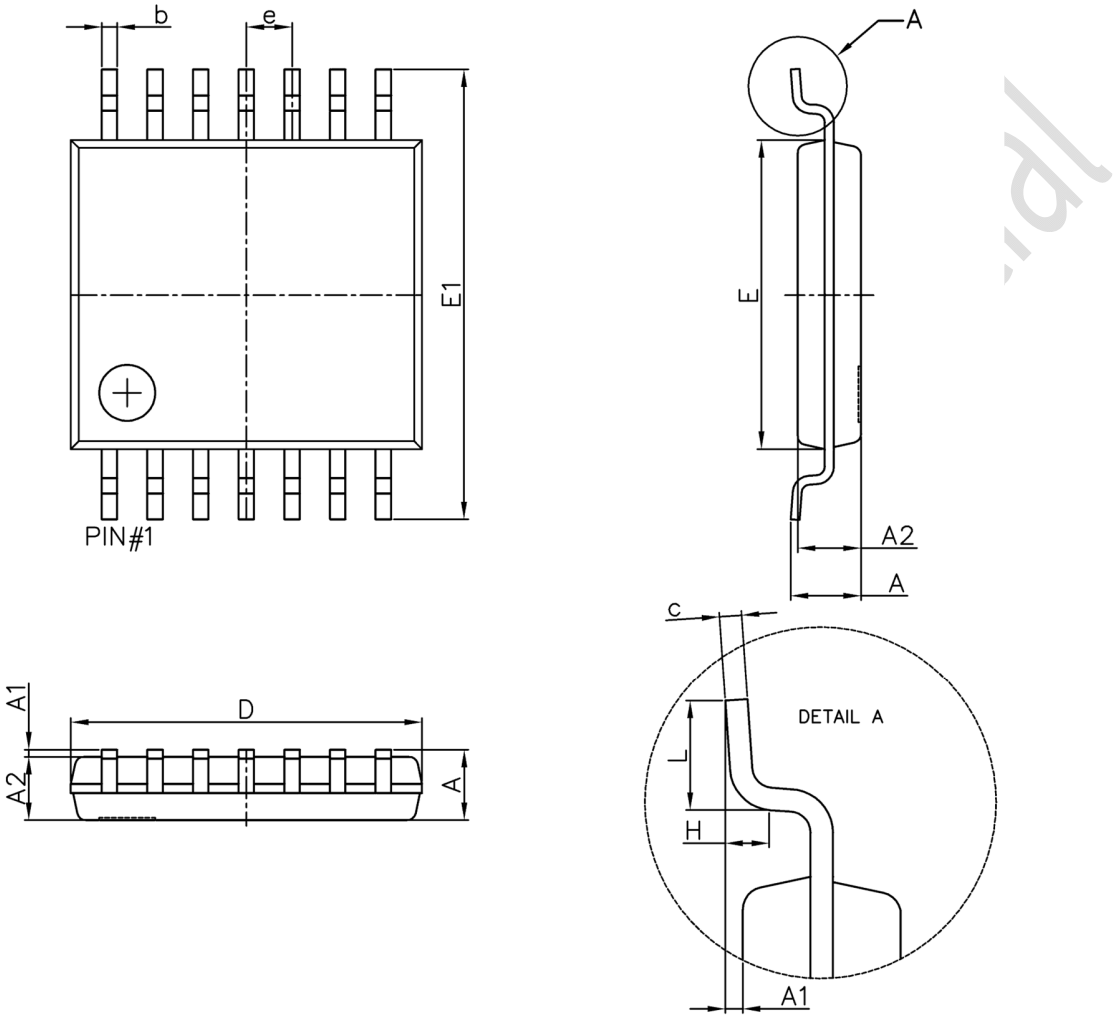
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.10	— —	0.043
A1	0.05	0.15	0.002	0.006
A2	0.75	0.95	0.030	0.037
A3	0.30	0.40	0.012	0.016
b	0.25	0.38	0.010	0.015
b1	0.24	0.33	0.009	0.013
c	0.15	0.20	0.006	0.008
c1	0.14	0.16	0.006	0.0062
D	2.90	3.10	0.114	0.122
E	4.75	5.05	0.187	0.199
E1	2.90	3.10	0.114	0.122
e	0.55	0.75	0.022	0.030
L	0.40	0.70	0.016	0.028
L1	0.95REF		0.037(BSC)	
L2	0.25BSC		0.010	
R	0.07	— —	0°	8°
R1	0.07	— —	0.003	— —
θ	0°	8°	0°	8°
θ1	9°	15°	9°	15°

SOIC (14)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.1	0.25	0.004	0.01
A2	1.25	— —	0.049	— —
b	0.31	0.51	0.012	0.02
c	0.1	0.25	0.004	0.01
D	8.45	8.85	0.333	0.348
E	5.8	6.2	0.228	0.244
E1	3.8	4	0.15	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.4	0.016	0.016	0.05
θ	0°	0°	0°	8°

TSSOP (14)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.9	5.1	0.193	0.201
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A	—	1.2	—	0.047
A2	0.8	1	0.031	0.039
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

6. ORDER INFORMATION

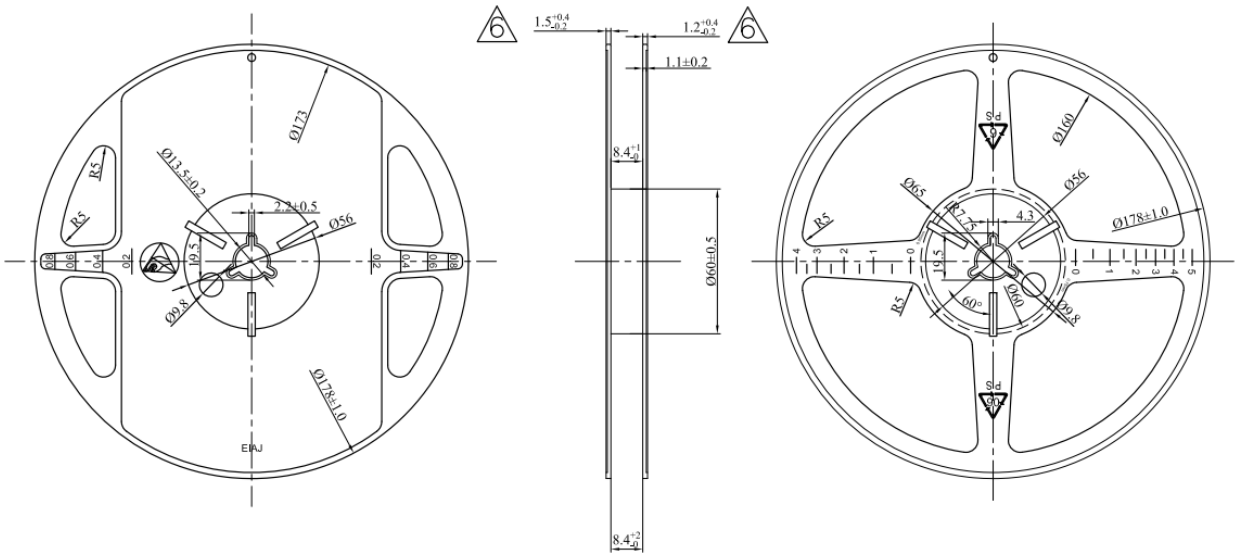
Part Number	*Package*	*MSL Level*	*Op Temp (°C)*
NSOPA9051-DSTAR	SOT-23 (5)	1	-40~+125
NSOPA9051-DSPR	SOIC (8)	1	-40~+125
NSOPA9052-DSPR	SOIC (8)	1	-40~+125
NSOPA9052-DMSR	MSOP (8)	1	-40~+125
NSOPA9054-DSPKR	SOP (14)	1	-40~+125
NSOPA9054-DTSKR	TSSOP (14)	1	-40~+125

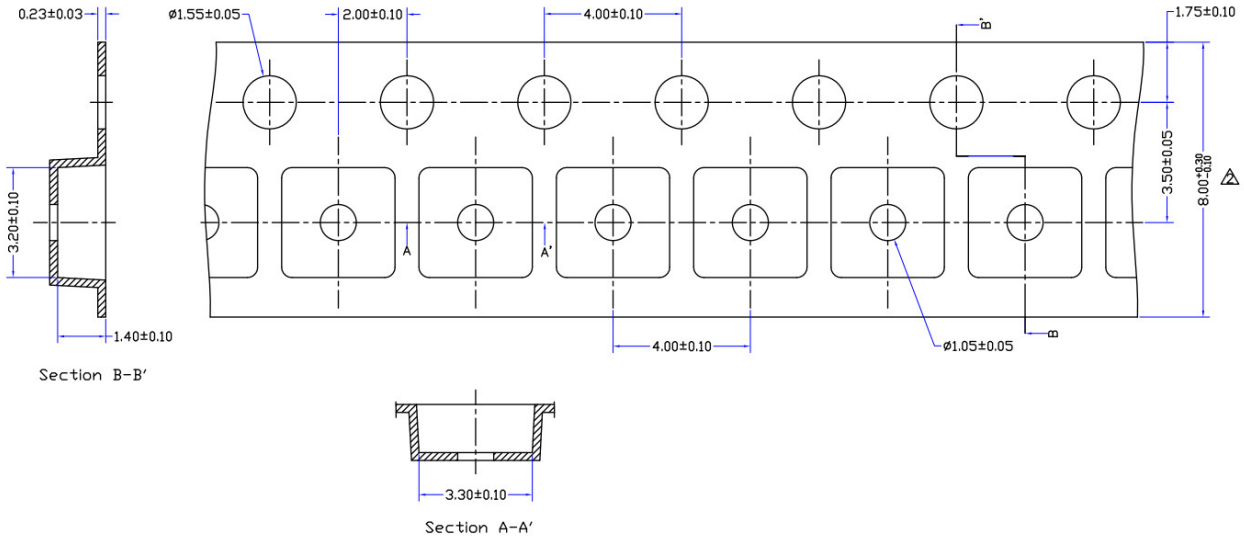
7. DOCUMENTATION SUPPORT

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NSOPA9051-DSTAR	TBD	TBD	TBD
NSOPA9051-DSPR	TBD	TBD	TBD
NSOPA9052-DSPR	TBD	TBD	TBD
NSOPA9052-DMSR	TBD	TBD	TBD
NSOPA9054-DSPKR	TBD	TBD	TBD
NSOPA9054-DTSKR	TBD	TBD	TBD

8. TAPE AND REEL INFORMATION

SOT-23(5)

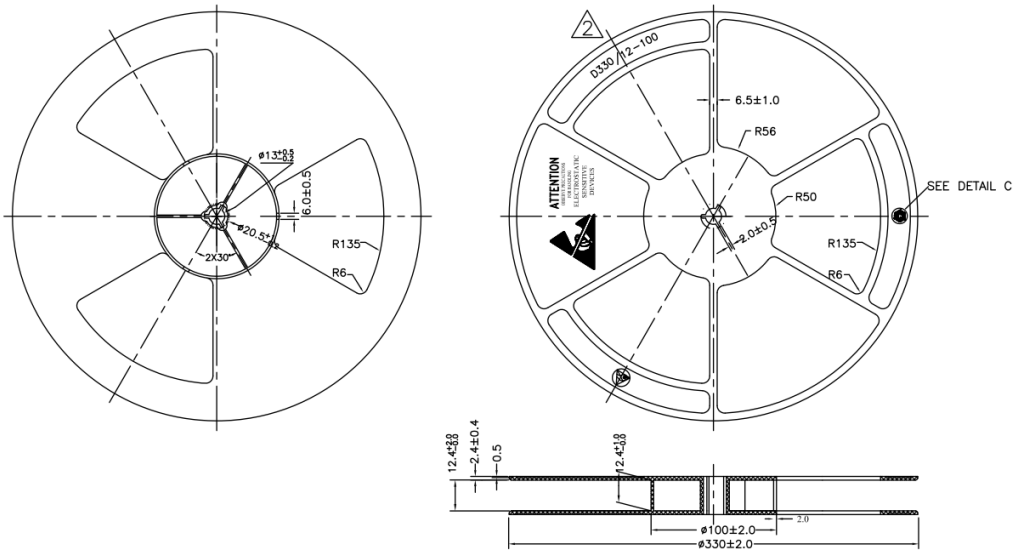


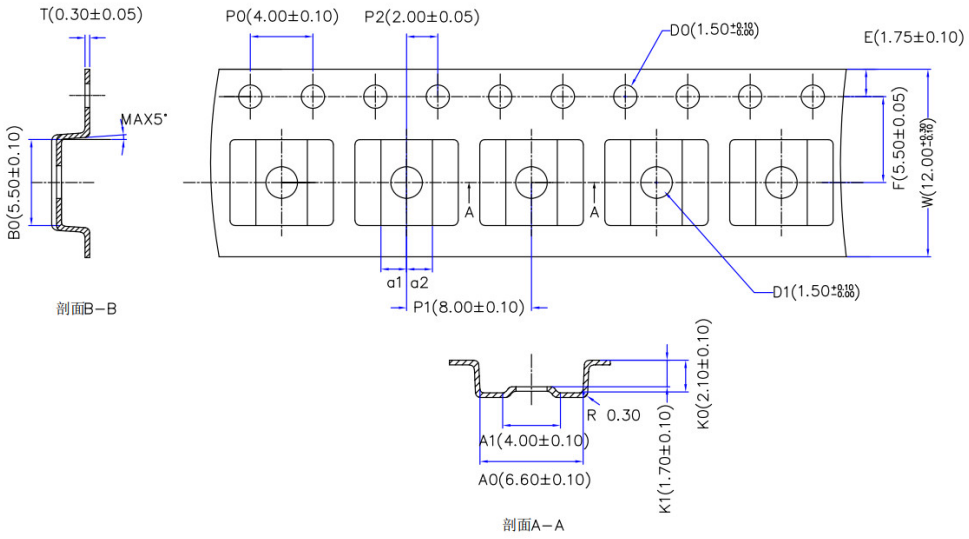


Note:

1. 3000ea/reel
2. Unit:mm

SOIC(8)

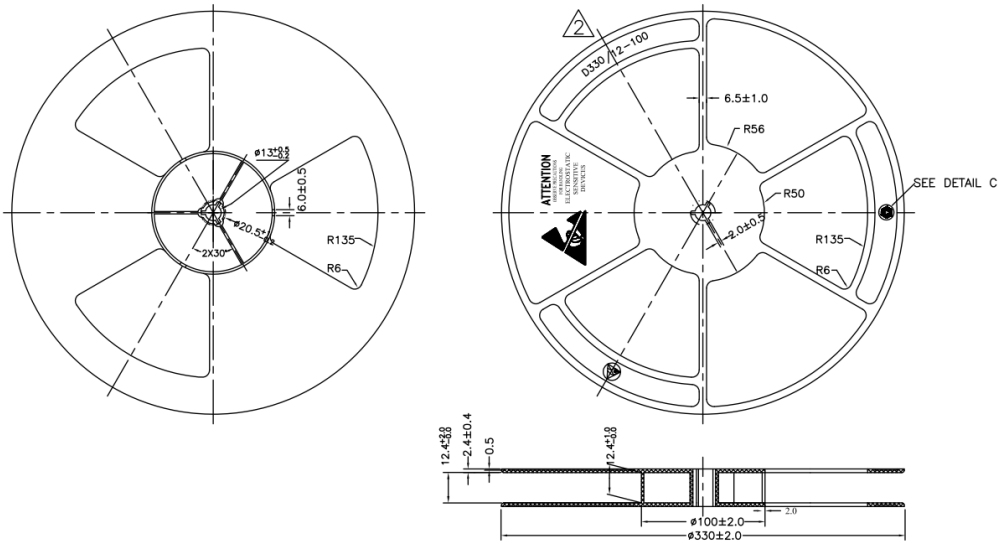


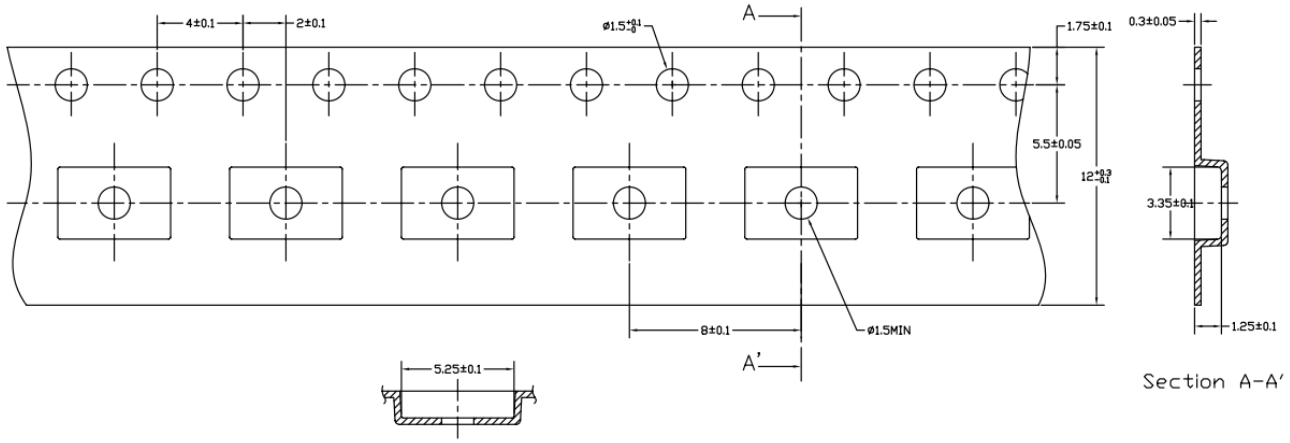


Note:

1. 3000ea/reel
2. Unit:mm

MSOP(8)

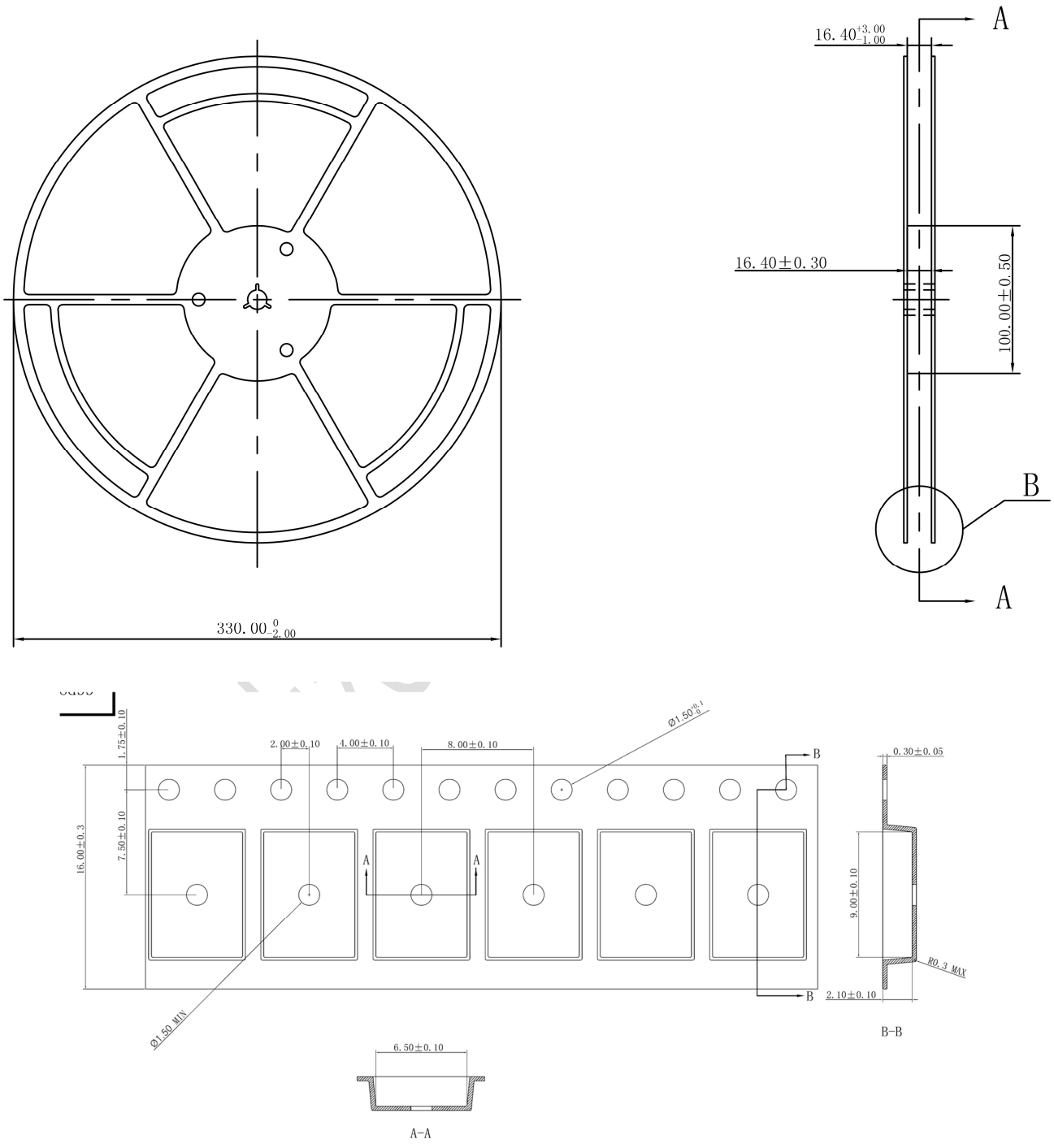




Note:

1. 3000ea/reel
2. Unit:mm

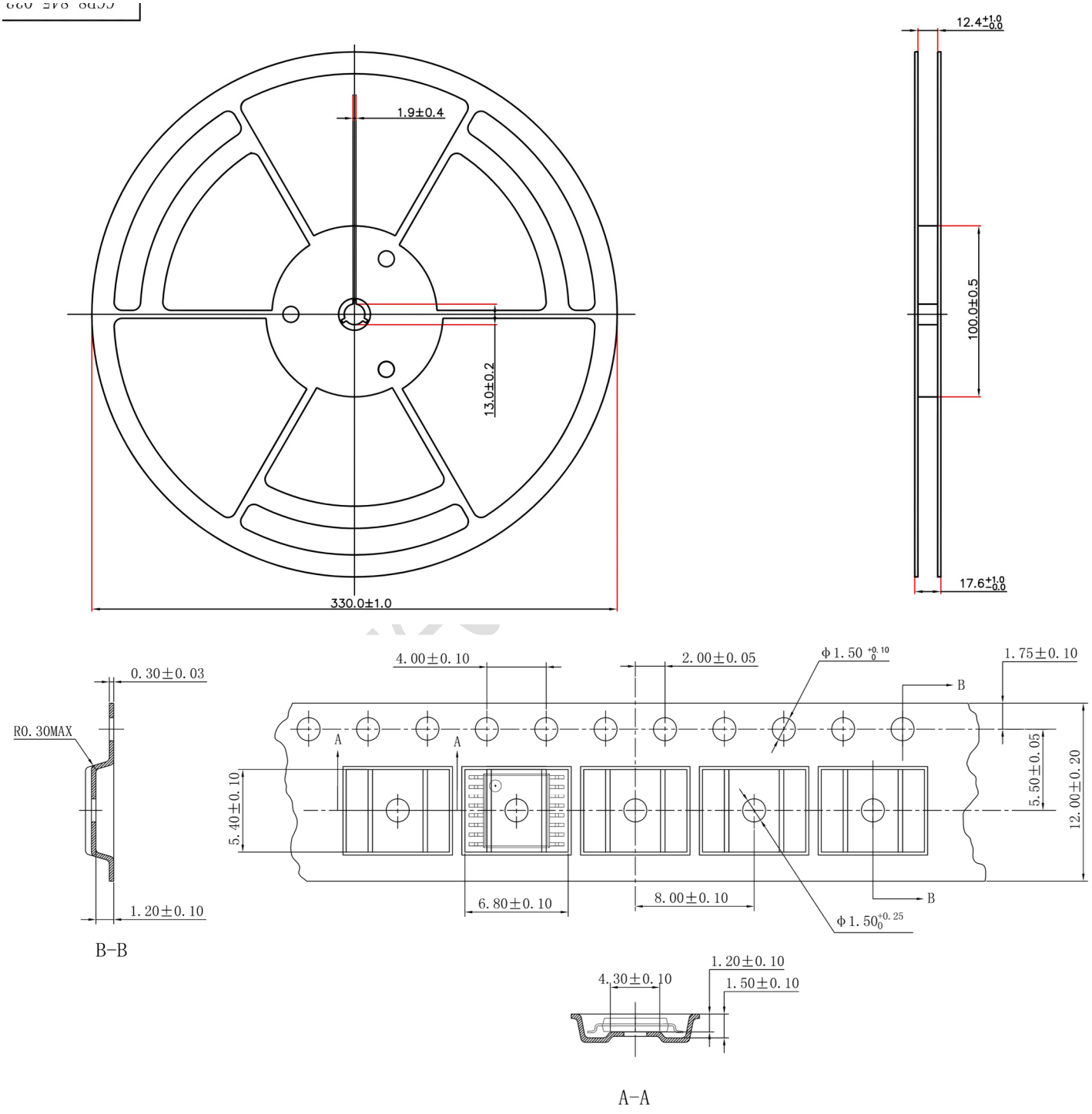
SOIC (14)



Note:

1. 3000ea/reel
2. Unit:mm

TSSOP (14)



Note:

1. 3000ea/reel
2. Unit:mm

9. REVISION HISTORY

Revision	Description	Date
0.1V	Initial version	2023/09

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