NST175

0.5°C Accurate Temperature Sensor With SMBus and I²C Interface

Datasheet (EN) 1.31

Description

The NST175 is a lower power, higher accuracy digital temperature sensors. It's an idealsubstitutes that substitute for negative temperature coefficient (NTC) and positive temperature coefficient (PTC) thermistor. NST175 Compatible with SMBus and I²C interfaces, supports up to 27 devices address and provides SMBus Reset and Alert function. The NST175 also feature a SMBus Alert function. without requiring calibration or external component signal conditioning, the typical accuracy of NST175 is 0.5 °C. The NST175 temperature sensor is a highly linear device, without require complex calculations or look-up tables to derive the temperature. Using a high resolution (12bit) analog-to-digital converter (ADC), the NST175 resolutions are down to 0.0625°C. NST175 device works over a temperature range of –55°C to 125°C, which makes it suitable for onboard and off board applications in automotive, industrial, and consumer markets. The NST175 is very low power device, which can be applied in IoT. The NST175 is available in a SOP (8) package and an MSOP (8) package.

Key Features

- High Accuracy Over –55°C to 125°C Wide Temperature Range
  - -20 °C ~ 85 °C: ±0.5 °C (Typical)
  - -20 °C ~ 85 °C: ±1 °C (Maximum)
  - -55 °C ~-20 °C: ±2 °C (Maximum)
  - 85 °C ~125 °C: ±2 °C (Maximum)
- Proportional to Temperature with 0.0625°C Resolution
- Power up Defaults Permit Stand-Alone Operation as Thermostat
- Supports up to 27 Device Addresses
- Supply Operation range from 1.62V to 5.5V
- Operating current: 30 µA (Typical)
- Shutdown current: 0.1 µA (Typical)
- Digital Interface: SMBus, I²C
- Package
  - MSOP (8) (3mm x 3mm)
  - SOP (8) (4.9mm x 3.91mm)

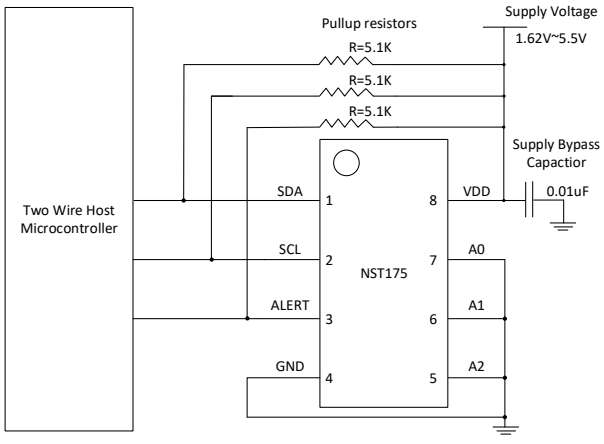
Applications

- General System Thermal Management
- Computer Thermal Protection
- Portable Computers
- Industrial Internet of Things (IoT)
- Communications Infrastructure
- Power-system monitors
- Thermal protection
- Environmental Detection and HVAC

Device Information

Part Number	*Package*	*Body Size*
NST175	MSOP (8)	3.00mm × 3.00mm
	SOP (8)	4.90mm × 3.91mm

Typical Application



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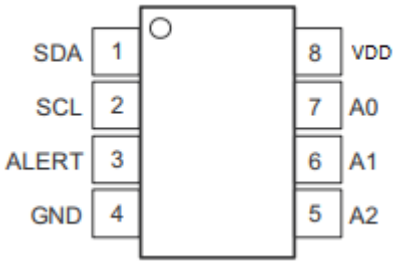
PIN CONFIGURATION AND FUNCTIONS



NST175 Function Top View

Pinout		Type	Description
NO	Name.		
1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor
2	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
3	ALERT	O	Over temperature alert. Open-drain output; requires a pullup resistor.
4	GND	GND	Ground
5	A2	I	Address selected. Connect to GND, VDD or leave these pins floating.
6	A1		
7	A0		
8	VDD	Power	Supply voltage, 1.62 V to 5.5 V

1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage Pin (VDD)	VDD	-0.3		6.5	V	
Voltage at A0, A1and A2 Pins	A0, A1, A2	-0.3		6.5	V	
Voltage at OS, SCL and SDA Pins	ALERT, SCL, SDA	-0.3		6.5	V	
Storage temperature		-60		155	°C	
Operation temperature	$TB_{operation}$	-55		125	°C	
Maximum junction temperature				155	°C	
ESD susceptibility	HBM	±5			KV	
	CDM	±1			KV	

2.0 ELECTRICAL CHARACTERISTICS

2.1 Electrical characteristics

At T_A = +25°C and VDD = +1.62V to +5.5V, unless otherwise noted.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply						
Supply voltage Range	VDD	1.62	3.3	5.5	V	
Pull up resistor Range	R_{pu}	0.5	5	10	KΩ	
Supply sensitivity			16		m°C /V	
Operation current	R_{CONV}		30	60	μA	Conversion
Shutdown current	ISD		0.1		μA	Serial bus inactive
	ISD		10		μA	Serial bus active, SCL frequency = 400 kHz
Temperature Range and Resolution						
Temperature Range		-55		125	°C	
Resolution			0.0625		°C	
Accuracy		-1	±0.5	1	°C	From -20°C to 85°C
		-2		2	°C	From -50°C to -20°C
		2		2	°C	From 85°C to125°C
Conversion time	T_{CONV}		24	32	ms	For VDD<2V, the max conversion time 64 ms.

ALERT Output Saturation Voltage				0.5	V	IOUT = 4 mA
ALERT Delay		1		6	conversion	
High limit Default Temperature	T_H		80		°C	
Low limit Default Temperature	T_L		75		°C	
Time out time	$T_{TIMEOUT}$		54		ms	
Digital DC Characteristics						
VIN(1) Logical "1" Input Voltage	VH	VDD*0.7		VDD+0.3	V	
VIN(0) Logical "0" Input Voltage	VL	-0.3		VDD*0.3	V	
IIN(1) Logical "1" Input Current				1	μA	
IIN(0) Logical "0" Input Current				-1	μA	
CIN All Digital Inputs	C_{IN}		5		pF	
I_{OH} High Current Level Output Open drain leakage	I_{OH}			1	μA	VOH=5V
Low Level Output Voltage	V_{OL}			0.4	V	IOL= 3 mA
Thermal response						
Stirred oil thermal response time to 63% of final value (package only)			0.75		s	MSOP (8)
Drift						
Drift (1)			0.1		°C	

Notes： (1). Drift data is based on a 1000-hour stress test at +125°C with VDD = 5.5V.

2.2 I²C Timing Diagram

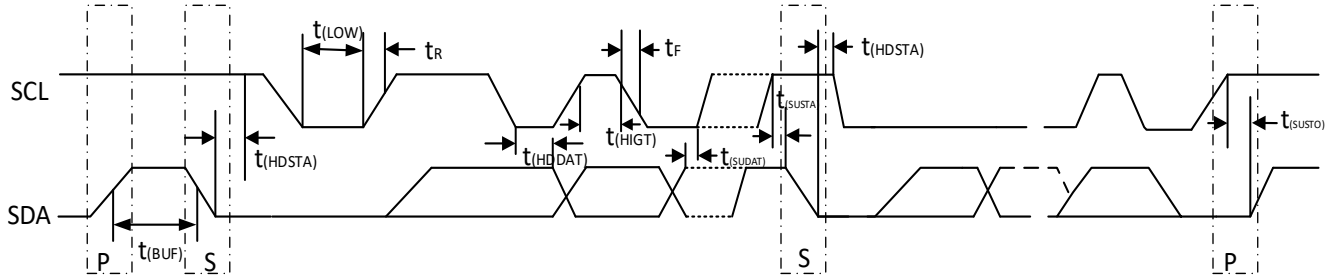


Figure 2.1 I²C Timing Diagram

2.3 I²C Timing characteristics

At T_A = +25°C and VDD = +1.62V to +5.5V, unless otherwise noted.

Parameters	Symbol	STARDARD MODE		FAST MODE		HIGH-SPEED MODE		Unit	Comments
		Min	Max	Min	Max	Min	Max		
SCL operating frequency	F_{SCL}	0.001	0.1	0.001	0.4	0.001	2	MHz	
Bus-free time between STOP and START conditions	$t_{(BUF)}$	4.7	-	1300	-	160	-	ns	
Hold time after repeated START condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4000	-	600	-	160	-	ns	
Repeated START condition setup time	$t_{(SUSTA)}$	4700	-	600	-	160	-	ns	
STOP condition setup time	$t_{(SUSTO)}$	4000	-	600	-	160	-	ns	
Data hold time	$t_{(HDDAT)}$	0	3450	4	900	4	120	ns	
Data setup time	$t_{(SUDAT)}$	250	-	100	-	10	-	ns	
SCL clock low period	$t_{(LOW)}$	4700	-	1300	-	280	-	ns	
SCL clock high period	$t_{(HIGH)}$	4000	-	600	-	60	-	ns	
Data fall time	t_{FD}	-	300	-	300	-	150	ns	
Clock rise time	t_{RC}	-	1000	-	300	-	40	ns	
		-	1000	-	1000	-	-	ns	SCL≤100kHz
Clock fall time	t_{FC}	-	300	-	300	-	40	ns	

Notes:

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{(HDDAT)}$ has only to be met if the device does not stretch the LOW period ($t_{(LOW)}$) of the SCL signal.
3. A Fast-mode I²C-bus device can be used in a Standard-mode I²C -bus system, but the requirement $t_{(SUDAT)}$ >250 ns must then be

met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.

If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max

+ $t_{(SUDAT)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C -bus specification) before the SCL line is released.

2.4 Typical Characteristics

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

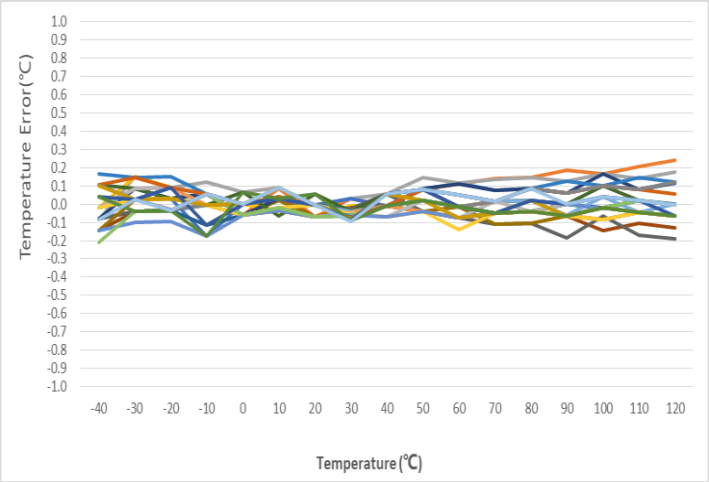


Figure 2.2 Temperature Error VS Temperature (MSOP (8))

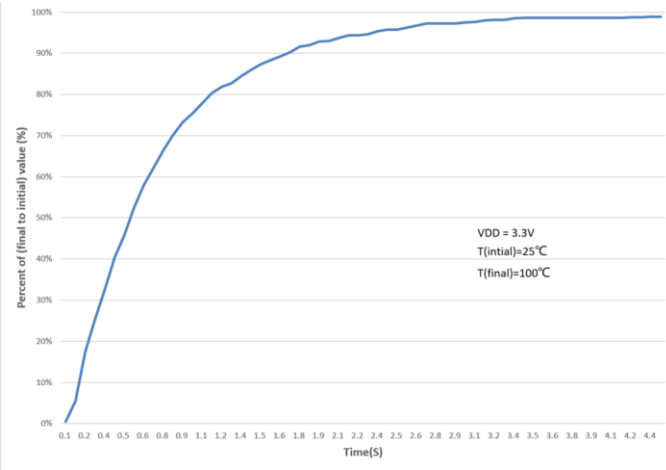


Figure 2.3 Temperature Response in stilling Oil (MSOP (8))

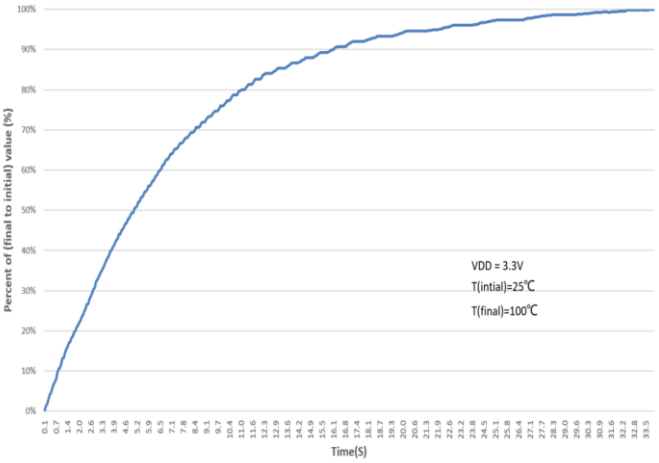


Figure 2.4 Temperature Response in stilling Air (MSOP (8))

3.0 FUNCTION DESCRIPTION

3.1 Function description

NST175 temperature sensor incorporates a bandgap type temperature sensor and 12-bit ADC ($\Sigma-\Delta$ ADC). NST175 temperature data is available at all times via the I^2C bus. NST175 also incorporates a digital comparator that compares a series of readings (the number of which can be selected by the user) with user-programmable setpoint and hysteresis values. The comparator triggers the ALERT pin state, which is programmable for mode and polarity. NST175 has an integrated low-pass filter on both the SDA and SCL lines. These filters increase communication reliability in noisy environments.

The NST175 has a bus fault timeout function. If the SDA and SCL line is held low for longer than $T_{TIMEOUT}$ (see specification), the NST175 will reset to the IDLE state (SDA and SCL set to high impedance) and wait for a new start condition. The TIMEOUT feature is not functional in Shutdown Mode.

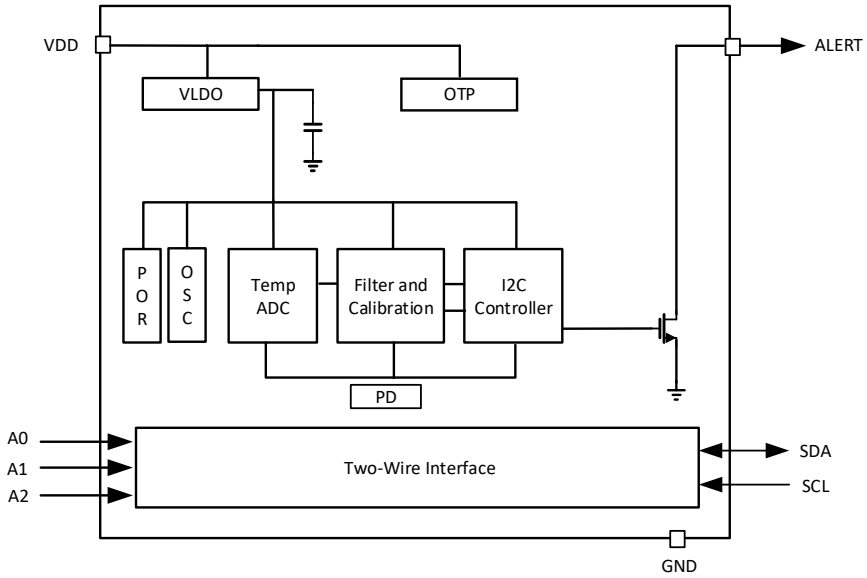


Figure 3.1 NST175 Functional Block Diagram

3.2 Feature Description

3.2.1 Digital Temperature Sensor

With an integrated sigma-delta ADC and I^2C interface, the NST175 is a digital temperature sensor, comply with industrial standards. The NST175 output 12-bit digital temperature value. In the range of –25 °C to 85 °C, the typical accuracy is ± 0.5°C. In the range of –55 °C to 125 °C the typical accuracy is ± 2 °C.

The NST175 has a wide supply voltage range of 1.62 V to 5.5 V. Communication with master through SDA and SCL lines, fast mode can reach 400kHz, high speed can reach 2MHz. On the same 2-wire bus, the NST175 allows up to 27 devices, by three address pins. The NST175 has special over temperature output, programmable high temperature limit and low temperature limit. The over-temperature output is programmable and fault tolerant, allowing the user to define the conditions under when the alert is triggered by setting the number of consecutive over-temperature points.

The temperature digital output is stored in the read-only Temperature register after each temperature measurement conversion. The Temperature register of the NST175 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are listed in Table 3.5 and Table 3.6. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits are used to indicate temperature. The data format for temperature is listed in Table 3.1. One LSB equals 0.0625 °C. Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

Table 3.1. Temperature Data Format

TEMPERATURE (°C)	12bit format	
	BINARY	HEX
150	0111 1111 1111 (0000)	7FF0
128	0111 1111 1111 (0000)	7FF0
127.9375	0111 1111 1111 (0000)	7FF0
100	0110 0100 0000 (0000)	6400
85	0101 0101 0000 (0000)	5500
50	0011 0010 0000 (0000)	3200
20	0001 0100 0000 (0000)	1400
0.125	0000 0000 0010 (0000)	0020
0	0000 0000 0000 (0000)	0000
-0.125	1111 1111 1110 (0000)	FFE0
-20	1110 1100 0000 (0000)	EC00
-50	1100 1110 0000 (0000)	CE00

3.2.2 Serial Interface

NST175 is compatible with SMBus and I2C interfaces, and transmits information to the master through two lines, SDA and SCL. NST175 has 27 slave addresses, which can support the simultaneous use of 27 NST175 slaves on the bus, data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 2.0 Mbit/s in the High-speed mode. All data bytes are transferred MSB-first.

3.2.2.1 Bus Overview

The device on the bus that initiates the transmission is referred to as the master device, and the devices controlled by the master are slaves. The bus has a master, which controls the generation of the clock (SCL) and the generation of the START and STOP signals.

Pulling the data line (SDA) from a logical high to a logical low when SCL is high indicates the initiation of a START condition, and all slaves on the bus are shifted into the slave address byte, with the last bit indicating that the master intends to perform a read or write operation. During the ninth clock pulse, the addressed slave responds to the master by generating an acknowledge signal and pulling SDA low. Then the data transfer starts with 8 clock pulses and a acknowledge bit. During data transfer, SDA must remain stable when SCL is high, because any change in SDA when SCL is high will be interpreted as a control signal.

When the data transfer is finished, pull SDA high when SCL is high to generate a stop signal.

3.2.2.2 Serial Bus Address

For communication between the master and the slave, a byte address needs to be sent first, including 7bit slave address bits and 1bit read and write direction bits. NST175 has three ADDR pins, and 27 different addresses can be obtained through different connections of this pin. Table 3.2 describes the pin logic levels used to properly connect up to 27 devices.

Table 3.2. Address Pins and Slave Addresses for the NST175

A0	A1	A2	SLAVE ADDRESS
0	0	0	1001000
1	0	0	1001001
0	1	0	1001010
1	1	0	1001011
0	0	1	1001100
1	0	1	1001101
0	1	1	1001110
1	1	1	1001111
0	0	Float	1110000
Float	0	Float	1110001
1	0	Float	1110010
0	1	Float	1110011
Float	1	Float	1110100
1	1	Float	1110101
0	Float	Float	1110110
1	Float	Float	1110111
0	Float	0	0101000
1	Float	0	0101001
0	Float	1	0101010
1	Float	1	0101011
Float	0	0	0101100
Float	1	0	0101101
Float	0	1	0101110
Float	1	1	0101111
Float	Float	0	0110101
Float	Float	1	0110110
Float	Float	Float	0110111

3.2.2.3 Writing and Reading to the NST175

Writing is done by sending the slave address in write mode (R/$\overline{W}$=0), then the master sends pairs of register addresses and register data. The transaction is ended by a stop condition. The configuration registers, T_{HIGH}, and T_{LOW} registers of NST175 can be written to specific values.

To be able to read registers, first the register address must be sent in write mode (R/$\overline{W}$=0), then either a stop or a repeated start condition must be generated. After this the slave is addressed in read mode (R/$\overline{W}$=1), after which the slave sends out 2 bytes temperature data. After reading two bytes of temperature data the master needs to generate the NACK and stop

condition to end the transaction. If the user does not care about the temperature value of the decimal part, a NACK and stop condition is needed to end the transaction after the first byte. The details of this sequence are shown in Figure 3.5.

If repeated reads from the same register are required, it is not necessary to send the pointer register byte repeatedly because the NST175 remembers the pointer register value until it is changed by the next write operation. Register bytes are sent MSB first, followed by the LSB.

3.2.2.4 Slave mode operations

The NST175 can be used as a slave receiver or slave transmitter.

3.2.2.4.1 Slave Receiver Mode

The master transfers the slave address byte firstly, including 7bit address bits and 1bit write direction bits, NST175 acknowledges after receiving the valid address. the second byte transmitted by master is the pointer register address, then NST175 acknowledges and the next byte or several bytes of data is written to the pointer register. The master can terminate communication by generating a START or STOP condition.

3.2.2.4.2 Slave Transmitter Mode

The master transfers the slave address byte firstly, including 7bit address bits and 1bit read direction bits, NST175 acknowledges after receiving the valid address. The second byte is transmitted by the slave and is the MSB of the data in the register indicated by the pointer register, and the master acknowledges receipt of the data byte. The next byte transmitted by the slave is the LSB of the data, and the master acknowledges receipt of that data byte. The master can generate not-acknowledges after any data byte to terminate the transmission, or a START or STOP condition.

3.2.2.5 SMBus Alert Function

When the NST175 is operating in interrupt mode (TM=1), the NST175 supports the SMBus Alert function, the ALERT pin of the NST175 can be connected as a SMBus Alert signal. When the master monitors that the alert is active, the master can send the SMBus alert command (00011001) on the bus, if the ALERT pin of the NST175 is active, the device responds to the SMBus Alert command by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether a temperature above T_{HIGH} or below T_{LOW} has caused an ALERT condition: this bit is high if the temperature is greater than or equal to T_{HIGH}. the bit is low if the temperature is less than T_{LOW}. The details of this sequence are shown in Figure 3.6.

If multiple slaves respond to the SMBus alert command issued by the master, the SMBus alert arbiter will arbitrate to determine which slave to clear the alert status. The one with the lowest slave address wins the arbitration. If the NST175 wins arbitration, the alert pin of NST175 activation status is cleared at the end of the SMBus alert command; if the NST175 loses arbitration, the alert activation status is not cleared.

3.2.2.6 General Call

The NST175 responds to the general call address (0000 000) if the eighth bit is 0. The device acknowledges the general call address and responds to the second byte of the command. If the second byte is 00000110, the NST175 latches the state of its address pins and resets its internal registers to the value at power-up.

3.2.2.7 High-Speed Mode

The NST175 supports bus operation above 400 kHz, requiring that the master device must switch the bus to high-speed mode operation by issuing a high-speed mode master code (00001XXX) in the first byte after the START condition. The NST175 do not acknowledge this byte, the NST175 switches the input filter of SCL, SDA and output filter of SDA to high-speed mode, allowing data transfer at up to 2 MHz (for VDD<1.8V, Hs mode is up to 1.6 MHz). After issuing the master code for high-speed mode, the master then transmits a two-wire slave address to initiate the data transfer operation. The bus will continue to operate in high-speed mode until a stop signal appears on the bus. Once the stop signal is received, the SCL, SDA input filter and SDA output filter of the NST175 switch to the fast mode.

3.2.2.8 Time-out Function

The NST175 resets the I²C interface when the SCL or SDA is continuously pulled low for 54ms (typical) between the start and stop signals, the NST175 release the SDA and SCL line and waits for the master to initiate a START condition. To avoid activating the timeout function, the SCL operating frequency must be maintained at a rate of at least 1kHz.

3.2.3 I²C Timing Diagram

The NST175 devices are SMBus, and I²C interface-compatible. Figure 3.2 to Figure 3.6 describe the various operations on the NST175. The following list provides bus definitions. Parameters for Figure 3.2 are defined in the *Timing Requirements*. Bus definitions are:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The termination of each data transfer can be done with a RESTART or STOP.

Data Transfer: The amount of data bytes transferred between START and STOP is controlled by the master and is unlimited. The receiver acknowledges the transfer of data.

Acknowledge: Each slave is obliged to generate an acknowledge bit when the address is matched. The slave must pull down SDA during the low-level period of the acknowledge signal cycle and keep it stable during the high-level period of the acknowledge signal cycle. Both establishment time and hold time should be fully considered. The data transfer can be terminated by the host generating a not-acknowledge during the host receiving data.

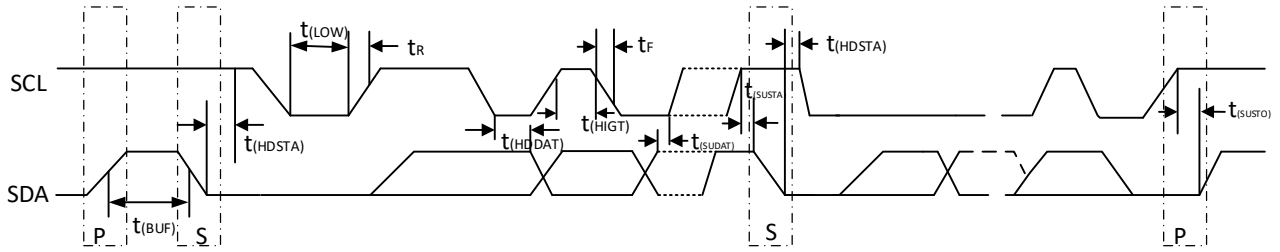
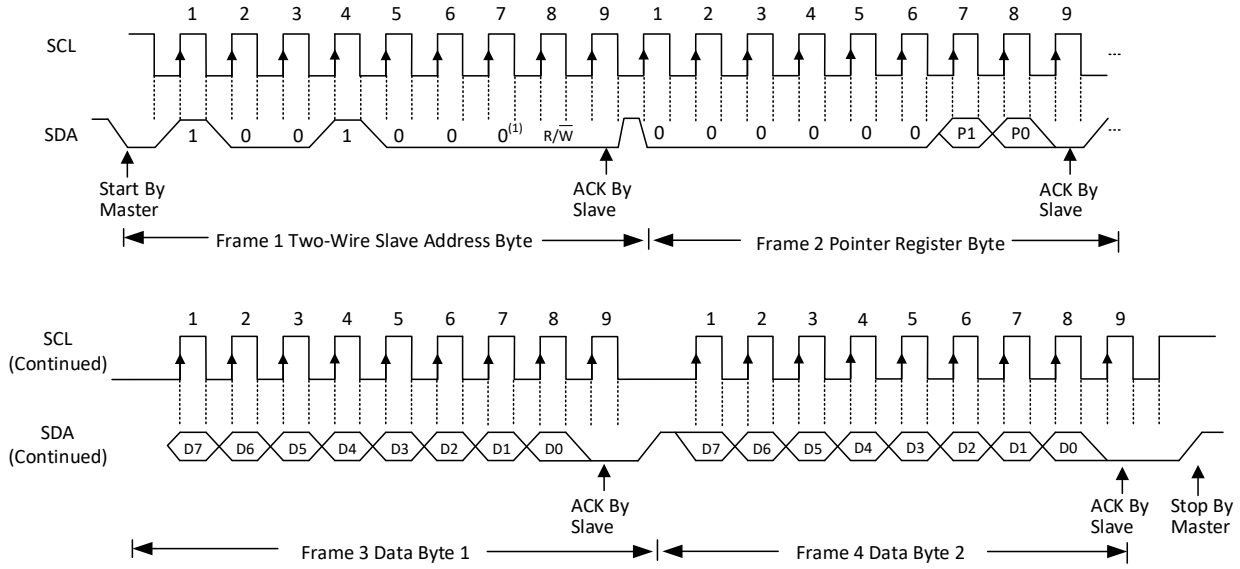
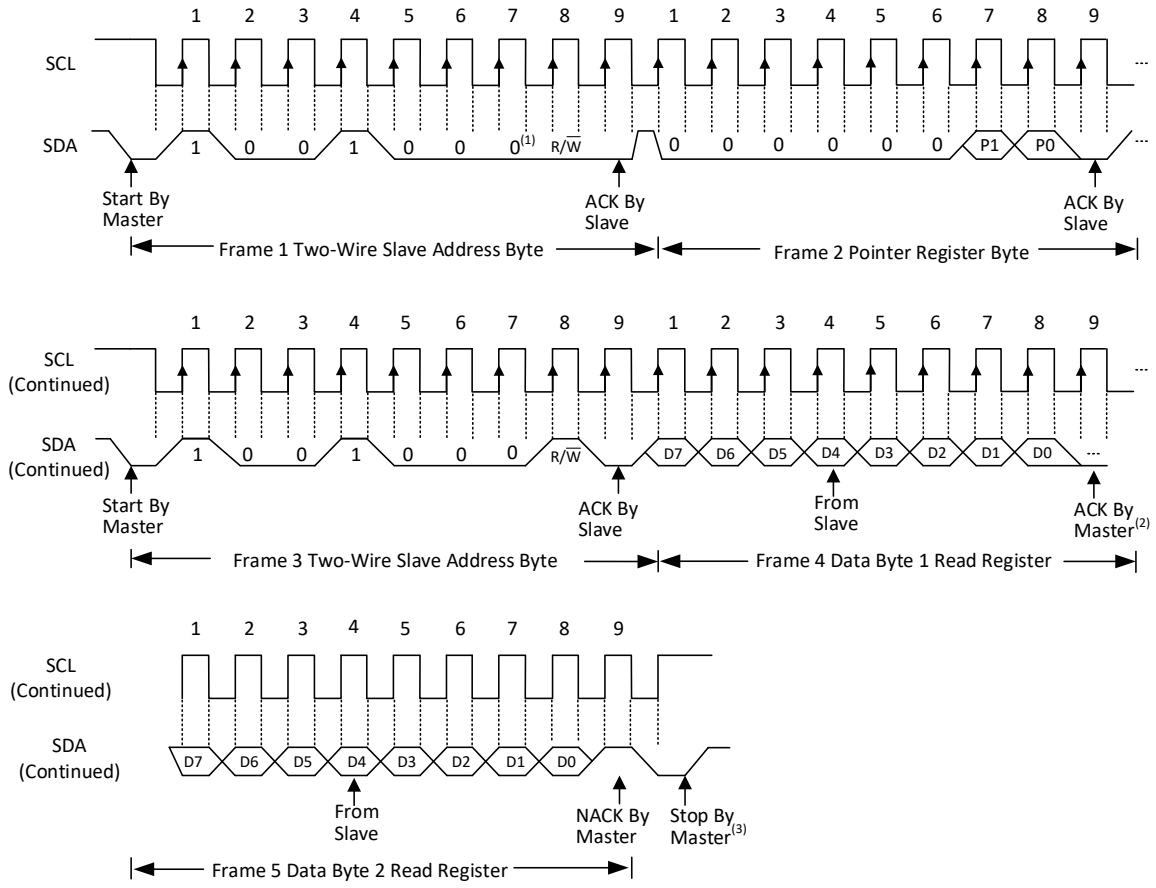


Figure 3.2. I²C Timing Diagram



(1) Slave address 1001000 is shown.

Figure 3.3. I²C Timing Diagram for the NST175 Write Word Format



(1) Slave address 1001000 is shown.

(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 3.4. I²C Timing Diagram for Read Word Format

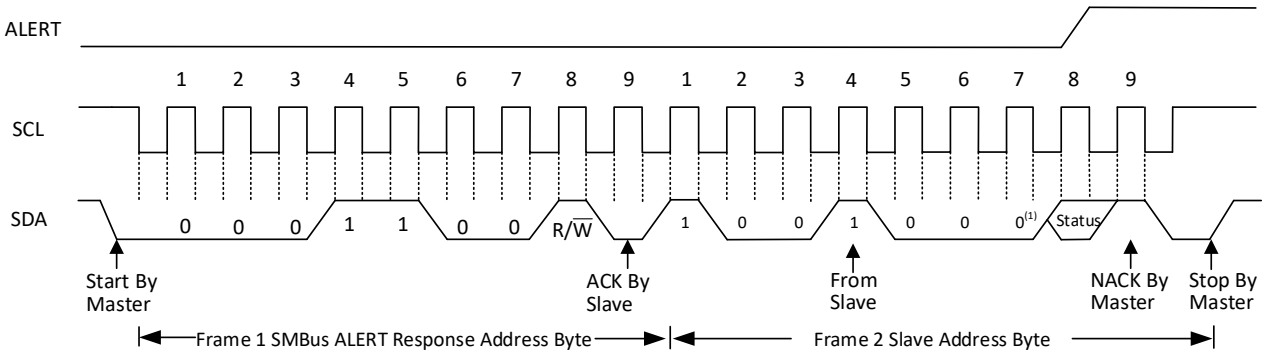


Figure 3.6. Timing Diagram for SMBus ALERT

3.3 Device Functional Modes

3.3.1 Shutdown Mode (SD)

The NST175 device supports a shutdown mode that lets the user to maximize power consumption savings by turning off all device circuitry other than the serial interface, which reducing current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; in SD mode an OS command can be sent to perform a temperature transition, and the device shuts down when the temperature transition is complete. When SD is equal to 0, the device maintains a continuous conversion state.

For the NST175, the TIMEOUT feature is turned off in Shutdown Mode.

3.3.2 One-shot (OS)

The NST175 supports a one-shot temperature opration mode when continuous temperature monitoring is not required. First set the chip into shutdown mode, write 1 to the OS bit to wake up the chip once and perform a temperature conversion. When temperature conversion is in progress, OS bit is 0. After the single conversion is complete, the device returns to the Shutdown state. At the end of the conversion, the OS bit reads 1.

Using one shot mode can achieve faster conversion frequency, temperature conversion takes 24ms typically, and reading the temperature value needs less than 20us, so using one shot can achieve more than 30 temperature conversions per second.

3.3.3 Thermostat Mode (TM)

The thermostat mode bit can be configured to make the NST175 work in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

3.3.3.1 Comparator Mode (TM = 0)

In comparator mode (TM=0), when the test temperature is equal to or higher than the T_{HIGH} register value, the alert pin is activated until the measured temperature is below the T_{LOW} register value. In *High and Low Limit Registers* section, there is more information of the comparator mode.

3.3.3.2 Interrupt Mode (TM = 1)

With the NST175 in interrupt mode, the alert pin is activated when the test temperature value is above T_{HIGH} or below T_{LOW}. and the alert state is cleared when the master reads the temperature register. In *High and Low Limit Registers* section, there is more information of the comparator mode.

3.4 Programming

3.4.1 Pointer Register

The 8-bit pointer register is used to address a given data register, and the three LSBs of the pointer register determine which data register responds to a read or write operation by the master. Figure 3.7 shows the internal register structure of the NST175. The default value of pointer register P2/P1/P0 after power on is "000", that is, the default state of the NST175 pointer register is the temperature register. Table 3.3 identifies the bits of the pointer register byte. Table 3.4 describes the pointer addresses of the registers available in the NST175. Bytes P3 through P7 must always be 0 during the write command.

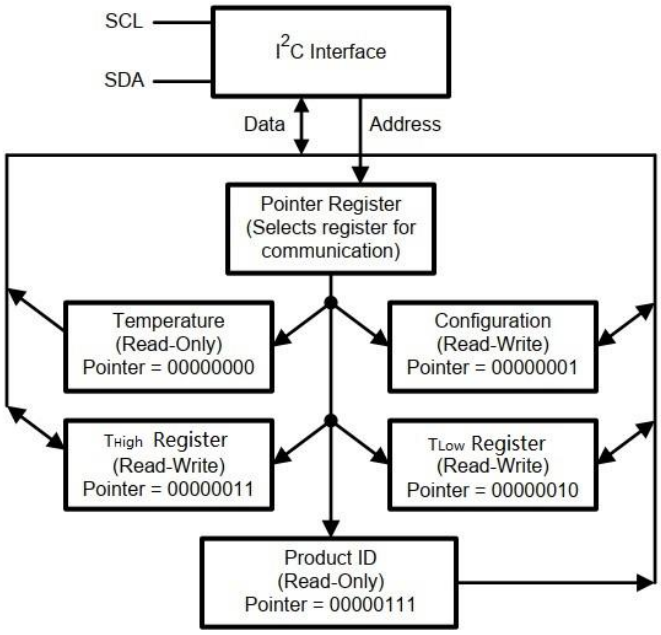


Figure 3.7. Internal Register Structure of the NST175

3.4.1.1 Pointer Register Byte (pointer = N/A) [reset = 00h]

Table 3.3. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register bit		

3.4.1.2 Pointer Addresses of the NST175

Table 3.4. Pointer Addresses of the NST175

P2	P1	P0	TYPE	REGISTER
0	0	0	R only default	Temperature register
0	0	1	R/W	Configuration register
0	1	0	R/W	TLOW register
0	1	1	R/W	THIGH register
1	1	1	R only	Product ID Register

3.4.2 Temperature Register

The temperature register of NST175 is a 12bit read-only register for storing the results of each completed temperature conversion, which consists of 2bytes in the format shown in Table 3.5 and Table 3.6, with MSB output first and followed by the LSB, and 12bits MSBs used to indicate the temperature value. After power-up or reset and before the first temperature conversion is completed, the value of the temperature register is 0.

Table 3.5. Byte 1 of the Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T11	T10	T9	T8	T7	T6	T5	T4

Table 3.6. Byte 2 of the Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	T3	T2	T1	T0	0	0	0	0

3.4.3 Configuration Register

The configuration register of the NST175 is an 8-bit read/write register used to store the control bits that control the NST175 into different operation modes, and the read/write operation is executed with MSB priority. Table 3.7 lists the configuration register format, power-up and reset values. All registers are updated byte by byte.

Table 3.7. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD
Default	0	0	0	0	0	0	0	0

3.4.3.1 Shutdown Mode (SD)

The shutdown mode of NST175 lets the user to maximize power consumption savings by turning off all device circuitry other than the serial interface, which reducing current consumption to typically less than 0.1 μA. When this SD bit is set to 1, the shutdown mode is active; in SD mode an OS command can be sent to perform a temperature transition, and the device shuts down when the temperature transition is complete. The device can keep a continuous conversion mode with the SD bit =0

3.4.3.2 Thermostat Mode (TM)

The thermostat mode bit can be configured to make the NST175 work in comparator mode (TM = 0) or interrupt mode (TM = 1). In *High and Low Limit Registers* section**,** there is more information of the comparator mode.

3.4.3.3 Polarity (POL)

The polarity bit allows the user to control the output polarity of the NST175 alert. When POL bit is 0, alert signal is active low, when POL bit is 1, alert signal is active high, while the state of alert is inverted. And the operation of ALERT pin in different modes is shown inFigure 3.8.

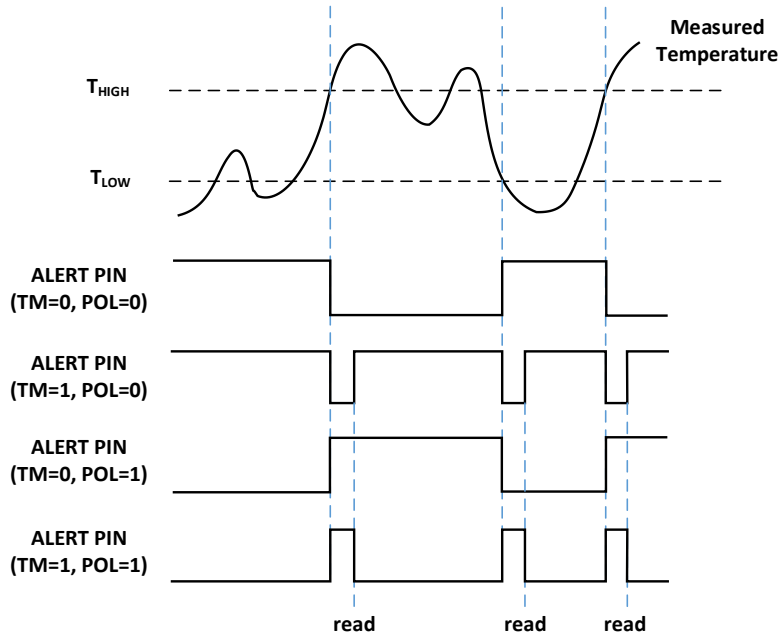


Figure 3.8. Output Transfer Function Diagrams

3.4.3.4 Fault Queue (F1/F0)

A fault condition is generated when the temperature measurement value exceeds the T_{HIGH} and T_{LOW} register values, and the number of fault conditions activated by the trigger alert can be programmed by the fault queue. False triggering of alerts due to temperature noise can be avoided by using a fault queue. Table 3.8 defines the number of measured faults that can be programmed to trigger a device alert condition. See the *High and Low Limit Registers* section for the format and byte order of the T_{HIGH} and T_{LOW} registers.

Table 3.8. Fault Settings of the NST175

F1	F0	CONSECUTIVE FAULTS
0	0	1 (Default)
0	1	2
1	0	4
1	1	6

3.4.3.5 Converter Resolution (R1/R0)

The conversion resolution bit controls the conversion resolution of the chip ADC, and the user can program it to get a higher resolution, Table 3.9 defines the resolution corresponding to R1/R0.

Table 3.9. Resolution of the NST175

R1	R0	Resolution	Conversion time（Typical）
0	0	9bit(0.5°C) (Default)	24ms

0	1	10bit(0.25°C)	24ms
1	0	11bit（0.125°C）	24ms
1	1	12bit（0.0625°C）	24ms

3.4.3.6 One-Shot (OS)

The NST175 supports a one-shot temperature measurement mode when continuous temperature monitoring is not required. When the NST175 is in shutdown mode, writing a 1 to the OS bit wakes up the device for a temperature conversion and returns the device to shutdown mode at the end of the conversion. During the temperature conversion, OS bit is 0, and at the end of the conversion, OS bit is 1.

In *One-Shot/Conversion Ready Mode (OS)* section**,** there is more information of the one-shot conversion mode.

3.4.3.7 High and Low Limit Registers

The temperature limit values in the T_{HIGH} and T_{LOW} registers have the same format as the temperature values in the temperature registers, and the result is used to compare with the limit to determine the status of the ALERT at the completion of each temperature conversion.

In comparator mode (TM=0), when the measured temperature data equals or exceeds the value of T_{HIGH} and the number of consecutive over-temperature data reaches the programmable queue setting (according to F1, F0), the alert pin is activated until the measured temperature falls below the value of T_{LOW} by the same number.

In interrupt mode (TM=1), when the measured temperature data equals or exceeds the value of T_{HIGH} and the number of consecutive over-temperature data reaches the programmable queue setting (according to F1, F0) the alert pin is activated until the master issues a read operation to any register or the device successfully responds to the SMBus alert address. The alert pin is also cleared when the device is set to SD mode. When the alert pin is cleared, it will be activated again only when the temperature falls below T_{LOW} until the master issues a read operation to any register or the device successfully responds to the SMBus alert address. the above cycle will be repeated after the alert pin is cleared. The alert's active state can also be cleared by general call reset. At the same time, this operation will reset the device registers to the power-up state and the device returns to comparator mode.

The operating modes of the devices are described in detail in Figure 3.8. Table 3.10, Table 3.11, Table 3.12, and Table 3.13 describes the data format of T_{HIGH} and T_{LOW}. The MSB is sent first, and the default values of T_{HIGH} and T_{LOW} after power-up are, both outputting MSB first and LSB second:

T_{HIGH} = 80 °C and T_{LOW} = 75 °C

The data format of T_{HIGH} and T_{LOW} registers is the same as that of the temperature register.

Table 3.10. Byte 1 of the TLOW Register (02H)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
Default	0	1	0	0	1	0	1	1

Table 3.11. Byte 2 of the TLOW Register (02H)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0

2	L3	L2	L1	L0	0	0	0	0
Default	0	0	0	0	0	0	0	0

Table 3.12. Byte 1 of the THIGH Register (03H)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
Default	0	1	0	1	0	0	0	0

Table 3.13. Byte 2 of the THIGH Register (03H)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0
Default	0	0	0	0	0	0	0	0

The T_{HIGH} and T_{LOW} register data format are the same as the temperature register. At any resolution, the T_{HIGH}, T_{LOW} register values are used to compare with the temperature test value to determine the function of the ALERT.

3.4.3.8 PRODID: Product ID Register (Read-Only) Pointer Address: 07h

Table 3.14. Product ID Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	P7	P6	P5	P4	P3	P2	P1	P0
Default	1	0	1	0	0	0	0	1

D4--D7 Product Identification Nibble. Always returns Ah to uniquely identify this part as the NST175.

D0--D3 Die Revision Nibble. Returns 1h to uniquely identify the revision level as one.

4.0 TYPICAL APPLICATION

4.1 Application information

The NST175 is compatible with both SMBus and I2C interfaces. the NST175 has 27 slave addresses, allowing up to 27 NST175 devices on one bus. the NST175 has an SMBus alarm function. No external components are required to operate the NST175 other than pull-up resistors on SCL, SDA and ALERT, although a bypass capacitor of 0.01μF is recommended. the sensing device for the NST175 device is the device itself. The thermal path is through the package leads as well as the plastic package. The low thermal resistance of the metal results in the leads providing the primary thermal path.

4.2 Typical application

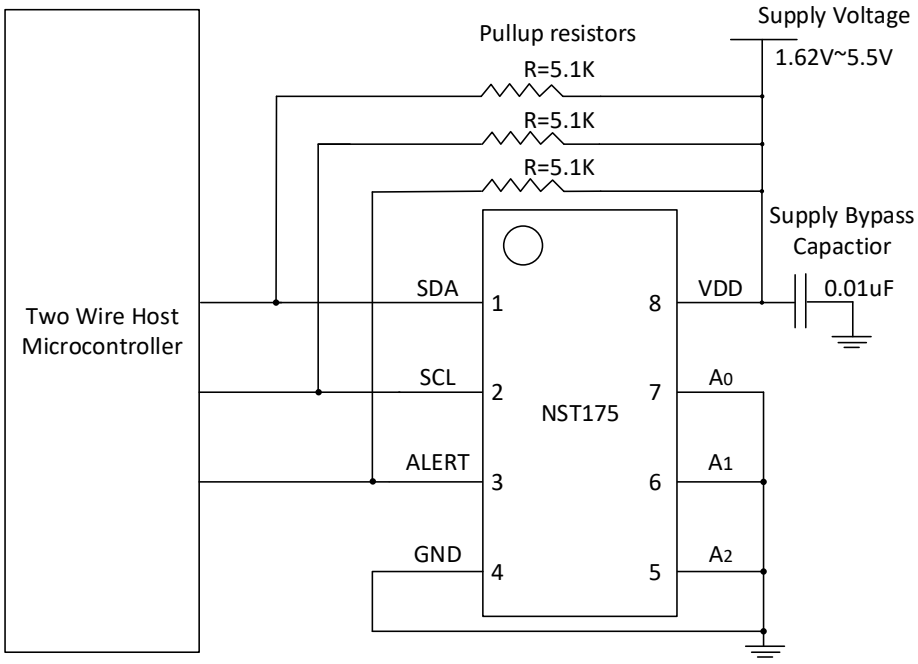
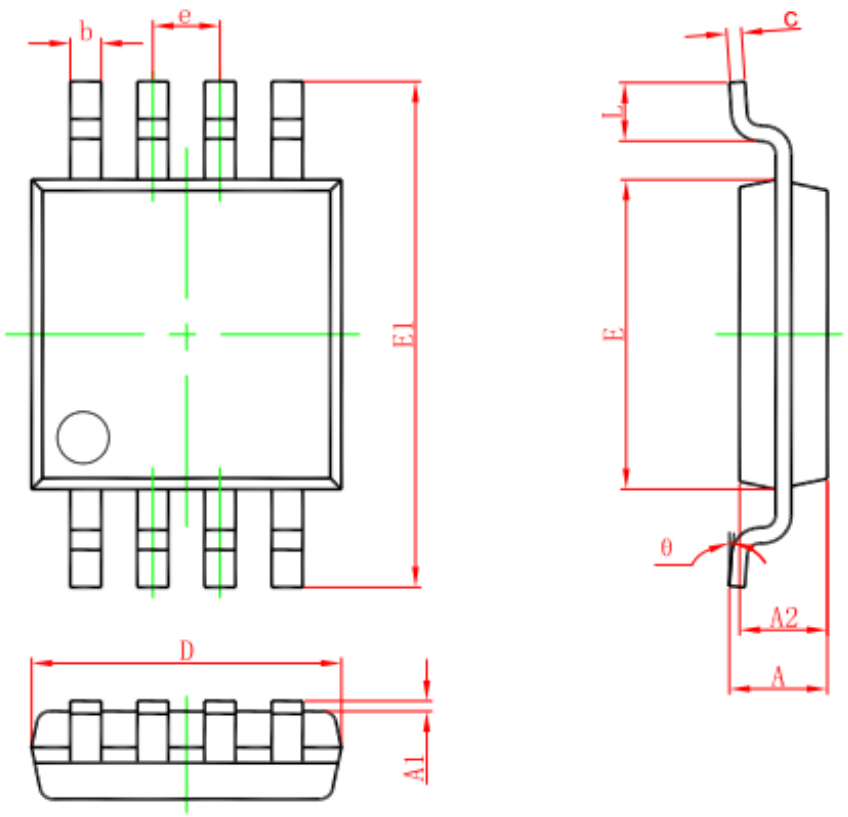


Figure 4.1. Typical Connections of the NST175

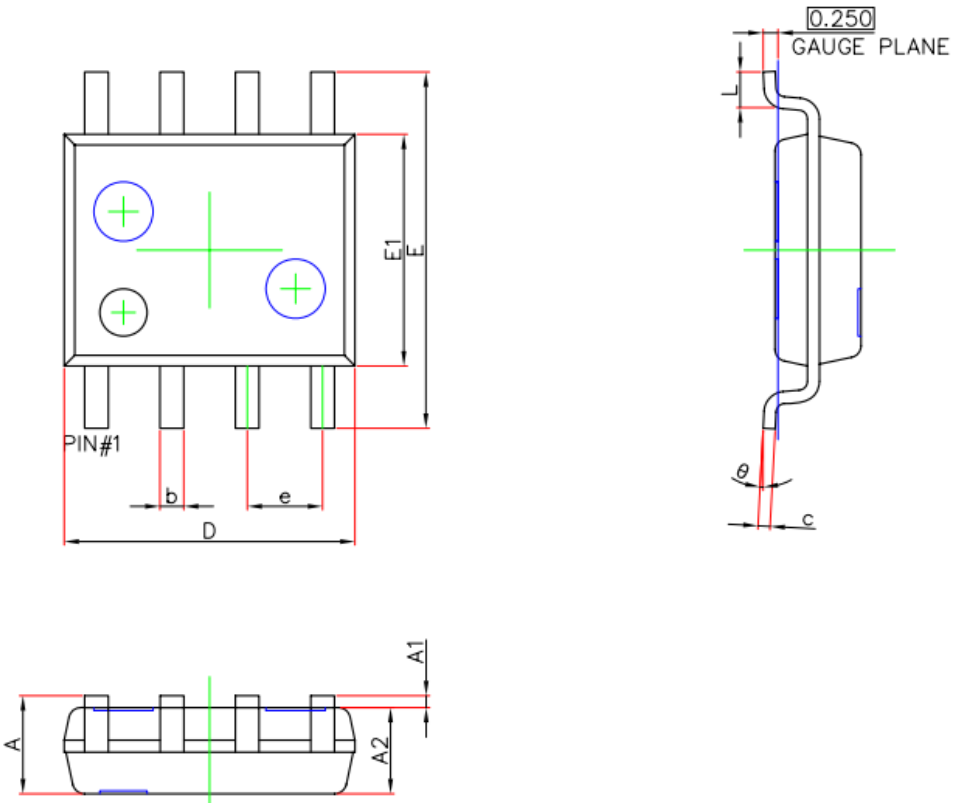
5.0 PACKAGE INFORMATION

5.1 MSOP (8) package



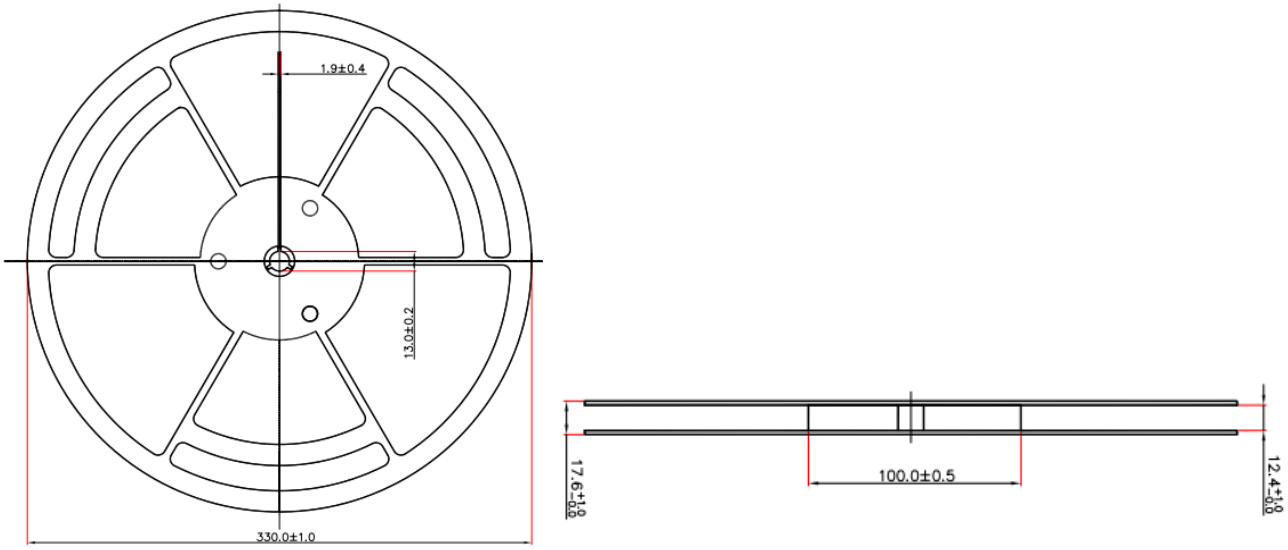
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

5.2 SOP (8) package

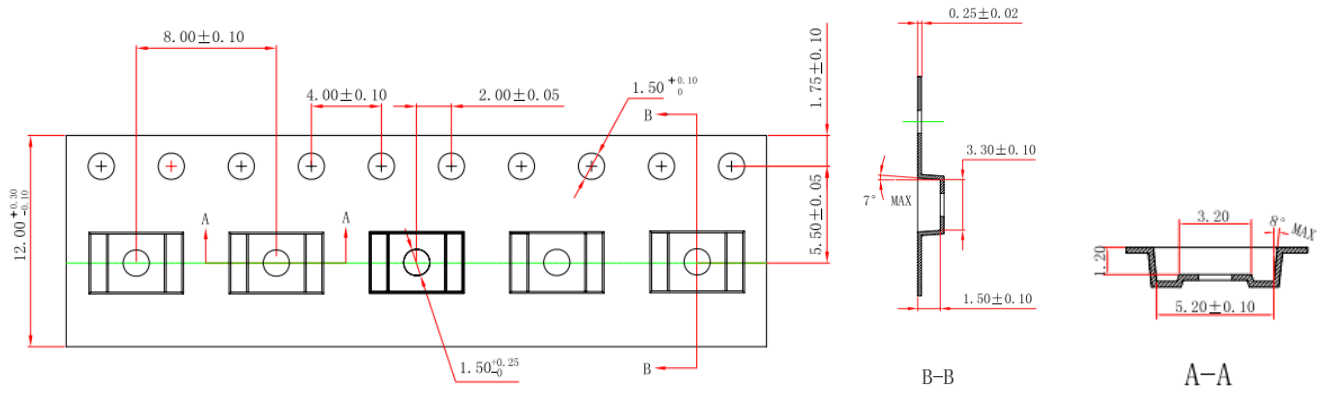


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

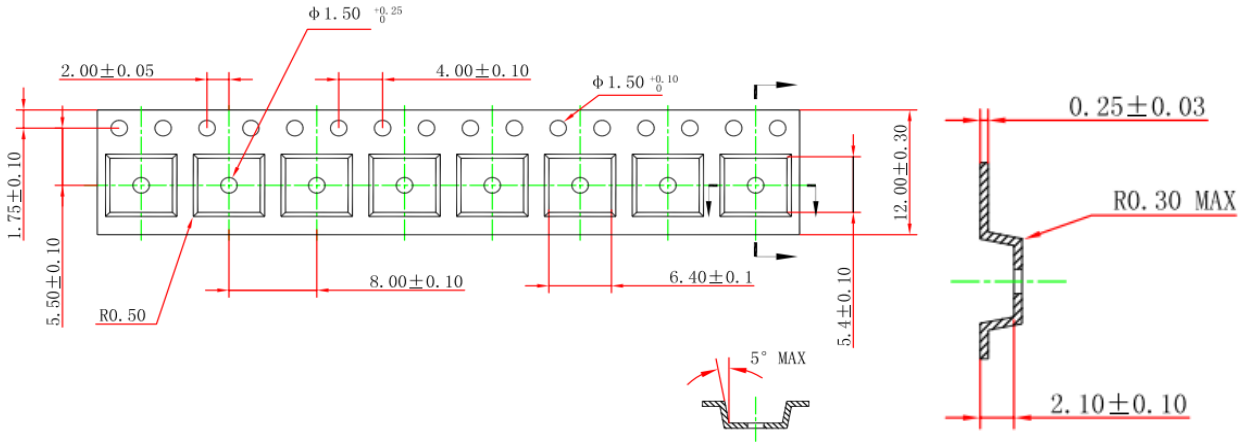
5.3 Tape and Reel Information



REEL Informatica (in mm)



MSOP8 TAPE Informatica (in mm)



SOP8 TAPE Informatica (in mm)

6.0 ORDER INFORMATION

Type	Unit	MSL	Marking	Description
NST175H-QMSR	4000ea/Reel	3	NST175	MSOP (8) package, Reel
NST175H-QSPR	4000ea/Reel	3	NST175	SOP (8) package, Reel
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures (Reflow profile: J-STD-020E).				

7.0 REVISION HISTORY

Revision	Description	Date
1.0	Initial Version	2019/4/20
1.1	MP Version	2019/9/12
1.2	Revise ordering infomation	2019/11/27
1.21	Revise ordering information	2020/2/12
1.3	Revise ordering information, tape and reel information	2021/2/1
1.31	Modify some descriptions	2021/7/28