NSiP1042

Signal Isolated CAN Transceiver With Integrated DC to DC Converter

Datasheet (EN) 1.0

Product Overview

NSiP1042 is a high reliability isolated controller area network(CAN) physical layer transceiver with integrated DC to DC converter. The isolated DC-DC converter provides output power using on-chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacitive isolation technology. Both devices are safety certified by UL1577, supporting 5kVrms insulation withstand voltage, while the high integrated solution can help to simplify system design and improve reliability.

The Bus pins of NSiP1042 are protected from ±5kV system level ESD to GND_2 on Bus side. The data rate of the NSiP1042 is up to 5Mbps. The NSiP1042 provides thermal protection and transmit data dominant time out function.

Key Features

- Up to 5000Vrms Insulation voltage
- Isopower integrated isolated DC-DC converter
- Power supply voltage:

  VDD_1:4.5V to 5.5V

  VDDL:1.8V to 5.5V
- Over current and over temperature protection
- High CMTI: ±150kV/us
- Data rate: 5Mbps
- Operation temperature: -40℃~105℃
- RoHS-compliant packages: SOW20

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	*Package*	*Body Size*
NSiP1042-DSWTR	SOW20	12.80mm × 7.50mm

Functional Block Diagrams

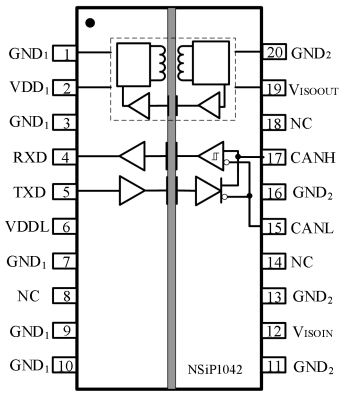

Figure 1. NSiP1042 Block Diagrams

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1. Pin Configuration and Functions

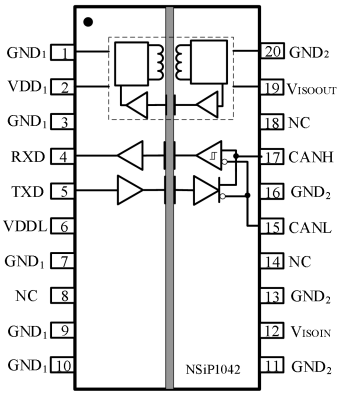


Figure 1.1 NSiP1042 Package

Table1.1 NSiP1042 Pin Configuration and Description

NSiP1042 PIN NO.	*SYMBOL*	*FUNCTION*
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	VDD_1	Power Supply for Isolator Side 1
3	GND_1	Ground 1, the ground reference for Isolator Side 1
4	RXD	Receiver output
5	TXD	Driver transmit data input
6	VDDL	I/O Power Supply input. Side1 I/O logic level.
7	GND_1	Ground 1, the ground reference for Isolator Side 1
8	NC	Not connected
9	GND_1	Ground 1, the ground reference for Isolator Side 1
10	GND_1	Ground 1, the ground reference for Isolator Side 1
11	GND_2	Ground 2, the ground reference for Isolator Side 2
12	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1 μ F capacitor to GND_2 (Pin11). Connect this pin through a ferrite bead and short trace length to V_{ISOOUT} for operation.
13	GND_2	Ground 2, the ground reference for Isolator Side 2
14	NC	Not connected
15	CANL	Low-level CAN bus line, when VDD is powered down, Pin CANL is put into a high impedance state to avoid overloading the bus
16	GND_2	Ground 2, the ground reference for Isolator Side 2
17	CANH	High-level CAN bus line, when VDD is powered down, Pin CANH is put into a high impedance

		state to avoid overloading the bus
18	NC	Not connected
19	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1 μF and 10uF capacitor to GND_2 (Pin20). Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.
20	GND_2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD_1	-0.5		6	V	
Maximum Input Voltage	TXD	-0.4		VDDL+0.4	V	
Driver Output/Receiver Input Voltage	CANH, CANL	-70		70	V	
RXD Output current	I_O	-15		15	mA	
Ambient Temperature	T_a	-40		105	℃	
Storage Temperature	T_{stg}	-40		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Power Supply Voltage	VDD	4.5		5.5	V
	VDDL	1.8		5.5	V
Operating Temperature	T_{opr}	-40		105	℃
High Level Input Voltage	V_{IH}	0.7*VDDL			V
Low Level Input Voltage	V_{IL}			0.3*VDDL	V
Data rate	DR			5	Mbps

4. Thermal Information

Parameters	Symbol	Value	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	68.5	°C/W
Junction-to-top characterization parameter	ψ_{JT}	17.1	°C/W
Junction-to-board characterization parameter	ψ_{JB}	50.9	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V,Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VDD	4.5		5.5	V	
	VDDL	1.8		5.5	V	
Supply current	IDD		100	180	mA	VDD=5V, TXD=0,R_{load}=60 Ω
			12.9	25	mA	VDD=5V, TXD=VDD
	IDDL		153	1000	uA	VDD=VDDL=5V, RL=60Ω TXD=0
	IDDL		57	500	uA	VDD=VDDL=5V, RL=60Ω TXD=VDD
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Isolated supply voltage	V_{ISOOUT}		5		V	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	See Fig 5.3.10
Logic Side						
High level input voltage	V_{IH}	0.7*VDDL			V	TXD pin
Low level input voltage	V_{IL}			0.3*VDDL	V	TXD pin
High level input current	I_{IH}	-1		1	uA	TXD pin
Low level input current	I_{IL}	-15			uA	TXD pin
Output Voltage High	V_{OH}	VDDL-0.4			V	I_{OH} = -4mA, RXD pin
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA, RXD pin
Input Capacitance	C_{IN}		2		pF	TXD pin
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4	V	V_I=0V, R_{Load} =60 Ω ,see Figure 5.3.1 and Figure 5.3.2
CANL output voltage	$V_{OL(D)}$	0.8	1.33	2	V	V_I=0V, R_{Load} =60 Ω ,see Figure

(Dominant)						5.3.1 and Figure 5.3.2
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	TXD=VDD_1, R_{Load} =60 Ω ,see Figure 5.3.1 and Figure 5.3.2
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	TXD=0, RLoad =60 Ω , see Figure 5.3.1 and Figure 5.3.2
		1		3	V	TXD=0, R_{Load} =45 Ω ,
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.12		0.12	V	TXD=VDD_1, R_{Load} =60 Ω
		-0.5		0.5	V	TXD=VDD_1, NO Load
Common-mode output voltage	V_{OC}	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	See Fig 5.3.6
Short- circuit output current	I_{OS}	-105	-44.1		mA	CANH=-30V, CANL open, see Figure 5.3.9
		0		10	mA	CANH=30V, CANL open, see Figure 5.3.9
		-5		0	mA	CANL=-30V, CANH open, see Figure 5.3.9
			42.5	105	mA	CANL=30V, CANH open, see Figure 5.3.9
Receiver						
Positive-going differential bus input threshold voltage	V_{TH+}		750	900	mV	V_{IC}=0 see Figure 5.3.4
Negative-going differential bus input threshold voltage	V_{TH-}	500	650		mV	V_{IC}=0 see Figure 5.3.4
Bus Differential input threshold Hysteresis	V_{HYS}		100		mV	
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input capacitance	C_{ID}		6.5		pF	
Differential input resistance	R_{ID}	30		80	kΩ	
Input resistance	R_{IN}	15	30	40	kΩ	
Input resistance matching	R_{Imatch}	-3		+3	%	CANH=CANL
Common-mode voltage range	V_{IC}	-30		+30	V	

5.2. Switching Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V,Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Loop delay1	T_{Loop1}		104	180	ns	Driver input to receiver output, Recessive to Dominant， see Figure 5.3.7
Loop delay2	T_{Loop2}		122	210	ns	Driver input to receiver output, Dominant to Recessive， see Figure 5.3.7
Driver						
Propagation delay time, recessive -to- dominant output	t_{PLHD}		77		ns	Figure 5.3.3
Propagation delay time, dominant -to- recessive output	t_{PHLD}		72		ns	Figure 5.3.3
Differential output signal rise time	t_{rD}		26		ns	Figure 5.3.3
Differential output signal fall time	t_{fD}		40		ns	Figure 5.3.3
Bus dominant time-out time	t_{TXD_DTO}	600	2000	4000	us	See Figure 5.3.8
Receiver						
Propagation delay time, low-to-high-level output	t_{PLHR}		50		ns	Figure 5.3.5
Propagation delay time, high-to-low-level output	t_{PHLR}		27		ns	Figure 5.3.5
RXD signal rise time	t_{rR}		3		ns	Figure 5.3.5
RXD signal fall time	t_{rF}		3		ns	Figure 5.3.5

5.3. Parameter Measurement Information

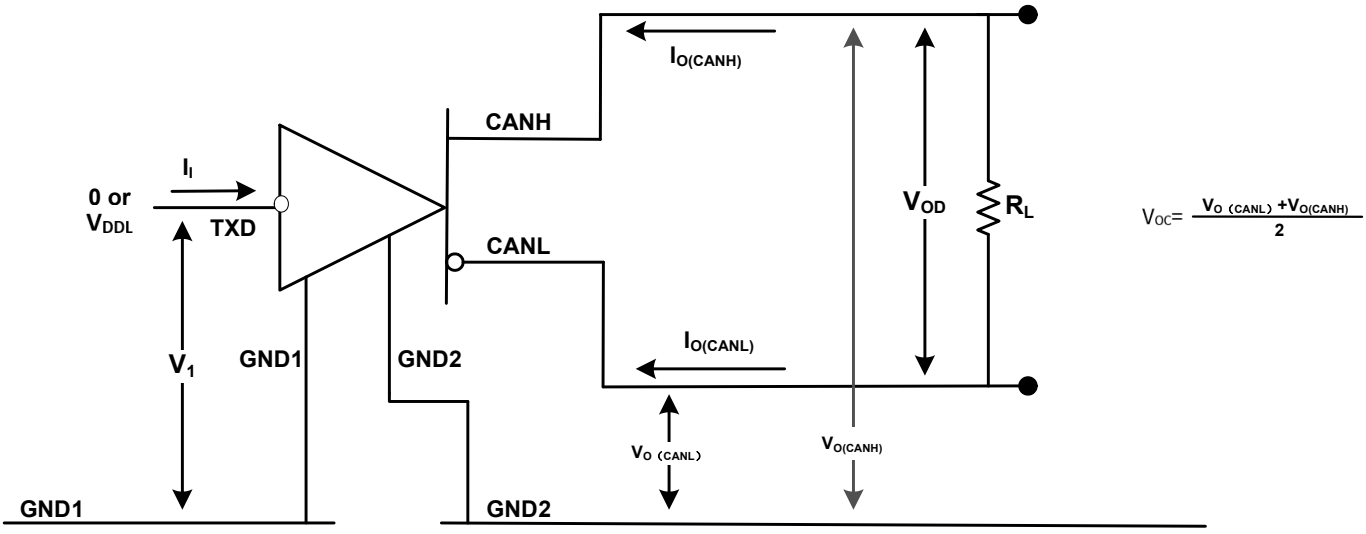


Figure 5.3.1. Driver Voltage, Current and Test Definitions

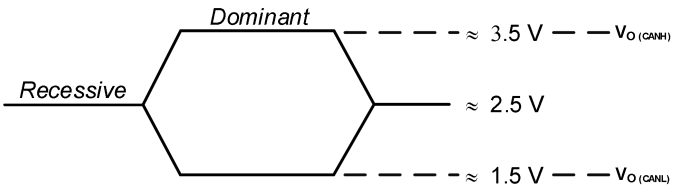
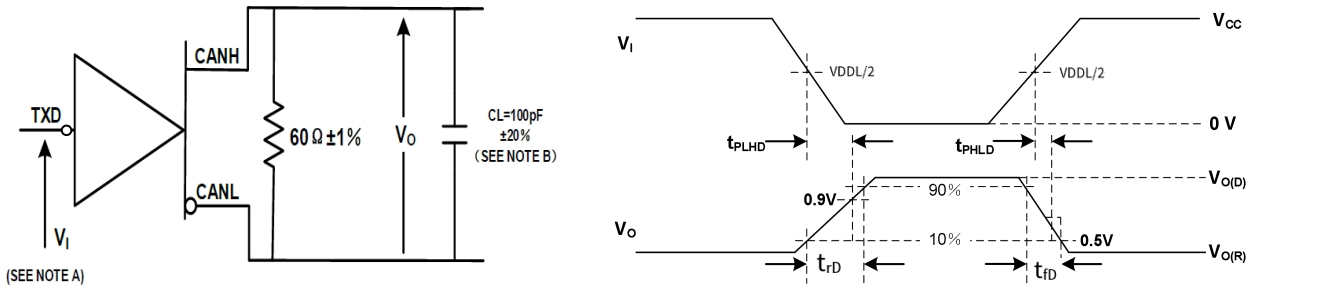


Figure 5.3.2. Bus Logic State Voltage Definitions



Note： A. The input pulse is supplied by a generator having the following characteristics: Pulse Repeat Rate ⩽ 125 kHz, 50% duty cycle t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 5.3.3. Driver Test Circuit and Voltage Waveform

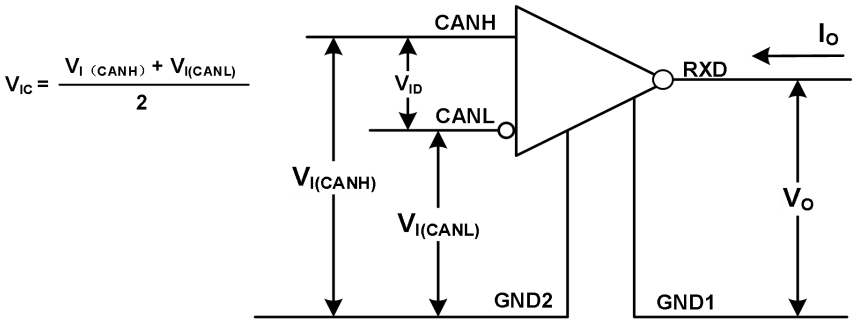
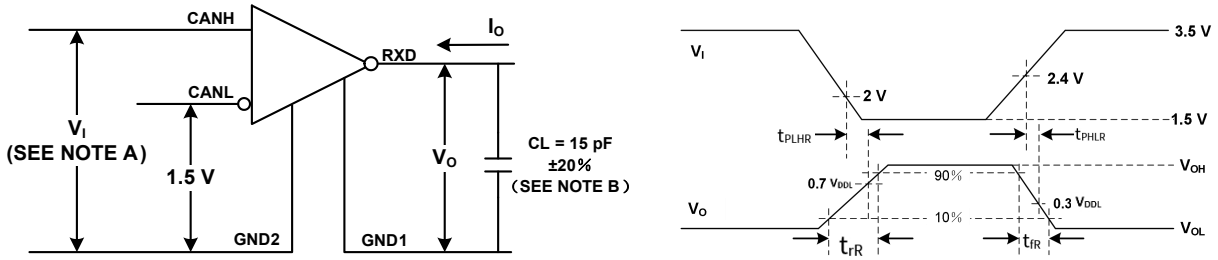


Figure 5.3.4. Receiver Voltage and Current Definitions



Note: A. The input pulse is supplied by a generator having the following characteristics: Pulse Repeat Rate ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.3.5. Receiver Test Circuit and Voltage Waveform

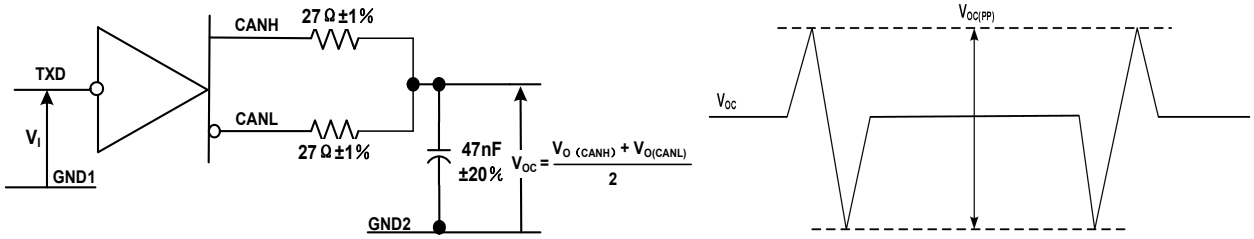


Figure 5.3.6. Peak-to-Peak Output Voltage Test Circuit and Waveform

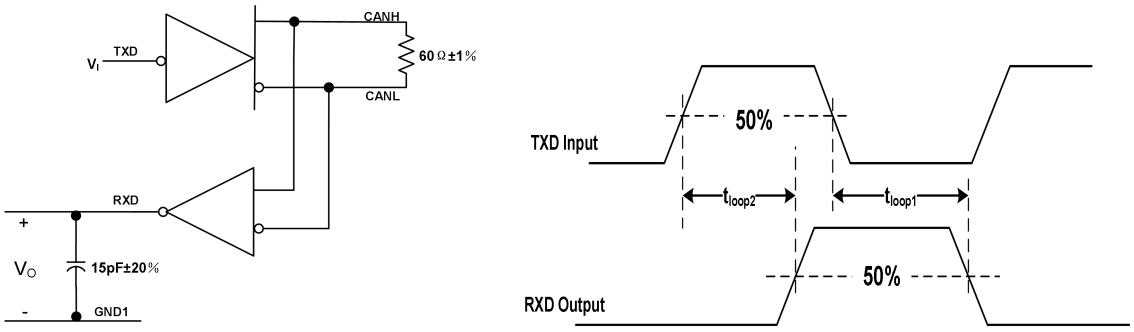
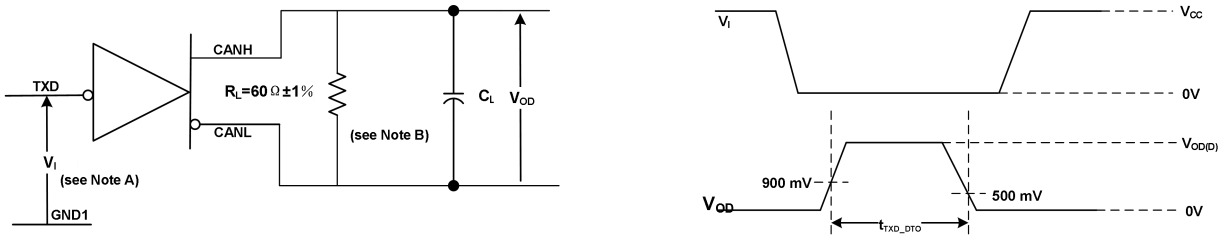


Figure 5.3.7. t_{LOOP} Test Circuit and Voltage Waveform



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 125 kHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5.3.8. Dominant Time-out Test Circuit and Voltage Waveform

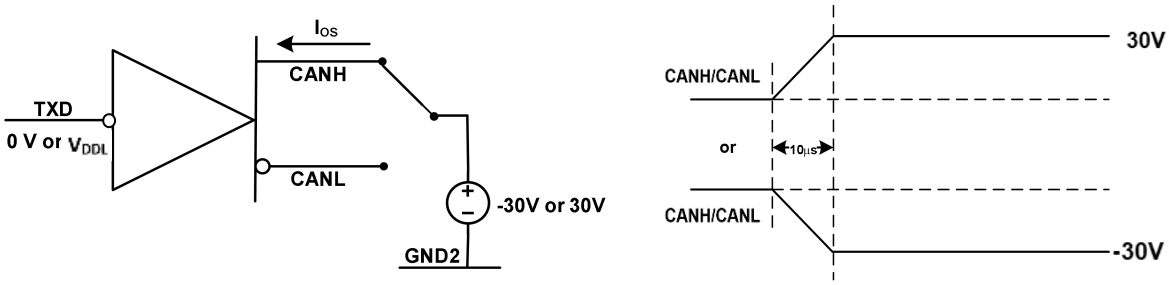


Figure 5.3.9. Driver Short-Circuit Current Test Circuit and Waveform

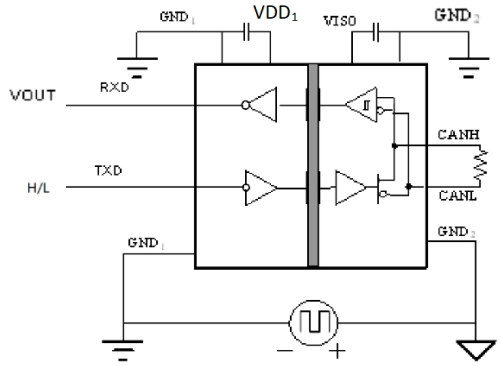


Figure5.3.10 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation And Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	16	um	Minimum internal gap (internal clearance – capacitive signal isolation)
		100	um	Minimum internal gap (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 600Vrms			Ⅰ to Ⅲ	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage	AC voltage(bipolar)	V_{IORM}	1166	V_{peak}
Maximum working isolation voltage	AC Voltage (TDDB) test	V_{IOWM}	824	V_{rms}
	DC Voltage	V_{IOWM}	1166	V_{DC}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t m = 10 sec, partial	$V_{pd(m)}$	1399	Vpeak

	discharge < 5 pC			
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production)	V_{IOTM}	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.3\times V_{IOSM}$	V_{IOSM}	5384	Vpeak
Isolation resistance	V_{IO} =500V	R_{IO}	>10^9	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	pF
Total Power Dissipation at 25℃		Ps	1459	mW
Safety input, output, or supply current	θ_{JA} = 68.5°C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C	Is	265	mA
Maximum safety temperature		Ts	125	℃

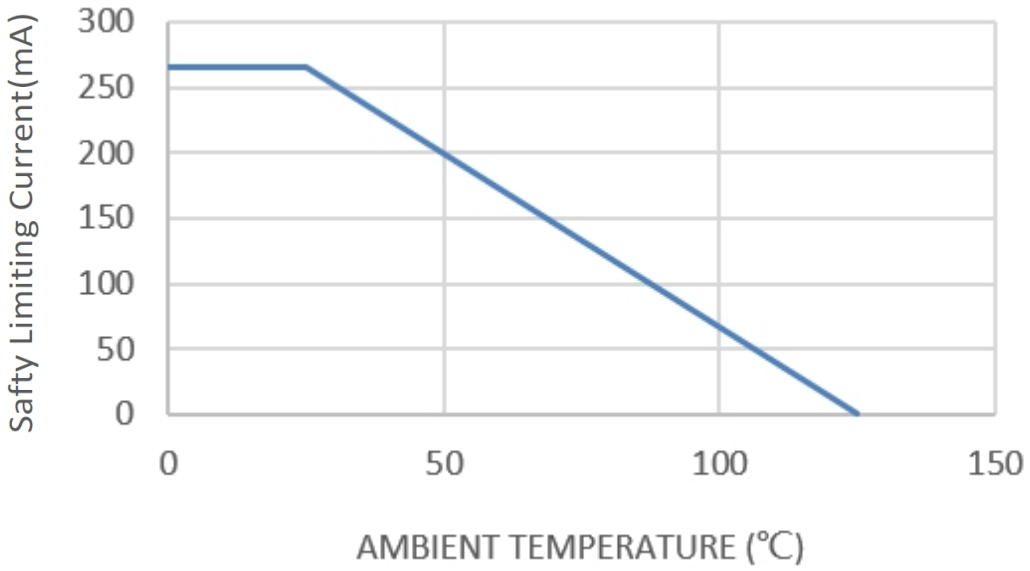


Figure 6.1 NSiP1042 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSiP1042 are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2022 GB4943.1-2022
Single Protection, 5000V_{RMS} Isolation voltage	Single Protection, 5000V_{RMS} Isolation voltage	Basic Insulation 1166V_{PEAK}, V_{IOSM}=5384V_{PEAK}	Basic insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

The NSiP1042 is an isolated CAN transceiver which is fully compatible with the ISO11898-2 standard. The NSiP1042 is a high reliability isolated controller area network(CAN) physical layer transceiver with integrated DC to DC converter. The digital isolator is SiO_2 isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSiP1042 device is safety certified by UL1577, supporting 5kVrms insulation withstand voltages. The NSiP1042 provides high electromagnetic immunity and low emission. The data rate of the NSiP1042 is up to 5Mbps. The NSiP1042 provides thermal protection and transmit data dominant time out function.

7.1. Device Functional Modes

TXD	*CANH*	*CANL*	*BUS STATE*
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

[1] H= high level; L=low level; Z= common mode(recessive) bias to V_{ISOIN}/2

Table 7.1. Driver Function Table

V_{ID}=CANH-CANL	*RXD*	*BUS STATE*
V_{ID} ⩾0.9V	L	Dominant
0.5< V_{ID} <0.9V	X	Uncertain
V_{ID} ⩽0.5V	H	Recessive
Open	H	Recessive

[1] H= high level; L=low level; X= uncertain

Table 7.2. Receiver Function Table

7.2. TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

7.3. Current Protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.4. Over Temperature Protection

The NSiP1042 is protected against over-temperature conditions. When the chip is over 165℃, it will be shut down until the temperature of below 145℃.

8. Application Note

8.1. Layout Considerations

The NSiP1042 require a 10 µF + 0.1 µF bypass capacitor between VDD_1 and GND_1, 10uF + 0.1 µF bypass capacitor between V_{ISOOUT} and GND_2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to place the bus connectors and termination resistor as close as possible to the CANH and CANL pins.

8.2. Typical Application

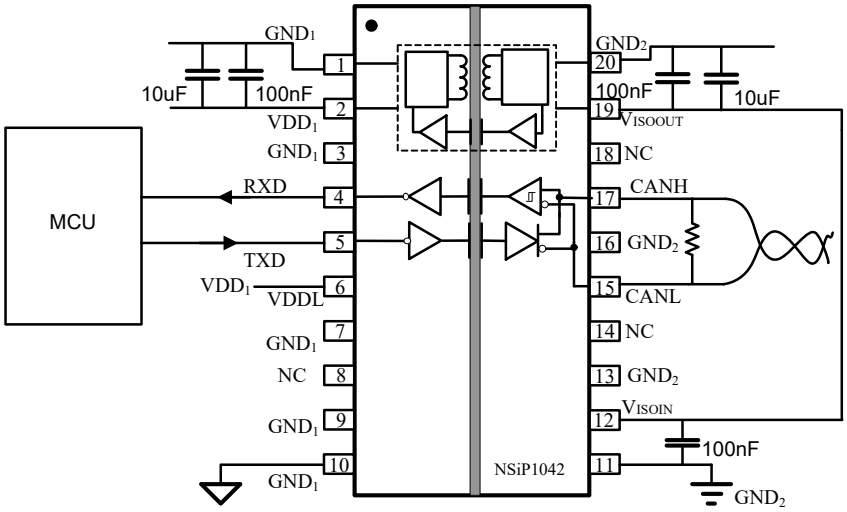
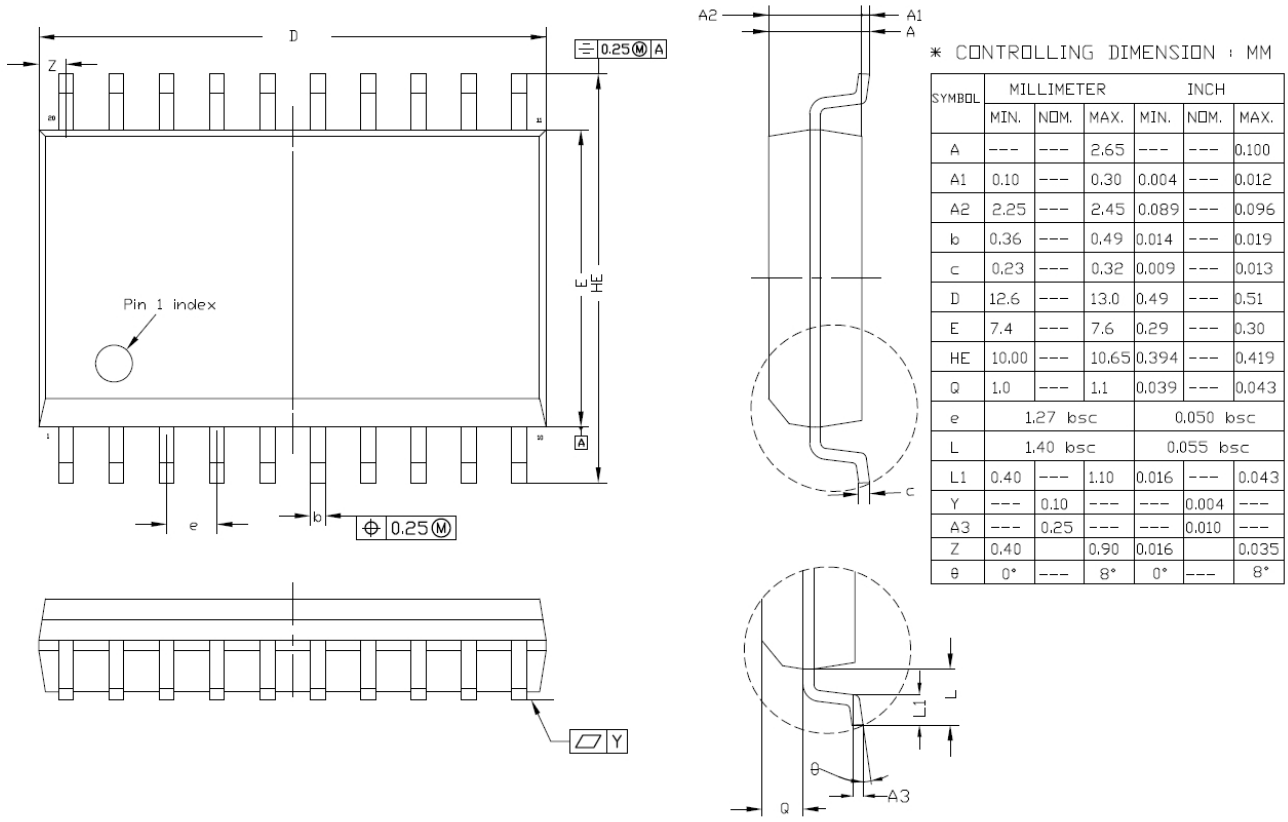


Figure 8.1 NSiP1042 typical application circuit

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	2.65	---	---	0.100
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.45	0.089	---	0.096
b	0.36	---	0.49	0.014	---	0.019
c	0.23	---	0.32	0.009	---	0.013
D	12.6	---	13.0	0.49	---	0.51
E	7.4	---	7.6	0.29	---	0.30
HE	10.00	---	10.65	0.394	---	0.419
Q	1.0	---	1.1	0.039	---	0.043
e	1.27 bsc			0.050 bsc		
L	1.40 bsc			0.055 bsc		
L1	0.40	---	1.10	0.016	---	0.043
Y	---	0.10	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
Z	0.40		0.90	0.016		0.035
θ	0°	---	8°	0°	---	8°

Figure 9.1 SOW20 Package Shape and Dimension in millimeters

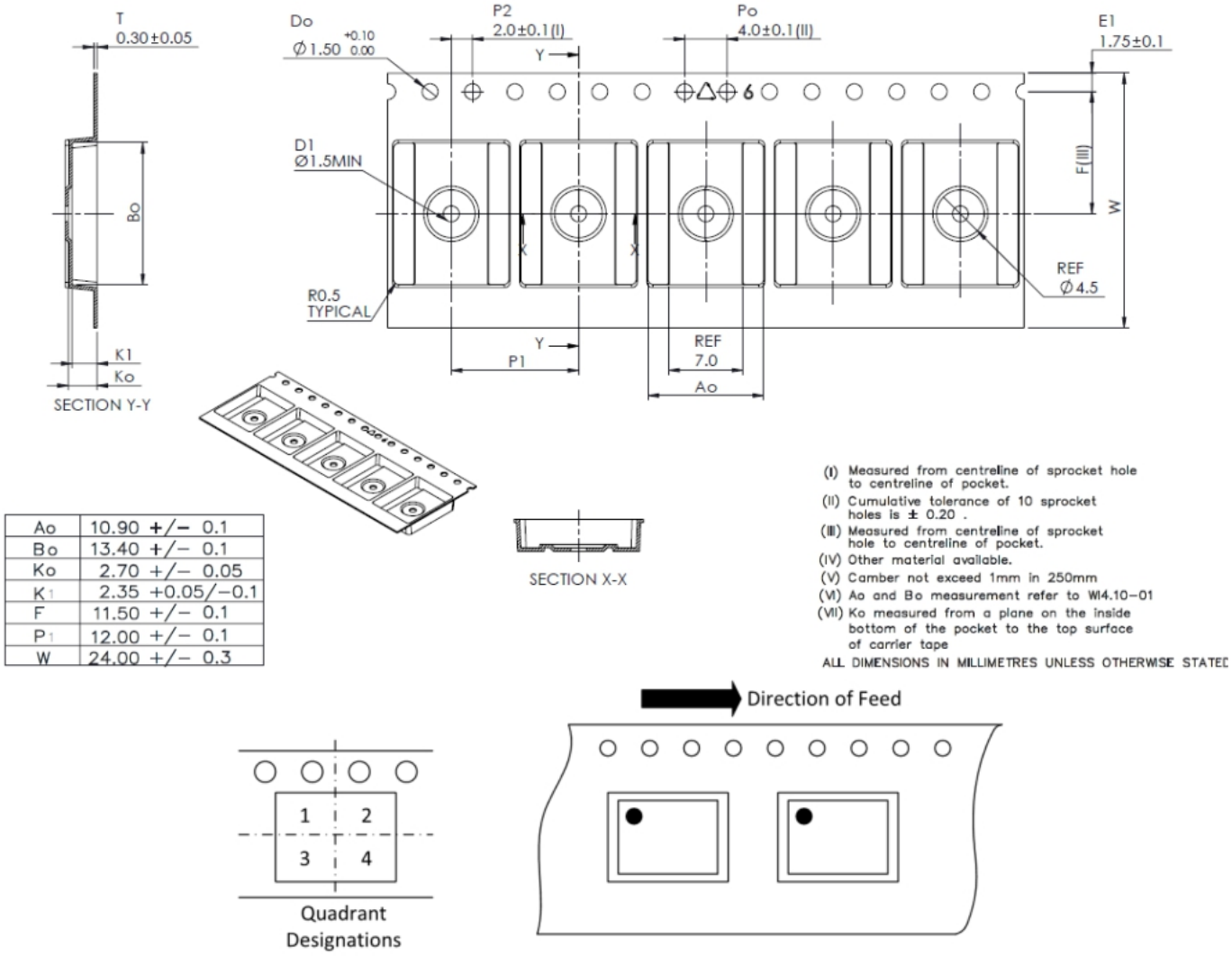
10. Order Information

Part Number	*Isolation Rating (kVrms)*	*Max Data Rate (Mbps)*	*MSL*	*Temperature*	*Package Type*	*Package Drawing*	*SPQ*
NSiP1042-DSWTR	5	5	3	-40 to 105°C	SOP20(300mil)	SOW20	1000

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Application Note*
NSiP1042	Tbd	Tbd	Tbd

12. Tape And Reel Information



Ao	10.90 +/− 0.1
Bo	13.40 +/− 0.1
Ko	2.70 +/− 0.05
K1	2.35 +0.05/−0.1
F	11.50 +/− 0.1
P1	12.00 +/− 0.1
W	24.00 +/− 0.3

Figure 12.1 Tape and Reel Information of SOW20

13. Revision History

Revision	Description	Date
1.0	Initial version	2022/12/28

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