Integrated GaN PFC Converter IC

■ GENERAL DESCRIPTION

The DK83XX is a power factor correction chip that operates in critical conduction mode and discontinuous conduction mode. It works in critical conduction mode under heavy loads and seamlessly switches to discontinuous conduction mode when the load decreases. The chip integrates a 700V gallium nitride power transistor, along with built-in functions such as soft start, input undervoltage protection, input power compensation, overtemperature protection, output undervoltage and overvoltage protection, and overcurrent protection. The DK83XX, when used in conjunction with downstream chips such as FLYBACK, AHB, and LLC, enables highly efficient and reliable power solutions.

■ FEATURES

- Ultra-low standby power consumption (25mW @115Vac, 39mW @230Vac): Meets CoC V5 Tier 2 and DoE VI requirements without disabling PFC
- Wide bus voltage input (85–265 Vac)
- CRM and DCM operation modes
- Valley switching
- Segmented output voltage function: (400Vdc @ AC > 170V, 264Vdc @ AC < 146V)
- Demagnetization detection without auxiliary winding
- Input power compensation
- Built-in 700V GaN power transistor
- Integrated comprehensive protection functions:
  VCC under-voltage protection, output over-current protection, output under-voltage/over-voltage protection, over-temperature protection, bypass diode short-circuit protection, and RCS resistor open-circuit protection

■ APPLICATIONS

- Power Adapters
- Computer power supplies
- Printer power supplies
- LED drivers

■ *MARKING DIAGRAMS*

Marking	Note
DK	DK Semiconductor
B	Production test code includes space, "A~Z, *#Δ"
2501	1st batch of 2025
8318	Product No.
SATH0	Ordering code
T01	IC code and small batch number,usually from 01 to 25

■ *Ordering code Definition*

1st digit: Package	2nd digit: Controller Version	3rd digit: Integrated GaN Specs	4th digit: Function	5th digit: Reserved
S:ESOP16L	A:controller version is A	V: 700V/196mΩ	H:Non-segmented Output	0：reserved
		O: 700V/160mΩ	L:Segmented Output	
		T: 700V/101mΩ		
		E: 700V/75mΩ		

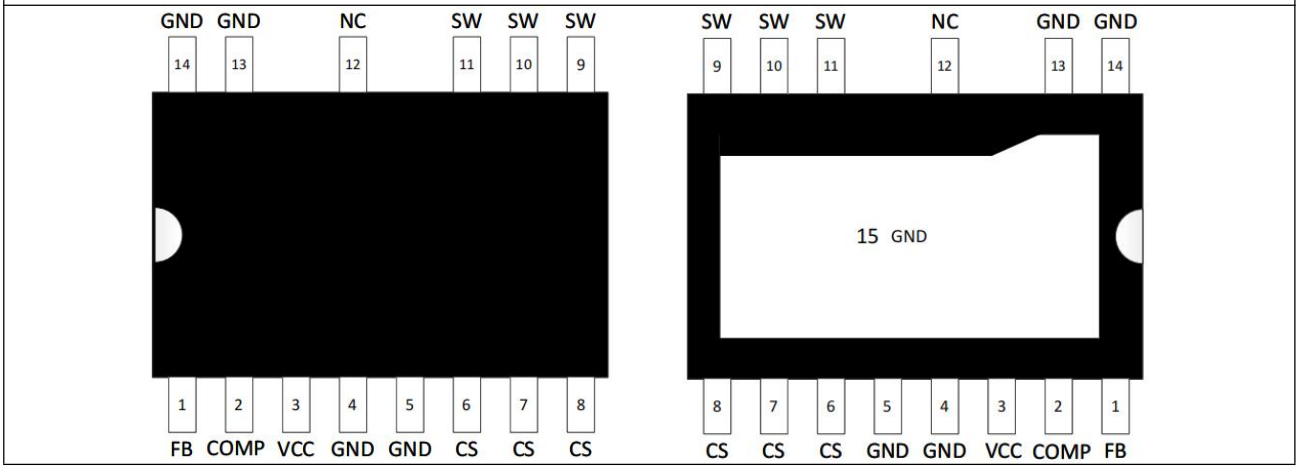
■ *Ordering Information*

Product No.	Ordering Code	Package	Integrated GaN Specs	Packaging form	Recommended power ($90\text{-}264V_{AC}$)
DK8310	SAVH0	ESOP16L	700V/196mΩ	2000pcs/Tray	100W
DK8310	SAVL0	ESOP16L	700V/196mΩ	2000pcs/Tray	
DK8312	SAOH0	ESOP16L	700V/160mΩ	2000pcs/Tray	120W
DK8312	SAOL0	ESOP16L	700V/160mΩ	2000pcs/Tray	
DK8318	SATH0	ESOP16L	700V/101mΩ	2000pcs/Tray	180W
DK8318	SATL0	ESOP16L	700V/101mΩ	2000pcs/Tray	
DK8320	SAEH0	ESOP16L	700V/75mΩ	2000pcs/Tray	200W
DK8320	SAEL0	ESOP16L	700V/75mΩ	2000pcs/Tray	

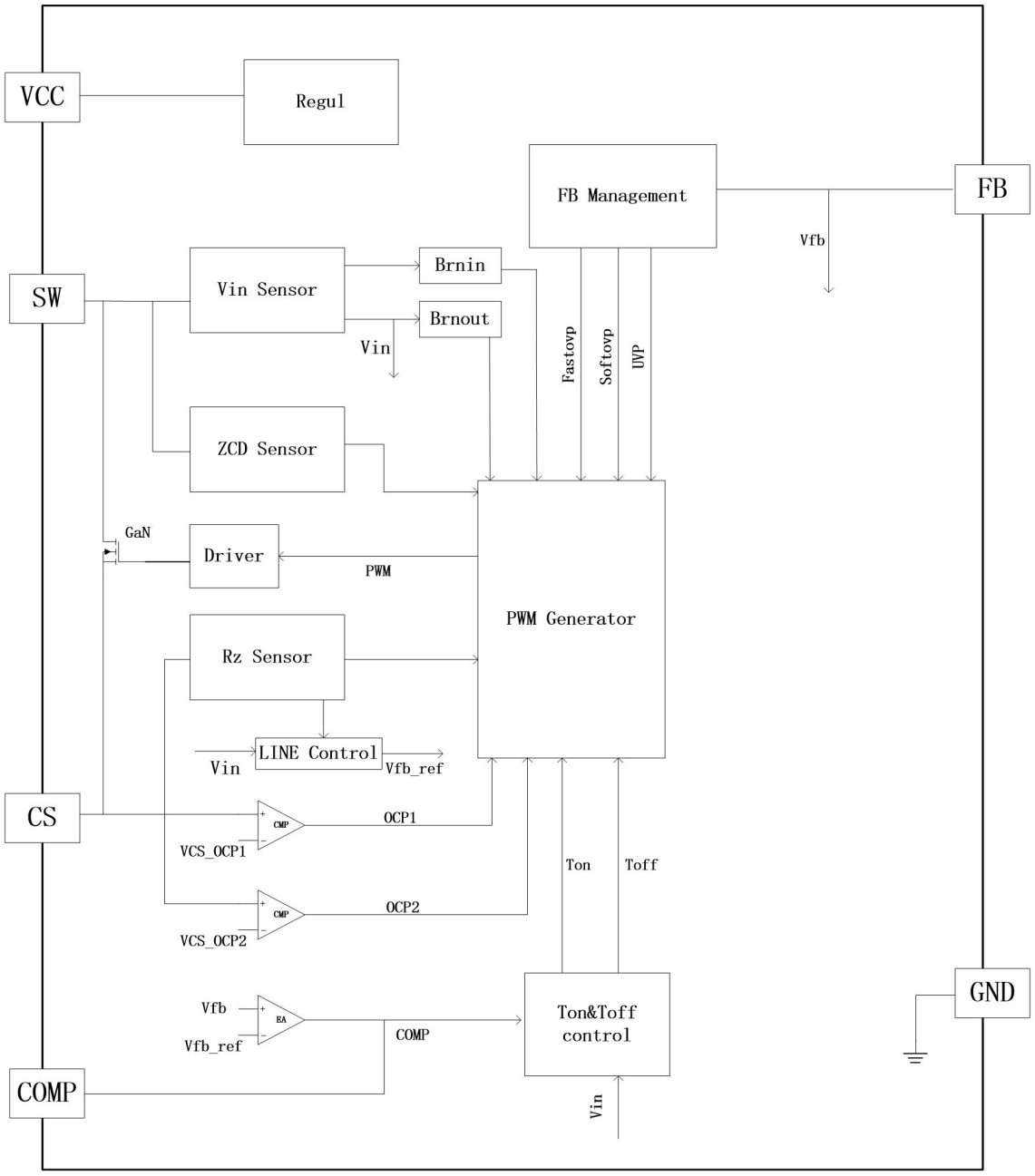
■ *PINS CONFIGURATION*

PINS No	PINS	Description
1	FB	Output Voltage Feedback Pin
2	COMP	EA External Compensation Pin
3	VCC	Chip Power Supply Pin
4,5,13,14,15	GND	Chip ground
6,7,8	CS	Inductor Current Sense Input Pin
9,10,11	SW	Power Transistor Drain
12	NC	Internally No Connect

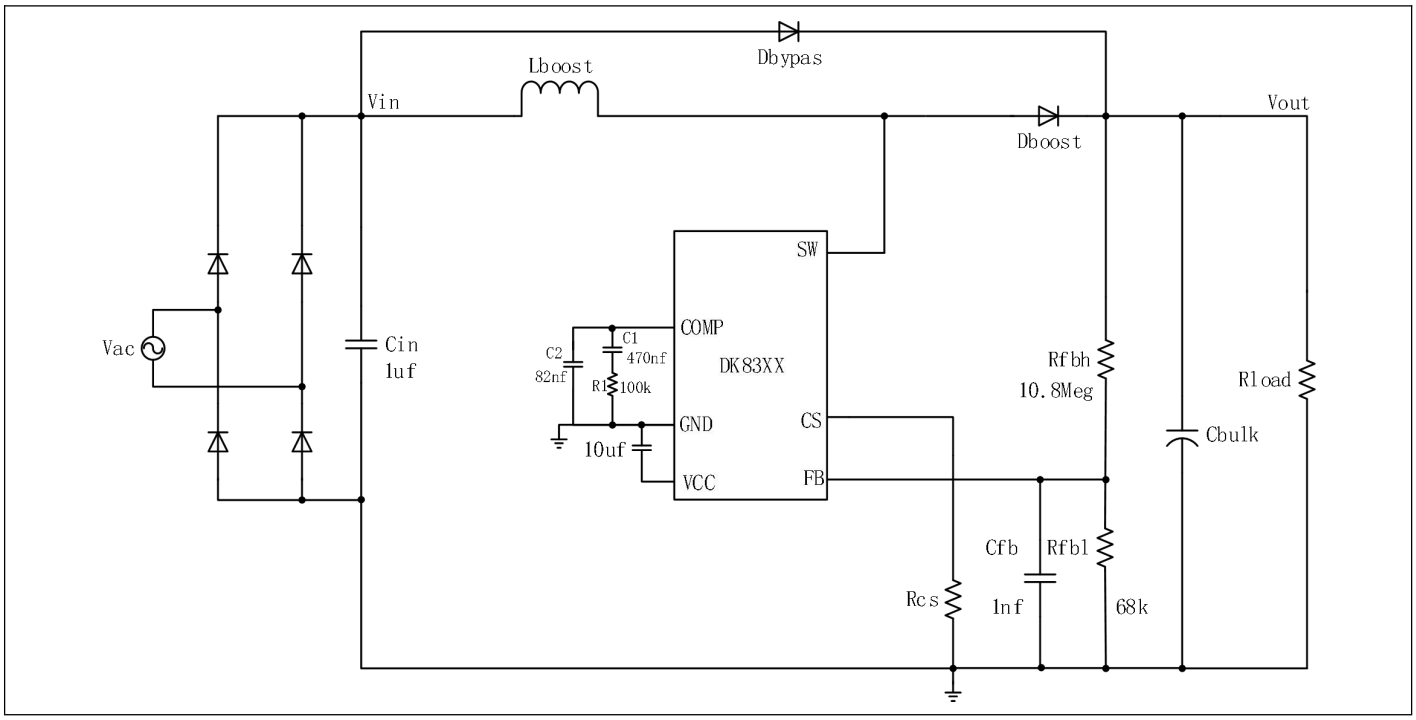
ESOP16L



■ *BLOCK DIAGRAM*



■ *TYPICAL APPLICATION CIRCUIT*



■ *ABSOLUTE MAXIMUM RATINGS (T_A=25℃ Unless otherwise noted)*

Rating	Symbol	Min	Max	Unit
GaN HEMT VD voltage	SW	-2	700	V
Saturation current①（Tc=125℃）	I_{SAT}	5.1(DK8310) 6.8(DK8312) 10.5(DK8318) 13.7(DK8320)		A
Drain-source continuous current	I_D		8(DK8310) 11(DK8312) 16(DK8318) 21(DK8320)	A
Drain-source pulse current（Tc = 25 °C,t_{PULSE}=10μs）	$I_{D,pulse}$		15.5(DK8310) 20(DK8312) 32(DK8318) 41(DK8320)	A
Drain-source pulse current（Tc = 125 °C,t_{PULSE}=10μs）	$I_{D,pulse}$		8(DK8310) 11(DK8312) 18(DK8318) 23(DK8320)	A
VCC Pin withstand voltage	VCC	-0.5	36	V
Current Sense Pin withstand Voltage	CS	-0.5	8.5	V
Output Voltage Feedback Pin withstand Voltage	FB	-0.5	8.5	V
Compensation Pin withstand Voltage	COMP	-0.5	8.5	V
Storage temperature range	TSTG	-55	-155	℃

Junction temperature	TJ	-40	150	℃
Soldering temperature	TW		260/5S	℃
ESD	HBM（Excluding SW pin）	±2000		V
	HBM（SW Pin）	±1000		V
	CDM	±500		V

Note: Absolute Maximum Ratings refer to limits beyond which damage to the chip may occur. The Recommended Operating Conditions specify the range within which the device functions normally, but does not fully guarantee all performance specifications. The Electrical Characteristics define the DC and AC parameter specifications under specific test conditions that ensure performance within the operating range. For parameters without specified min/max limits, the accuracy is not guaranteed by this specification, but the typical value reasonably reflects the device performance.

①: ISAT is the maximum saturation current of the GaN device at 125°C. The device's saturation current is inversely proportional to its temperature, so device temperature must be considered during use. Refer to the normalized current capability curve of the GaN device in the OPERATION DESCRIPTION section below for saturation current data conversion. The actual system current setting should be determined based on the chip's temperature.

■ *ELECTRIC CHARACTERISTICS* (V_{CC}=18V,T_A=25℃ *Unless otherwise noted)*

Symbol	Description	Conditions	Value			Unit
			Min	Typ	Max	
VCC Power Supply						
Vcc_start	VCC Startup Voltage		10.1	10.8	11.6	V
Vcc_uvlo	VCC Under-voltage Restart Threshold		8.5	9.1	9.8	V
Ivcc_st	VCC Startup Current				120	uA
Ivcc_op	VCC Operating Current				1	mA
Brown-in/Brown-out Detection						
Vin_pk(brnin)	Vin Power-On Recognition Voltage		103	108	115	V
Vin_pk(brnout)	Vin Power-Down Detection Voltage		86	90	96	V
Tzcd	Zero-Crossing Detection to GT Rise Delay Time			21		nS
COMP Regulation and Compensation						
GEA	Error Amplifier Transconductance Gain			50		uA/V
GEA_DRE	Error Amplifier Transconductance Gain in DRE State			300		uA/V
Vcomp_clamp	COMP Pin Clamp Voltage			5.5		V
Vcomp(stdh)	Standby Mode Exit Voltage Threshold			820		mV
Vcomp(stdl)	Standby Mode Entry Voltage Threshold			700		mV
Tsmin	Minimum PWM Off-Time			2		us
Tonmax	Maximum Turn-On Time	85Vac input		12.8		us
Tonmax@175Vac	Maximum Turn-On Time	175Vac input		2.66		us

CS Peak Current Detection						
Vcs(ocp1)	Vcs Threshold for Over-Current Protection (OCP1)		450	500	550	mV
Tleb_ocp1	Primary Over-Current Protection LEB Time			300		ns
Vcs(ocp2)	Vcs Threshold for Over-Current Protection (OCP2)			760		mV
Tleb_ocp2	Secondary Over-Current Protection LEB Time			150		ns
FB Output Voltage Detection						
Vfb(ref)	FB Reference Voltage	Rz=1K/Rz=4.7K,Icomp=0uA	2.45	2.50	2.55	V
Vfb(fovph)	FB Over-Voltage Detection Threshold	Rz=1K/Rz=4.7K	2.65	2.72	2.78	V
Vfb(fovpl)	FB Over-Voltage Recovery Threshold	Rz=1K/Rz=4.7K	2.57	2.64	2.7	V
Vfb(uvp)	FB Voltage for Vin Power-On Recognition			500		mV
Vfb(DREh)	FB High Threshold for Entering DRE State	Rz=1K/Rz=4.7K		2.58		V
Vfb(DREl)	FB Low Threshold for Entering DRE State	Rz=1K/Rz=4.7K		2.42		V
FB Output Voltage Detection(AC＜146V)						
Vfb_L(ref)	FB Reference Voltage	Rz=2.2K/Rz=10K,Icomp=0uA	1.62	1.65	1.68	V
Vfb_L(fovph)	FB Over-Voltage Detection Threshold	Rz=2.2K/Rz=10K	1.81	1.85	1.89	V
Vfb_L(fovpl)	FB Over-Voltage Recovery Threshold	Rz=2.2K/Rz=10K	1.76	1.8	1.84	V
Vfb_L(DREh)	FB High Threshold for Entering DRE State	Rz=2.2K/Rz=10K	1.7	1.73	1.76	V
Vfb_L(DREl)	FB Low Threshold for Entering DRE State	Rz=2.2K/Rz=10K	1.54	1.57	1.6	V
Internal Over-Temperature Protection						
Totp(in)	OTP Trip Temperature			150		℃
Totp(out)	OTP Release Temperature			120		℃
Power Transistor Parameters						
Rds_on	On-Resistance	V_{GS}=6V,I_D=3A,T_j=25℃,DK8310		196	260	mΩ
		V_{GS}=6V,I_D=3A,T_j=25℃,DK8312		160	210	mΩ
		V_{GS}=6V,I_D=5A,T_j=25℃,DK8318		101	130	mΩ
		V_{GS}=6V,I_D=0.5A,T_j=25℃,DK8320		75	100	mΩ
		V_{GS}=6V,I_D=3A,T_j=150℃,DK8310		441		mΩ
		V_{GS}=6V,I_D=3A,T_j=150℃,DK8312		360		mΩ
		V_{GS}=6V,I_D=5A,T_j=150℃,DK8318		230		mΩ
		V_{GS}=6V,I_D=6A,T_j=125℃,DK8320		151		mΩ
Coss	Output Capacitance①	DK8310		17.7		pF
		DK8312		23.6		pF
		DK8318		36.5		pF
		DK8320		47.2		pF
Ciss	Input Capacitance①	DK8310		49		pF
		DK8312		65		pF
		DK8318		101		pF
		DK8320		139		pF

Crss	Reverse Transfer Capacitance①	DK8310		0.2		pF
		DK8312		0.3		pF
		DK8318		0.4		pF
		DK8320		0.52		pF
* **Fault Protection Stop Time**						
Tstop	STOP time		1.89	2.1	2.31	s

Note: Conditions:Vgs=0V,Vsw=400V,F=100KHz

■ *OPERATION DESCRIPTION*

Startup

The chip is powered by the downstream VCC supply. When VCC is applied and detected to be greater than Vcc_start, the chip's internal control circuit begins operation.

Input Voltage Power-On Detection (Brown-in)

After power-on, the chip detects the Vin voltage via the SW pin. When Vin_pk > Vin_pk(brnin) is detected and simultaneously Vfb(fovpl) > Vfb > Vfb(uvp) is satisfied, the bus is determined to be successfully powered up, and the chip begins outputting PWM signals.

Input Voltage Brown-out Detection (Brownout)

During normal operation, the chip continuously monitors the Vin voltage in real-time through the SW pin. If Vin_pk < Vin_pk(brnout) is detected, the input voltage is determined to be in an undervoltage state. The chip then stops PWM output and enters the input voltage power-on detection state.

Line Voltage Power Compensation and Turn-On Control (Ton Time)

The chip monitors the input voltage (Vin) through the SW pin and adjusts the power transistor's turn-on time (Ton) based on both Vin and the Comp pin voltage. This ensures that the maximum input power is independent of the input voltage Vin, achieving compensation for the maximum input power across different line voltages.

Valley Switching

After the power transistor turns off, the inductor enters the demagnetization phase. The chip detects the power transistor's drain-source voltage (Vds) through the SW pin. When demagnetization ends, the power transistor is turned on at the valley of the Vds voltage, reducing switching losses.

DCM and CRM Modes

By monitoring the COMP pin voltage, the chip operates in Critical Conduction Mode (CRM) under heavy loads to provide good efficiency. Under light loads, it automatically switches to Discontinuous Conduction Mode (DCM) to reduce the switching frequency, achieving good light-load efficiency.

Segmented Output Voltage Function

Segmented Version: The chip detects the input voltage (Vin) through the SW pin.

When the input voltage is less than 146 Vac, the FB reference voltage drops to 1.65V, corresponding to a typical output voltage of 264 Vdc. This effectively reduces the conduction losses of the PFC power transistor at 90 Vac input.

When the AC input voltage is greater than 170 Vac, the FB reference voltage returns to 2.5V, corresponding to a typical output voltage of 400 Vdc.

Fixed Output Version:By default, this version lacks the segmented output voltage function, and the FB reference is fixed at 2.5V.

Standby (STDBY) Mode

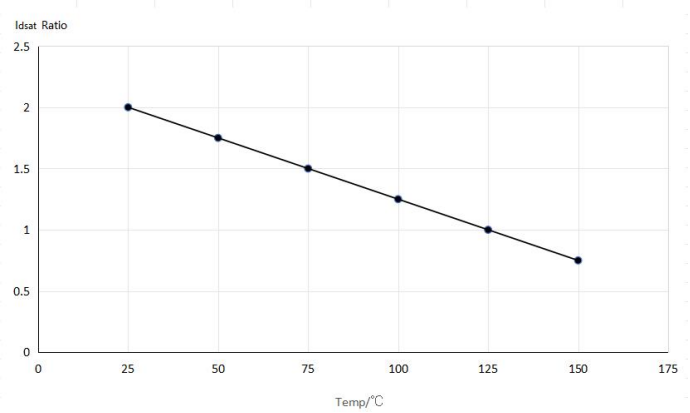
The chip enters STDBY mode when the COMP pin voltage Vcomp is detected to be less than Vcomp(stdl). The chip exits STDBY mode when Vcomp is detected to be greater than Vcomp(stdh).

Enhanced Error Amplifier (DRE)

The chip utilizes an Enhanced Error Amplifier (EA) to optimize dynamic performance. When the FB voltage rises above Vfb(DREh), the fast response loop of the EA is activated, speeding up the loop response and accelerating the discharge of the COMP pin voltage. Conversely, when the FB voltage falls below Vfb(DREl), the fast response loop is activated to speed up the loop response and accelerate the charging of the COMP pin voltage. This Enhanced EA improves the response speed during load transients, enhances system stability, and reduces component stress.

GaN Device Current Capability

For gallium nitride (GaN) power devices, temperature is a critical factor affecting current capability. The provided normalized curve illustrates the relationship between device current capability and junction temperature. Using TJ=125°C as the reference, the device's current capability at other junction temperatures can be calculated based on the actual operating junction temperature.



Output Over-voltage Protection (FOVP)

When the chip detects Vfb > Vfb(fovph), it stops the PWM output. PWM output is resumed only after Vfb is detected to be below Vfb(fovpl).

Output Under-voltage Protection

When the chip detects Vfb < Vfb(uvp), it stops the PWM output and enters the input voltage power-on detection state.

VCC Under-voltage Lockout (UVLO)

When the chip detects VCC < Vcc_uvlo, it stops the PWM output and enters a reset state.

Bypass Diode Short-Circuit Protection

If the chip detects a short circuit in the bypass diode, it stops the PWM output and enters STOP mode.

Over-current Protection (OCP1, OCP2)

The chip monitors the power transistor current through the CS pin to provide cycle-by-cycle current limiting.

OCP1:If, after the PWM turns on and after a blanking time of Tleb_ocp1, the CS pin detects Vcs > Vcs(ocp1), OCP1 protection is triggered, and the PWM is immediately turned off.

OCP2:If, after the PWM turns on and after a blanking time of Tleb_ocp2, the CS pin detects Vcs > Vcs(ocp2), OCP2 protection is triggered, the PWM is immediately turned off, and the chip waits for 1ms before allowing the PWM to restart.

If Vcs > Vcs(ocp2) is detected for three consecutive PWM cycles, the chip enters STOP mode.

RCS Resistor Open-Circuit Protection

If the chip detects an open circuit in the RCS resistor, it stops the PWM output and enters STOP mode.

Over-Temperature Protection (OTP)

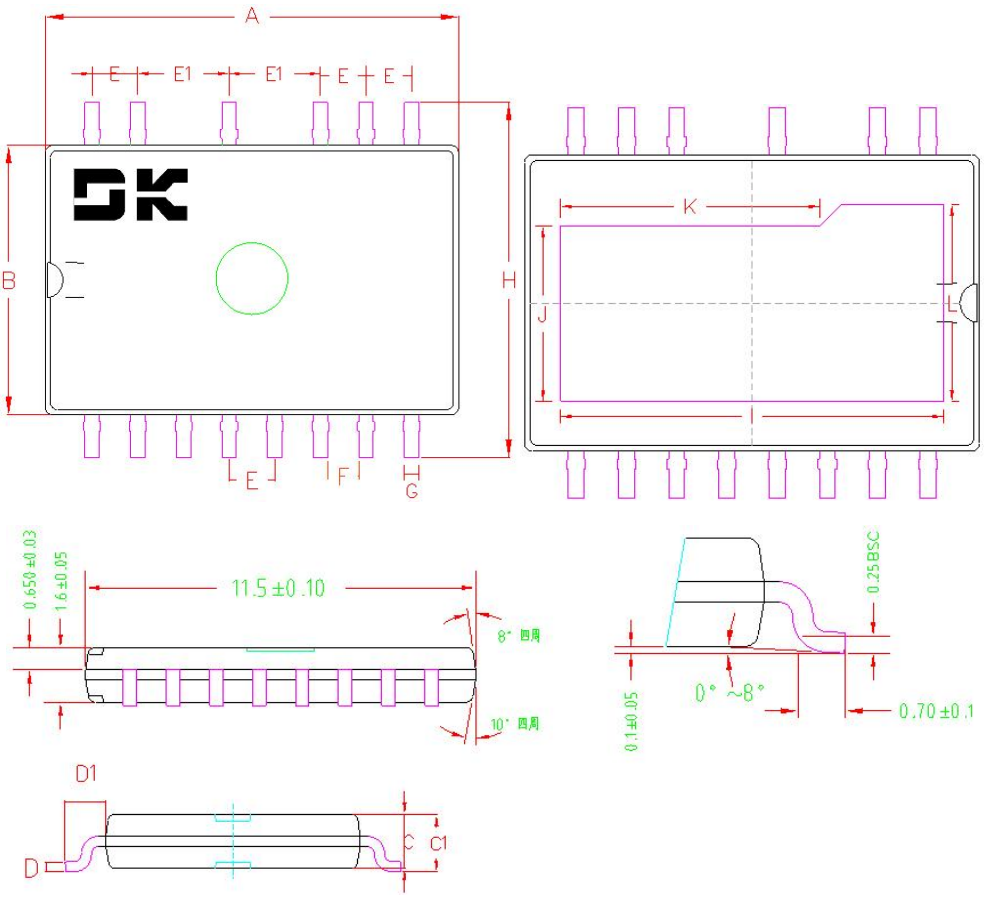
The chip incorporates an internal OTP circuit. If the chip temperature exceeds Totp(in), it disables the PWM output. Once the chip temperature drops below Totp(out), the chip re-enters the input voltage power-on detection state.

STOP Mode

The chip enters STOP mode when it detects an OCP2 event or a bypass diode short-circuit. After waiting for a duration of Tstop, the chip re-enters the input voltage power-on detection state.

■ *PACKAGE OUTLINE DIMENSIONS*

ESOP16L



Symbol	Dimensions In Millimeters		
	Min	NOM	Max
A	11.40	11.50	11.60
B	7.40	7.50	7.60
C	1.55	1.60	1.65
C1	1.65	1.70	1.75
D		0.30(BSC)	
D1	1.10	1.20	1.30
E		1.27(BSC)	
E1		2.54(BSC)	
F	0.75	0.80	0.85
G	0.40	0.42	0.45
H	9.80	10.00	10.20
I	9.60	9.70	9.80
J	4.35	4.45	4.55
K	6.47	6.57	6.67
L	4.90	5.00	5.10